Application Note for Molded Plastic QFN/DFN Packages

Monolithic Packaged Microwave IC

1. General considerations on plastic molded packages

SMD* packaged MMIC are now massively adopted for microwave and millimeter-wave applications. The use of such packages requires some specific knowledge in order to optimize the performances. In particular, the design of the motherboard has a strong impact on the overall performance since transition from the package leads to the transmission lines can lead to strong parasitic effects.

The UMS RoHS* compliant plastic QFN*/DFN* packages, SMT* compatible are appreciated for their very good electrical and thermal performances at low cost. Thanks to a limited area and very short leads, they perfectly suit to the microwave circuits where the package's parasitic elements must be as small as possible in order to be negligible at high frequency. A lead to lead pitch of 0.5mm gives the best trade-off between electrical performances and industrial constraints up-to 40GHz.
The performances of the packaged products are optimum when the effects of the package are taken into account during the design of the MMIC*.
The lead-frame structure made of copper (C194 alloy) includes small leads but also a large metallic exposed-pad acting as an efficient ground-pad and a thermal drain to the PCB* circuit. So, the thermal and electrical ground paths are optimum, and the embedded MMIC is working in very good conditions (see Figure 1).

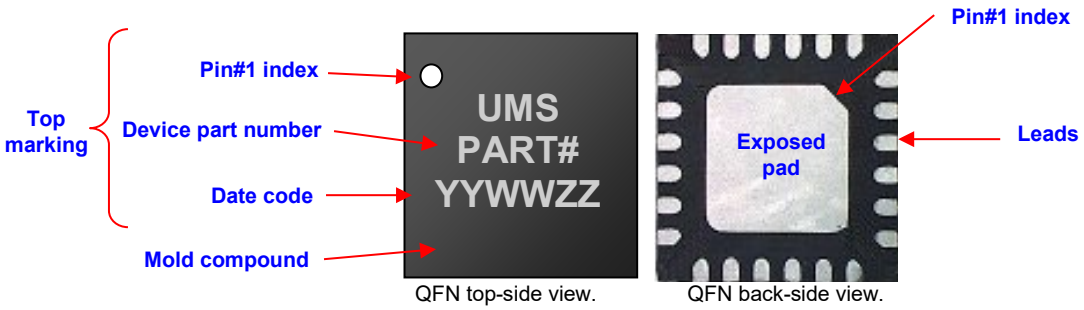

Figure 1 : QFN package outline.

United Monolithic Semiconductors S.A.S.
Bât. Charmille - Parc SILIC - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34 - www.ums-rf.com

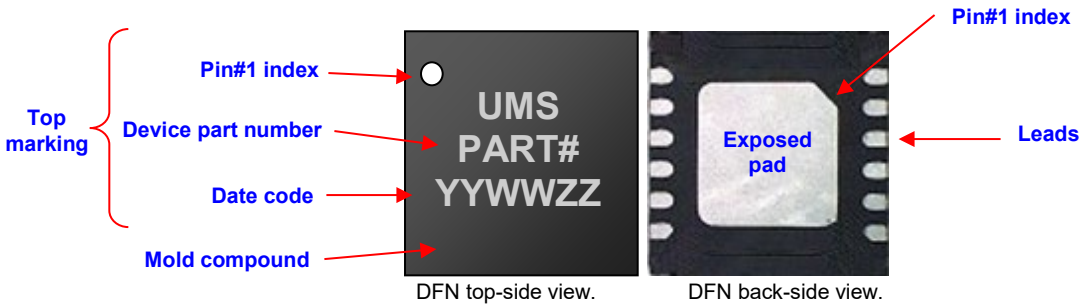

Figure 2 : DFN package outline.

* *See Glossary*

Packages are LASER marked on top-side as shown on the Figure 1 and Figure 2. The package top marking includes a Pin#1 index and three lines of text used for the device identification.

- Line 1: UMS logo.
- Line 2: device part number.
- Line 3: date code
  - YY stands for the two last digits of the assembly year.
  - WW stands for the week in the assembly year (from 01 to 52).
  - ZZ are two optional characters used internally at UMS for lot identification.

Remark: In some cases, samples or prototypes can be marked with white ink.

The mold protection of the plastic QFN/DFN acts as a very good mechanical protection for SMT handling steps.

A product qualification must include a set of environmental and ageing tests [4].

The UMS's QFN/DFN plastic packages are compliant with RoHS directive (Pb* free). The list of the materials constituting the product is given on the Figure .

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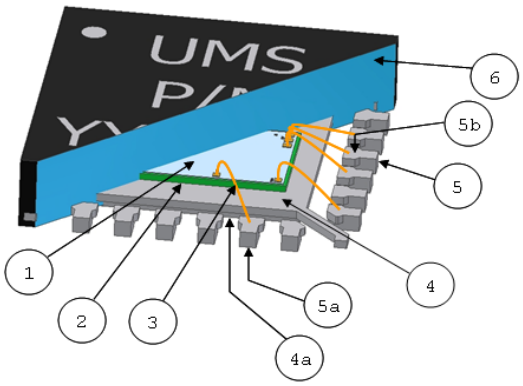

No.	Name	Material	Note
1	MMIC	GaAs	
2	Die attach	Epoxy resin with silver filler	
3	Bonding Wire	Gold	
4	Frame	Copper (C194) with Sn external finish	Sn finish on back side, see 4a
4a	Frame external Sn finish	Matte tin (Sn), thickness 400 µinch	Package's exposed surfaces only
5	Lead	Copper (C194) with Sn external finish	Sn finish on back side, see 5a Ag finish on top side, see 5b
5a	Lead external Sn finish	Matte tin (Sn), thickness 400 µinch	Package's exposed surfaces only
5b	Lead bond pad Ag finish	Silver spots (Ag), thickness <40 µinch max.	Lead's internal bond area
6	Mold Resin	Multi-Aromatic Resin (Br/Sb free)	

Figure 3 : Example of QFN/DFN products build-up structure.

Some UMS QFN/DFNs are also available with a NiPdAu treatment of the bottom contacts and remain compatible with the RoHS SMT assembly processes on PCB.

The QFN/DFN devices are designed to be mounted onto any standard PCB compatible with SMT process. But, of course at millimetre-wave frequencies a special care must be taken at the PCB level to manage a good electrical and thermal matching of the device. This application note gives guide lines and recommendations in order to design the appropriate motherboard and take advantage of the best circuit performances. Further information can be available under request. However, UMS reminds that the customer is responsible of the development of their PCB.

2. UMS's QFN/DFN packages outlines

Considering the specificities of the microwave products and the impact of the package on the device performances, UMS proposes several dimensions of over-molded plastic packages in order to match perfectly with the specificities of each MMIC. This family of packages complies with high performances and takes advantage of the standard low cost assembly solutions available today for mass production.

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Bât. Charmille - Parc SILIC - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
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The table below gives some available QFN/DFN sizes at UMS:

Package case	*UMS designation*	*Package Outlines*
QFN 3x3, 16 leads	QAG	See annex 6.1
QFN 3x3, 16 leads, 2RF fused leads	QAG	See annex 6.2
QFN 4x4, 24 leads	QDG	See annex 6.3
QFN 4x4, 24 leads 2RF fused leads	QDG	See annex 6.4
QFN 4x5, 24 leads	QEG	See annex 6.5
QFN 5x5, 32 leads	QFG	See annex 6.6
QFN 5x6, 36 leads	QXG	See annex 6.7
QFN 6x6, 40 leads	QJG	See annex 6.8
DFN 2x2, 8 leads	QKA	See annex 6.9

The package outlines have been defined based on the JEDEC MO-220 standard [1].

3. PCB design

This paragraph presents some recommendations shared by UMS to design the PCB. The development of the PCB must be a point of attention for the functionality of an enhanced motherboard, nevertheless this development strongly depends on each customer's solution and UMS doesn't propose a standard.

3.1. General considerations for PCB design

The products developed by UMS are tested on an evaluation board in order to guarantee the best performances at the customer level in the equipment. Since the internal design of the MMIC is generally based on a micro-strip structure, the motherboard where the QFN/DFN device will be mounted should be designed in accordance with this configuration. Indeed, the motherboard acts as a:

Signal feeding structure to the QFN/DFN device: Transmission lines are needed on the PCB. For electromagnetic reasons, a micro-strip mode is generally chosen and helps to avoid parasitic propagations modes on the PCB. It will also help to minimize the electrical transmission losses. The UMS' QFN/DFN packages are generally designed to be matched on 50Ω loads. However, the motherboard in the close area around the QFN/DFN device should be designed to have a good impedance transition from the micro-strip line to the package leads.

The main electrical grounding of the QFN/DFN: Since the QFN/DFN device at millimeter-wave frequencies contains generally a micro-strip chip, it is necessary to provide a very good grounding of the package to the PCB's ground. The main ground interface between the package and the motherboard is done through the package

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exposed pad (see Figure 1 and figure 2) which is soldered to the PCB's ground pad (see figure 4) in the case of a SMT mounting process.

The link between the ground of the sub-system and the ground pad on the motherboard is generally done using a metallic via-hole structure. A very standard configuration with metallic via holes to connect the sub-system ground at the PCB's back-side interface to the package exposed pad is presented Figure .

The main heat-sink of the QFN/DFN: The QFN/DFN package thanks to its copper lead-frame has very good thermal performances. The dissipated power is easily spread out from the package through the exposed pad to the PCB. Via holes in the PCB will act as thermal drain to dissipate the thermal energy to the main heat-spreader of the sub-system (see Figure).

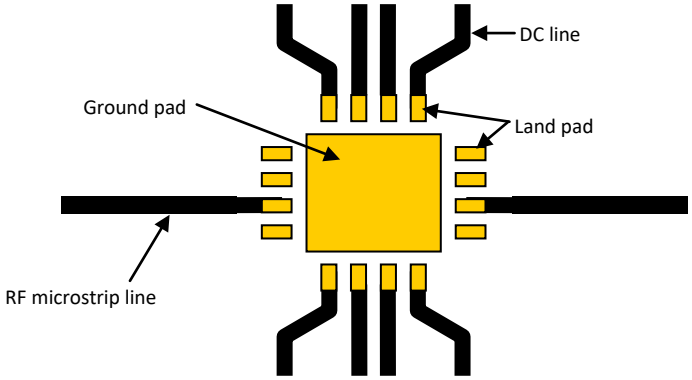

Figure 4 : General overview of a QFN motherboard.

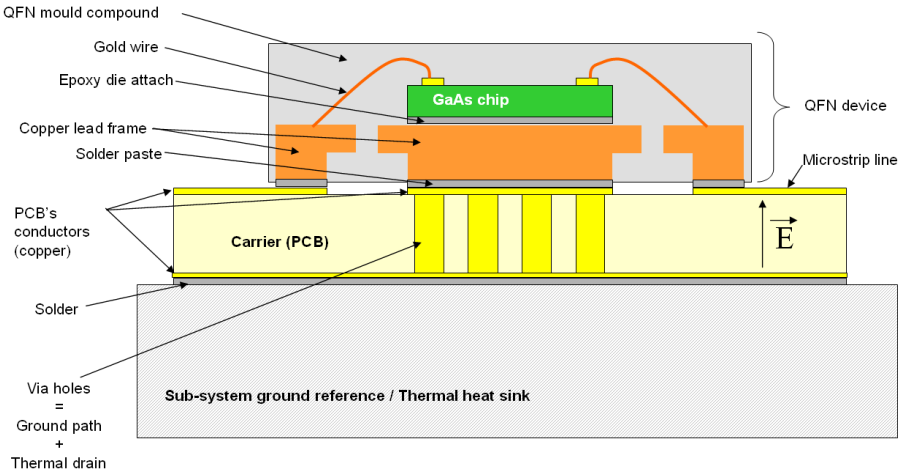

Figure 5 : Cross section view of a QFN device assembled on a PCB.

3.2. Typical UMS evaluation boards

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SMD type packages from UMS allow the design and fabrication of mm-wave modules at low cost. Therefore, a suitable motherboard environment was chosen according to this aim. All tests and verifications were performed on Rogers RO4003. This material has a permittivity of 3.38 and is used with a thickness of 203µm [8mils] and a 1/2oz or less copper cladding. The corresponding 50Ohm transmission line should have a strip width of about 460µm [approximately 18mils]. Other materials with similar properties can be used as well.

The product datasheet generally includes the recommended motherboard used for the product characterization. Sometimes, for different products with a same package size, slight differences can be observed between the motherboard proposed in the datasheet. These differences might come from product specificities.

It is recommended to use as much as possible the proposed layout and technology shown in the product's datasheet in order to achieve the best performances out of the packaged product.

3.2.1. Recommended package footprint on PCB

The QFN/DFN packages outline drawings can be provided as DXF CAD files on request in order to help to design the PCB footprint.

Most of the electrical tests done at UMS are performed on a demonstration board with a grid of plated via-holes through the substrate with a diameter of less than 300µm [12mils] and a spacing lower than 700µm [28mils] from the centres of two adjacent via holes. Via holes grid should cover the whole area of the ground pad.

In order to improve the impedance matching, the nearest via holes to the RF ports should be as close as possible from the edges of the PCB ground pad which should be shaped as a CPW structure (ground / signal / ground) surrounding the RF port (see Figure).

Since via holes are also important for heat transfer, a proper via filling should be guaranteed during the mounting procedure to get a low thermal resistance between the package and the heat sink. However, it is important to consider that via holes internal copper plating will always act as the main thermal drain.

Via filling is also recommended for SMT assembly reasons. Conductive epoxy or any other appropriate thermal conductive material can be used before solder past deposition in order to avoid solder wicking into via holes during the reflow process. This configuration will help to decrease the thermal resistance of the PCB structure, but it will also avoid low package stand-off height.
For the power devices, the use of heat slugs in the motherboard instead of a grid of via holes is recommended.

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Bât. Charmille - Parc SILIC - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
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The table hereafter gives the via holes geometry for some examples of QFN/DFN package size.

	QKA DFN 2x2 8L	*QAG QFN 3x3 16L*	*QAG QFN 3x3 16L 2RF fused lead*	*QDG QFN 4x4 24L*	*QDG QFN 4x4 24L 4RF fused lead*	*QEG QFN 4x5 (or 5x4) 24L*	*QFG QFN 5x5 32L*	*QXG QFN 5x6 36L*	*QJG QFN 6x6 40L*
Via-hole external diameter (mm)	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3
Via-hole internal diameter (mm)	0.2	0.2	0.2	0.2	0.2	0.2	0.2	0.2	0.2
Number of vias under the package	9	9	9	16	16	30	36	42	49
Via holes pitch (mm)	0.50	0.60	0.60	0.60	0.60	0.60	0.60	0.60	0.60
Via holes height (=PCB thickness) (mm)	0.203	0.203	0.203	0.203	0.203	0.203	0.203	0.203	0.203
$R_{th\_PCB\_UMS}$: Estimated thermal resistance equivalent to the package footprint on PCB (°C/W)	~1.3	1.46	1.46	0.82	0.82	0.44	0.36	0.31	0.27

3.3. Recommendations for PCB design adjustments

Several parameters may influence the design of mother board required for the application as:

- the PCB stack-up structure
- the PCB materials properties
- the PCB thermal capacitance
- the PCB patterns resolution
- the solder paste properties
- the fabrication tolerances of the stencil printer
- the pick & place equipment placement accuracy
- the reflow process

Since it is not possible to define a generic motherboard layout fully compatible with all the industrial SMT processes, this paragraph intent to provide some guides line to adjust the PCB design for a better adaptation to the selected SMT process. But the recommendation given here after should not replace the design rules provided by the industrial assembler who will consider all the parameters and the equipments capabilities to achieve the best yield in production.

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3.3.1. Guide lines for package footprint adjustments

The footprint recommended in the paragraph 3.2.1 should be used to design the application motherboard. But in some cases, for industrial assembly reasons (stencil printer complexity, solder past selected, PCB material, etc…) it could be necessary to decrease the via-hole density under the package.
The impact of low via holes density below the package might have very bad effect on the device performances:

- The PCB thermal resistance will increase. Then the ambient maximum temperature must be adjusted in order to keep the case temperature (Tcase, see Figure) below the maximum value specified in the product datasheet.

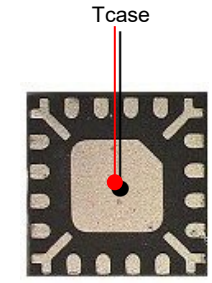

Figure 6 : Temperature reference point (Tcase) considered in the product datasheet.

Remark: A similar effect on the device thermal performances is observed when the PCB thickness increases.

- The electrical grounding of the package could be also affected. It's recommended to locate the via holes at the edges of the ground pad area and RF Pad as recommended on the UMS's footprint drawings in order to avoid device mismatch of unsuitable propagation modes (see black filled hatched or squares on the Figure , the un-filled squares correspond to the thermal via holes).

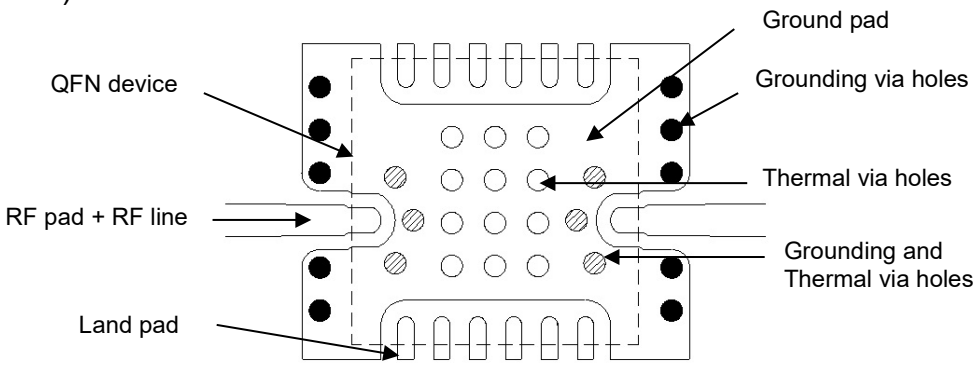

Figure 7 : Example of via holes matrix on the PCB foot print.

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Remark: A modification of the package footprint should be done only after an analysis of the impact on the device electrical and thermal performances.

3.3.2. Guide lines for solder mask adjustments

For compact and low pitch packages as for QFN/DFN packages it's difficult to prevent the solder bridging. Generally, a solder mask is used to avoid this kind of issues in production. The solder mask will also help to define the areas where the solder can flow and control the solder homogeneity under the package contacts (leads and exposed pad). Then the quality and the reliability of the solder join are enhanced.

The recommended solder mask clearance around the copper pads on the PCB for land pads is 70µm [2.8mils] as shown at Figure 9.
Concerning the package ground pad, it is recommended to manage an overlap of 70µm [2.8mils] minimum on the solder mask over the copper pad (see Figure). This configuration is suitable for self-centring of the package on the PCB footprint during reflow process.

The information's given in this paragraph are only indicative and should not replace the design rules of the PCB manufacturer. Furthermore, the solder mask design must also take into account the final SMT assembly process used for module as well as the selected solder past characteristics.

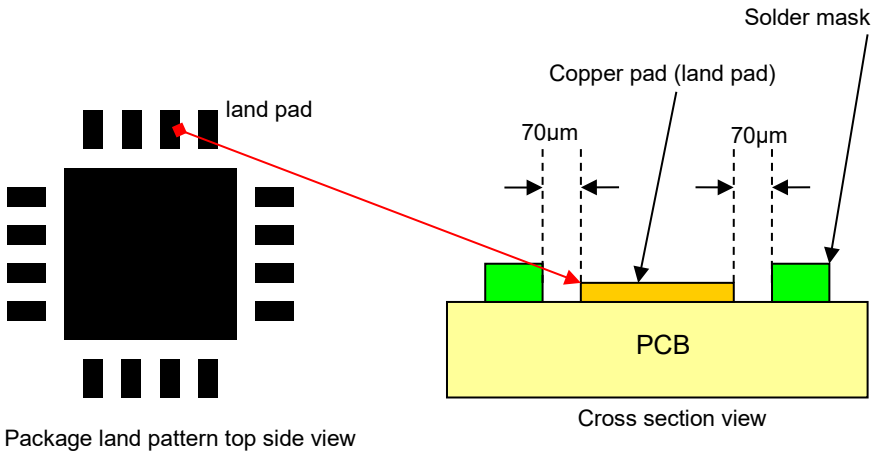

Figure 8 : Solder mask clearance around the land pads.

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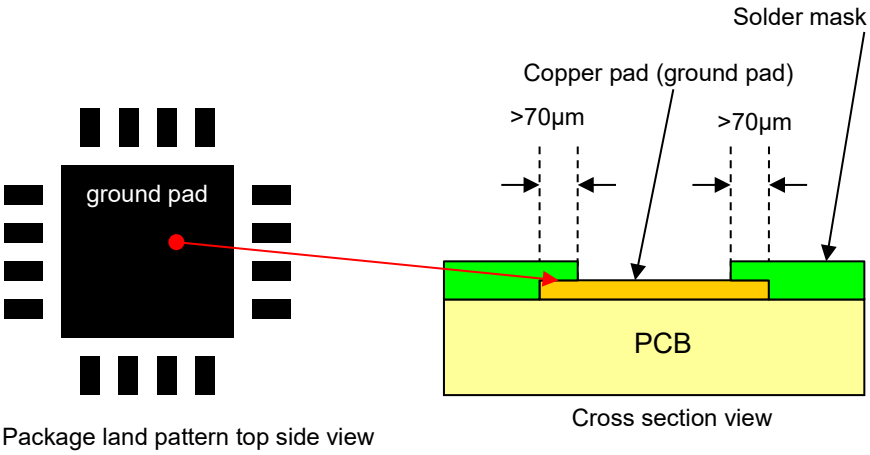

Figure 9 : Solder mask clearance around the ground pad.

3.3.3. Recommendation for stencil printer

The choice of the stencil printer is very critical and must be done by the SMT assembler. The design of the stencil must be done in accordance with the solder paste material selected and the printing equipment capability. The guide lines given below are very general and only the assembler design rules might be considered for the product industrialization.

The solder paste deposition for a small pitch package is very sensitive to the process, and should fit with the deposition on very small surfaces like the land pads (lead contact surface is less than 0.1mm²) but also on large surfaces as for the ground pad (from 2.5mm² for a QFN 3x3 to 12mm² for a QFN 5x5).
The squeegee blade used to deposit the solder paste into the stencil cavities could bend in the larger cavities and then limit the amount of solver paste deposited. A very convenient method used to solve this issue is to split the exposed pad surface into an array more compatible with the smallest zones defined for the land pads.

In principle the stencil aperture opening above the land pad is smaller than the copper land pad (about 50µm [2 mils] in the two directions, see Figure).
The stencil design for the exposed pad region results from trials and evaluations on pre-serial batches in order to define the optimum pattern. Two examples of configuration are given on Figure 11
.

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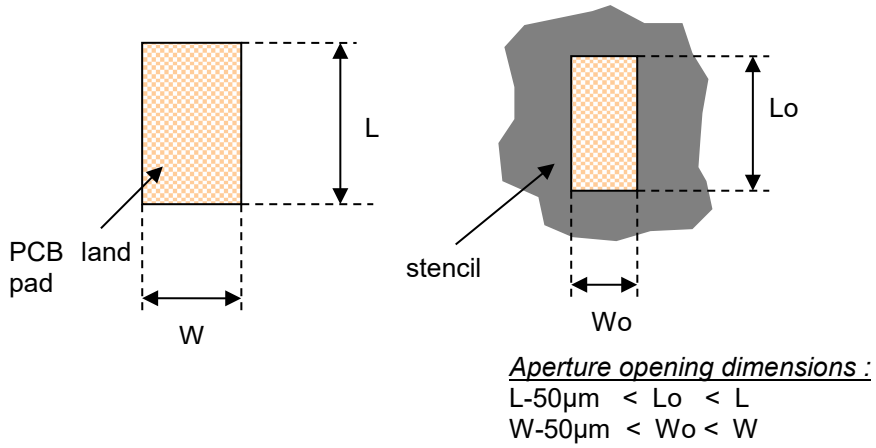

Figure 10 : Stencil aperture opening for land pads.

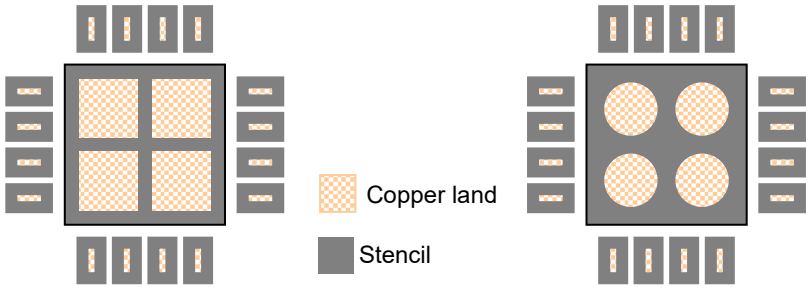

Figure 11 : ground pad stencil examples.

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4. PCB assembly

4.1. SMT assembly process flow

For the assembly process, the QFN/DFN type package can be handled as a standard surface mount component (please refer to the IPC/JEDEC J-STD-020C standard or equivalent [2]). The use of solder is recommended, standard techniques involving solder paste and reflow process can be used (e.g. stencil solder printing, standard pick-and-place equipment, and solder reflow oven). However, caution should be taken to perform a good and reliable contact over the whole pad area. The standard SMT process flow is given on the Figure 12.

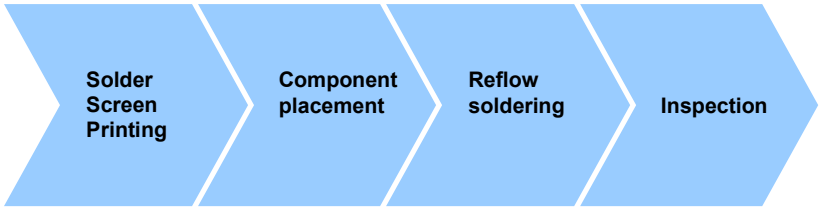

Figure 12 : Standard SMT process flow.

4.2. Bill of materials

- Motherboard (typically RO4003 or equivalent, 203µm thickness).
- SMD product.
- SMD components that might be necessary.
- Solder paste (RoHS compliant, but SN63/Pb37 might be used also).
- An appropriate solder stencil printer.
- A hot plate or a reflow oven.

4.3. Component placement

UMS proposes antistatic tubes or tape&reel as standard delivery conditioning for QFN/DFN devices.
Tape&reel conditioning is appreciated for automatic SMT assembly lines. The QFN/DFN devices are orientated in the tape&reel pockets as shown on Figure 14 and following the norm EIA-481 Rev C [5]. Automatic recognition systems will detect the QFN/DFN orientation in the tape&reel pocket to align the device on the PCB.
In spite of discrepancies between suppliers that could affect the recognition system (top marking aspect, the lead finish aspect), the relative position of the Pin#1 indicator on top marking to the tape&reel feeding direction is the key parameter to drive the placement process.

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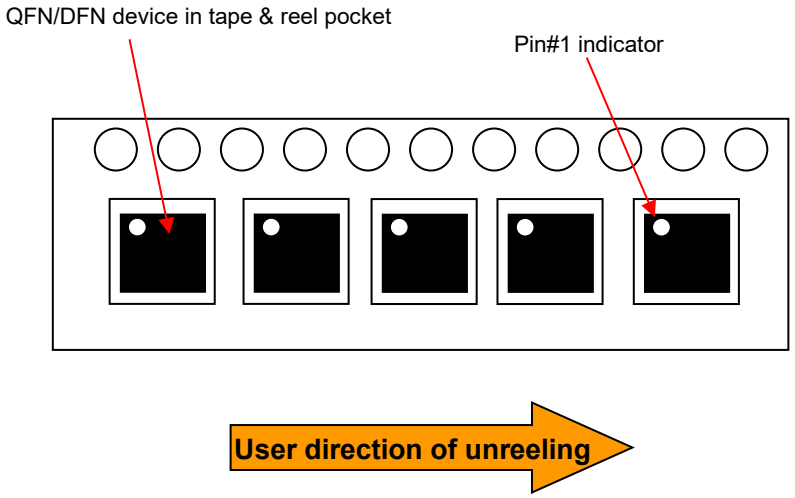

Figure 13 : QFN/DFN orientation in tape&reel conditioning.

4.4. Reflow soldering

The reflow temperature control will directly impact the mechanical robustness and the life time of the product during its operating life.

A typical reflow profile for the UMS QFN RoHS devices (mat tin lead finish) is presented on Figure 14.
It is preferable to follow solder manufacturer recommendations, per J-STD-020.

Figure 2 : Recommended reflow temperature profile for lead free solder (RoHS).

The solder thickness after reflow should be typically 50µm [2mils] and the lateral alignment between the package and the motherboard should be within 50µm [2mils].

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It is important for the performance of the product that the whole overlapping area between the motherboard and package pads is connected. Voids or improper connections, in particular, between the ground pads on the motherboard and the package will lead to a deterioration of the RF performance and an increase of the device thermal resistance. Finally, the reliability and the lifetime of the product might be affected.

4.5. Moisture sensitivity level (MSL)

The QFN/DFN package is a non-hermetic solution, and considering that the mold compound trends to absorb moisture, some precautions have to be taken before the device assembly on PCB.

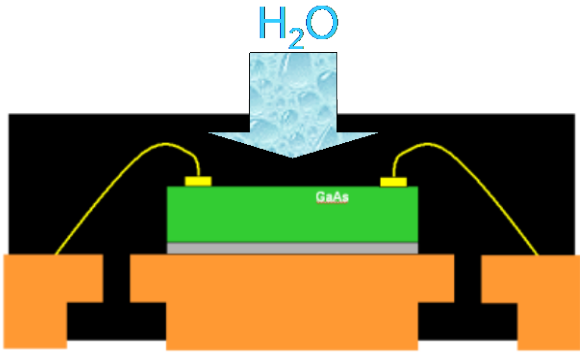

Figure 15: Moisture absorption through the QFN mold compound.

During the assembly reflow the moisture absorbed by the mold compound after storage will be vaporized. Then depending on the percentage of humidity contained in the resin, high mechanical constraints might be applied to the package.

The MSL* is an indicator for the maximum allowable time period (Floor Life Time) during which a moisture sensitive plastic device, once removed from the dry bag, can be exposed to an environment with a maximum temperature of 30°C and a maximum relative humidity of 60%RH or 85%RH before the solder reflow process:

MSL Level	***MSL4***	***MSL3***	***MSL2A***	***MSL2***	***MSL1***
Floor Life (out of bag) at factory ambient	72hours	168hours	192hours	1year	Unlimited
Max. storage temperature	≤30°C	≤30°C	≤30°C	≤30°C	≤30°C
Max. storage relative humidity	≤60%RH	≤60%RH	≤60%RH	≤60%RH	≤85%RH

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For details, refer to IPC/JEDEC J-STD-020C [2].

MLS1 is easier to achieve on the small packages than on the large ones as QFN 4x5 and 5x5.

For MSL4 to MSL2, if during the device storage time none of the conditions below has been exceeded, the device Floor Life Time can be reset after a baking.

- Condition 1: Floor Life Time exceeded and storage conditions during this time ≤30°C and ≤60%RH.
- Condition 2: Device storage conditions have never exceeded ≤40°C and ≤85%RH.

The backing conditions are described in the table below:

Package Body thickness ≤1.4mm	Bake @ 125°C		Bake @ 90°C ≤5%RH		Bake @ 40°C ≤5%RH	
	Exceeding Floor Life by>72h	Exceeding Floor Life by≤72h	Exceeding Floor Life by>72h	Exceeding Floor Life by≤72h	Exceeding Floor Life by>72h	Exceeding Floor Life by≤72h
Bake duration @ MSL2	5hours	3hours	17hours	11hours	8days	5days
Bake duration @ MSL2a	7hours	5hours	23hours	13hours	9days	7days
Bake duration @ MSL3	9hours	7hours	33hours	23hours	13days	9days
Bake duration @ MSL4	11hours	7hours	37hours	23hours	15days	9days

For details, refer to IPC/JEDEC J-STD-033B [3].

4.6. Inspection

The quality of the solder joint will be inspected by X-Ray analyse. This technique helps to detect a defective brazing quality where solder voids are present under the package exposed pad.

The solder joint quality can be also inspected on the lead edges. After the QFN/DFN singulation the lead endings of the UMS's packages are visible at the package edges (see Figure 16). During the reflow process, the solder will melt on these surfaces. This configuration has two main advantages. Firstly, the solder joint on the lead edges help to get a robust lead to the PCB attachment. Secondly, a standard visual inspection can confirm that all the package leads are connected to the PCB.

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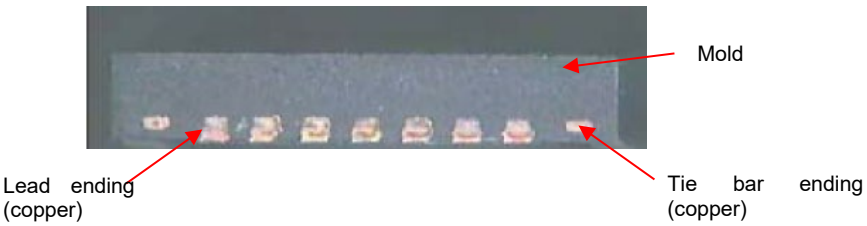

Figure 16: QFN side view showing the lead endings after dicing.

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4.7. Procedure for prototyping

The different steps are:

1. The motherboard should be cleaned with Acetone and rinsed with alcohol and DI* water. Afterwards the circuit should be fully dried.

2. The solder paste dispense should be done according to the patterns shown in the paragraph 3.3.2. It is important to note that an excessive use of solder paste can cause electrical shorts leading to poor RF performances.

3. A packaged product should be placed on the motherboard with a correct orientation and a good alignment (see the corresponding product datasheet). The alignment can be done manually by centring the packaged MMIC on the motherboard.

4. Then a reflow of the assembly should be performed on a hot plate for 5 to 6 seconds. The temperature of the plate surface should be about 240°C – 260°C.

5. The assembly should cool down completely after the reflow process.

6. The whole assembly should be finally cleaned with acetone and rinsed with alcohol and DI water.

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5. Datasheet electrical information and de-embedding method for the scattering parameters exploitation

The RF performances of the QFN device might be enhanced by slight impedance re-matching on the PCB in a dedicated frequency sub-band depending on the actual specific requirements of the application. To ease such design of the custom motherboard, the Sij (scattering) parameters of the UMS device are provided in the product datasheet and can be also supplied as a Touchtone file (.s2p).

Without another notice in the product datasheet, these Sij parameters are given in the calibration plans located by de-embedding at 1.1 mm from the edge of the QFN/DFN package as shown at Figure 17

.

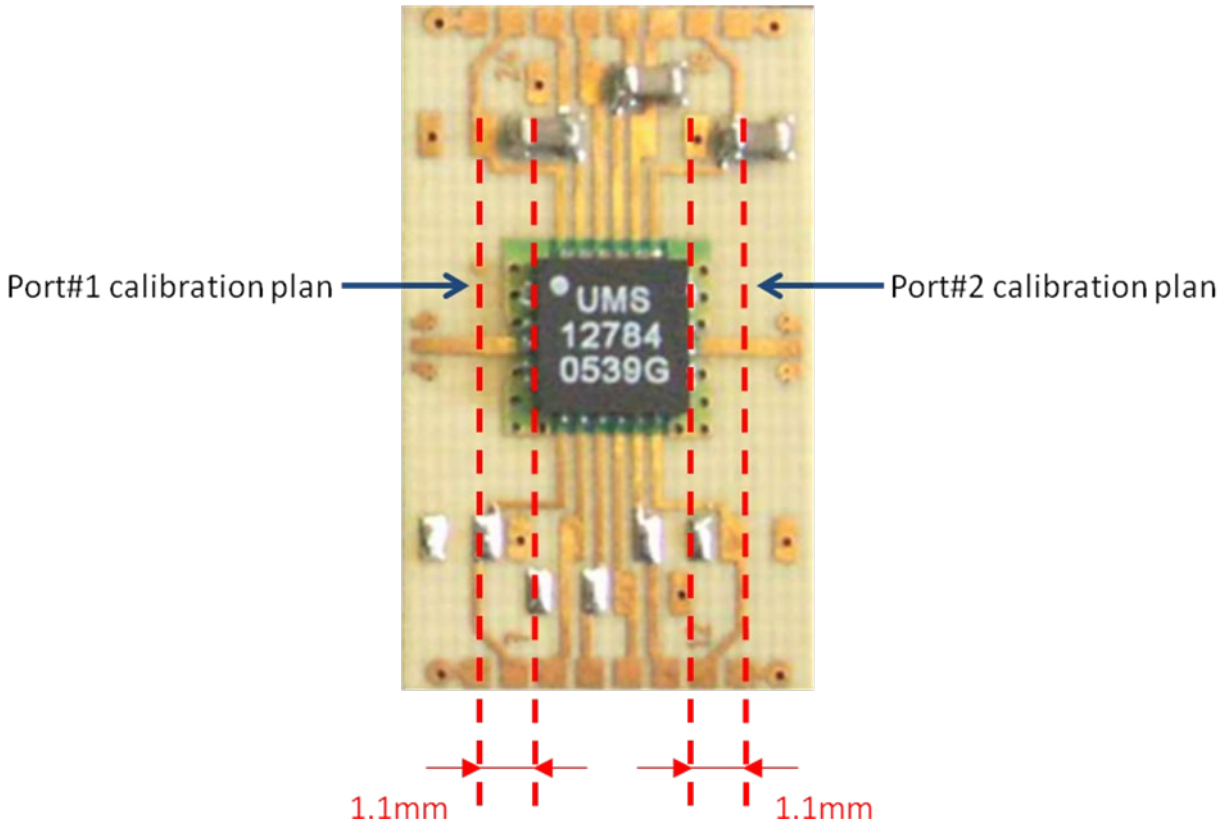

Figure 17: Location of the calibration plan for scattering parameters measurements.

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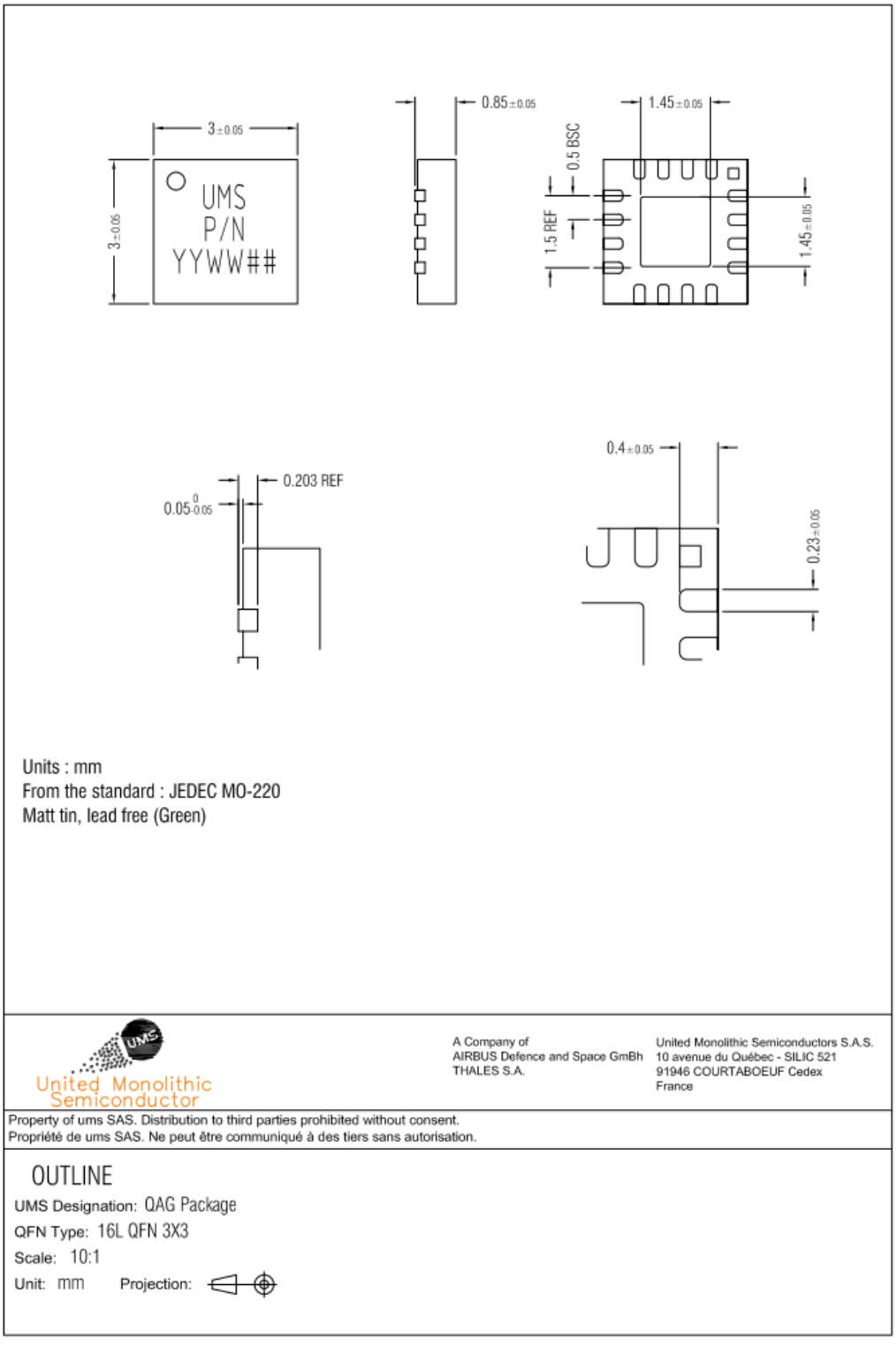
6. Annex 1: package outlines

6.1. QFN 3x3, 16 leads (QAG)



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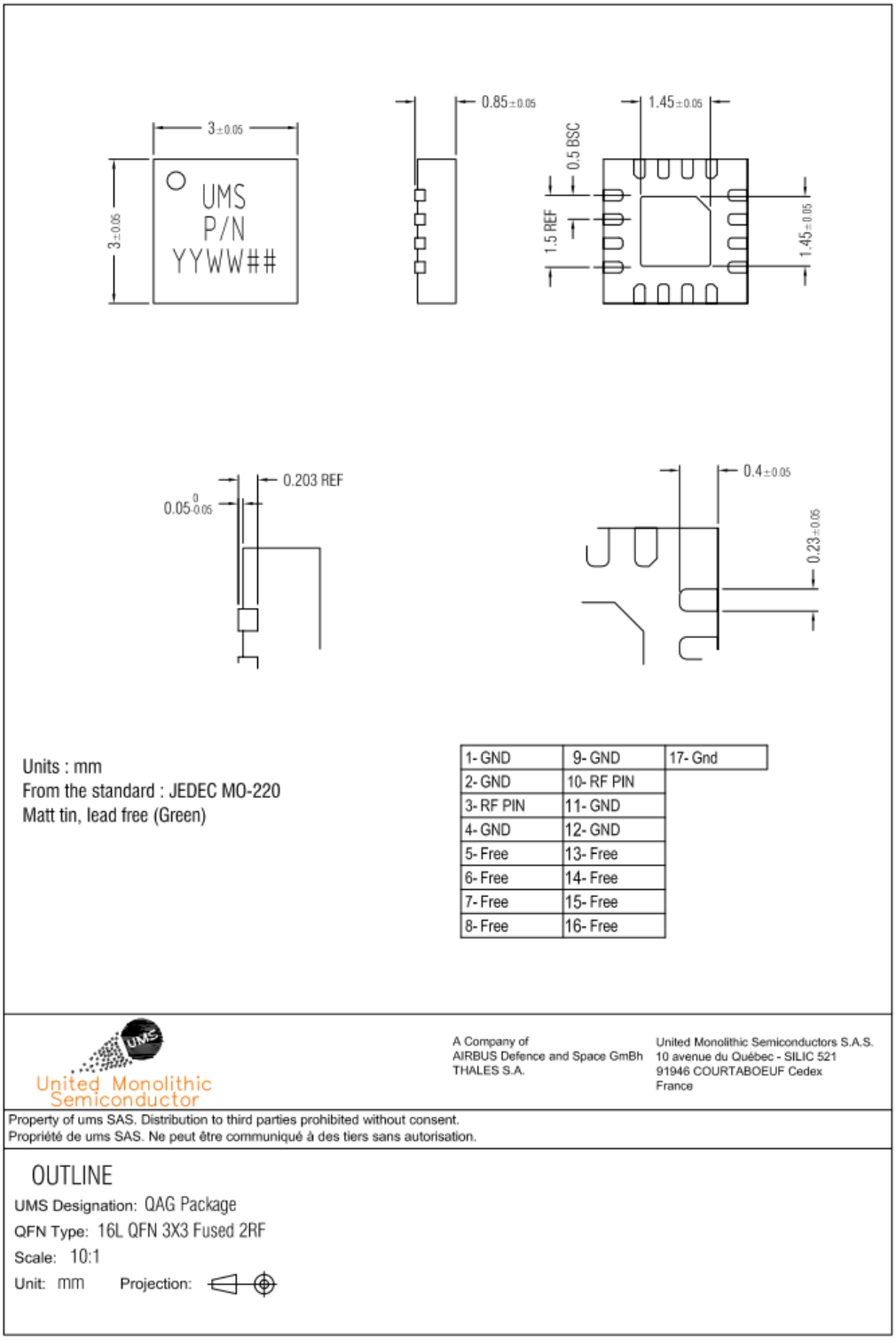
6.2. QFN 3x3, 16 leads (QAG) 2RF fused Leads



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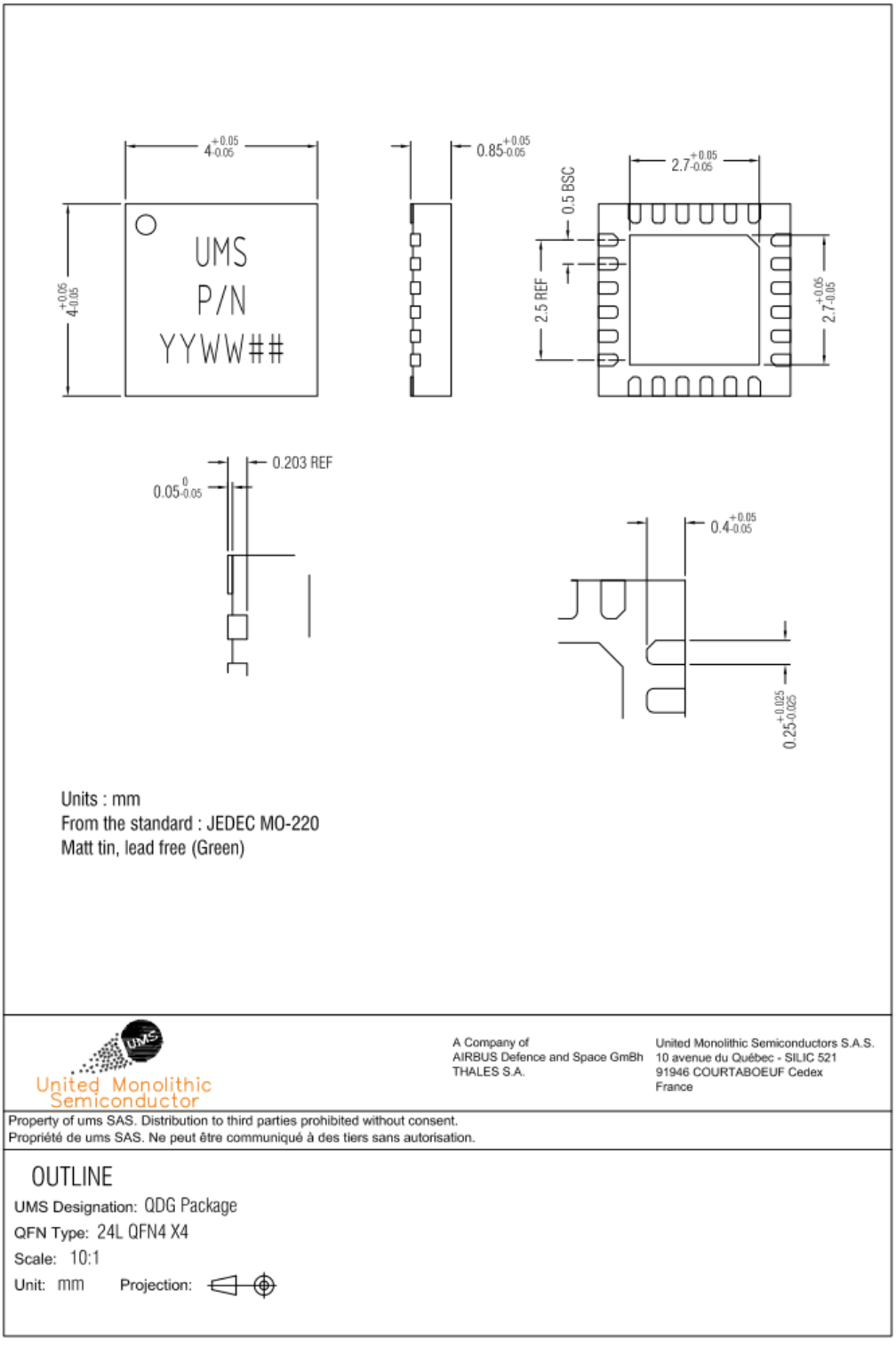
6.3. QFN 4x4, 24 leads (QDG)



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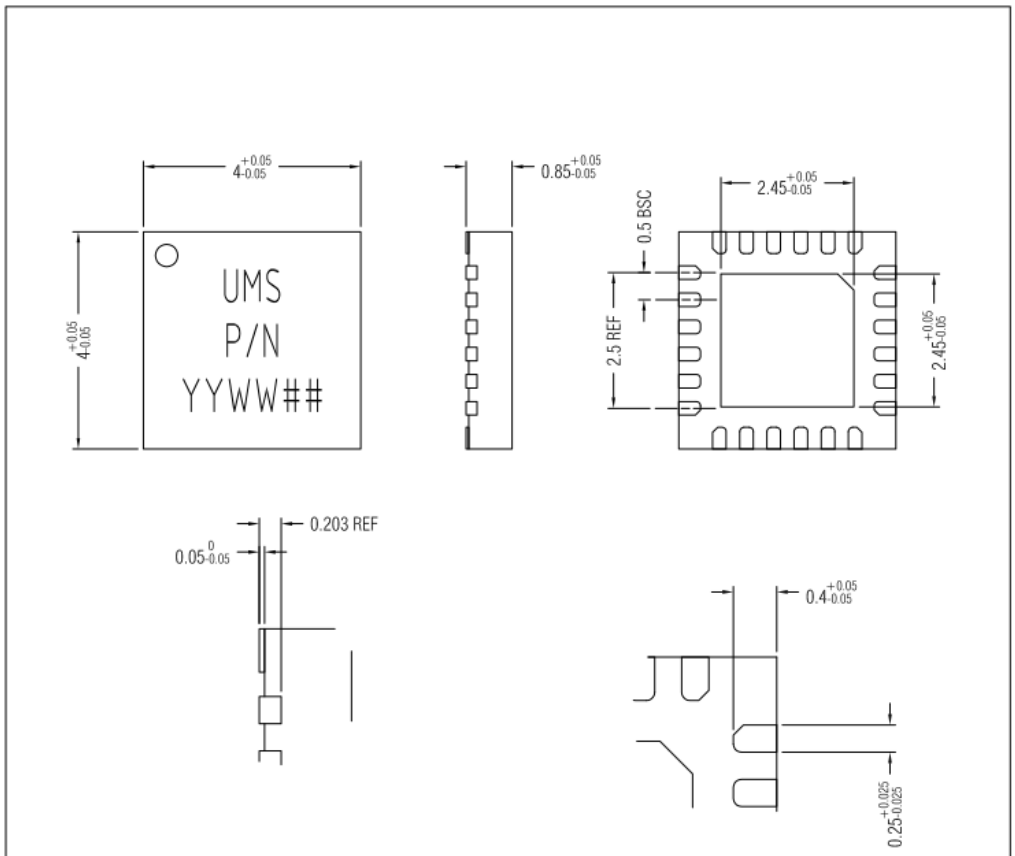
6.4. QFN 4x4, 24 leads (QDG) 2RF fused Leads



Units : mm
From the standard : JEDEC MO-220
Matt tin, lead free (Green)

1- Free	9- Free	17- GND	25- Gnd
2- GND	10- Free	18- Free	
3- GND	11- Free	19- Free	
4- RF PIN	12- Free	20- Free	
5- GND	13- GND	21- Free	
6- GND	14- GND	22- Free	
7- Free	15- RF PIN	23- Free	
8- Free	16- GND	24- Free	

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OUTLINE

UMS Designation: QDG Package
QFN Type: 24L QFN 4 X4 Fused 2RF
Scale: 10:1
Unit: mm Projection:

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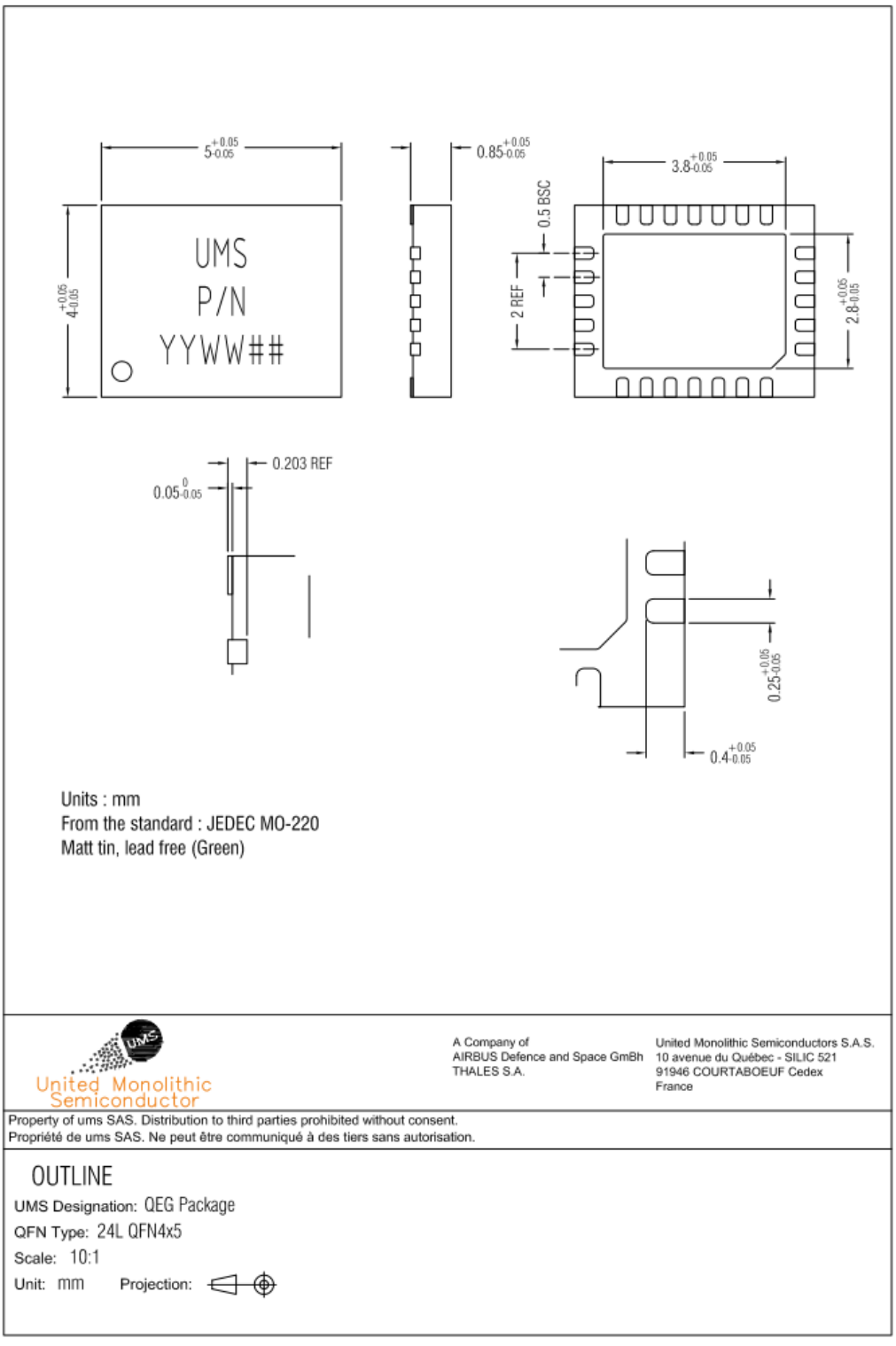
6.5. QFN 4x5, 24 leads (QEG)



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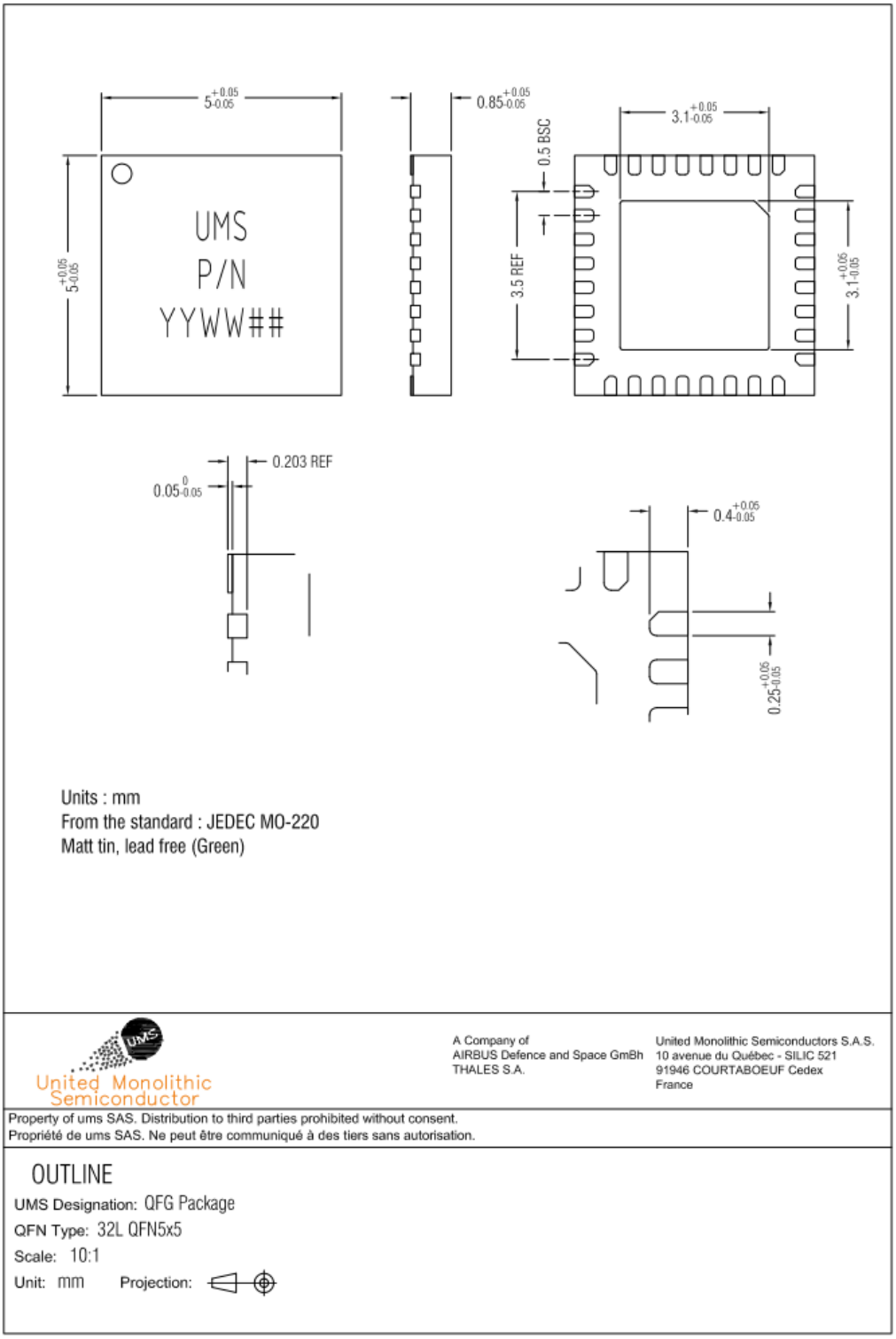
6.6. QFN 5x5, 32 leads (QFG)



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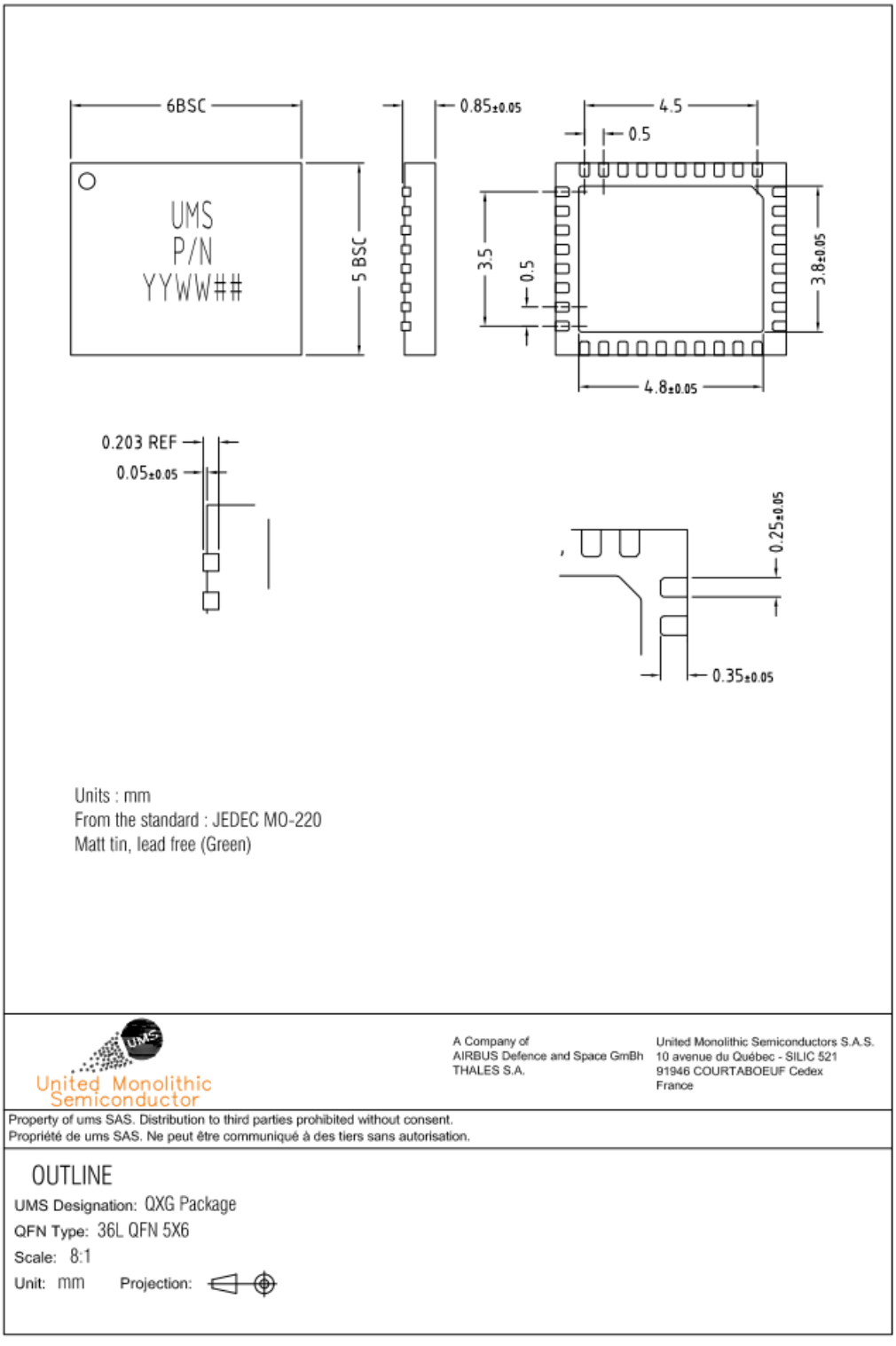
6.7. QFN 5x6, 36 leads (QXG)



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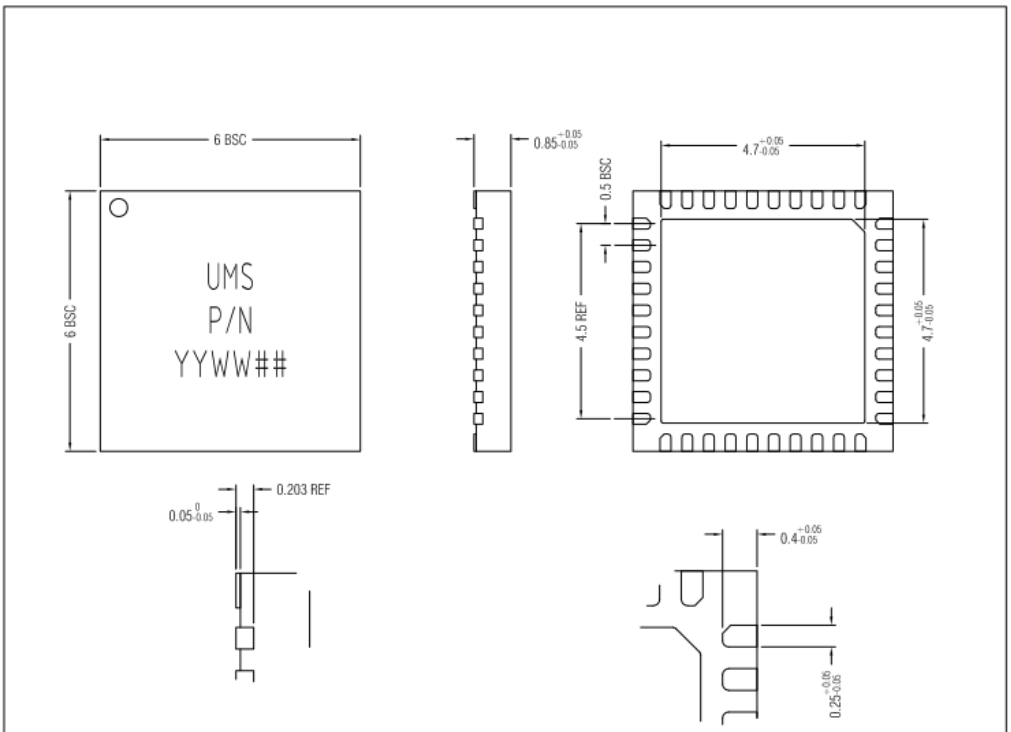
6.8. QFN 6x6, 40 leads (QJG)



Units : mm
From the standard : JEDEC MO-220
Matt tin, lead free (Green)

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OUTLINE

UMS Designation: QJG Package
QFN Type: 40L QFN6x6
Scale: 8:1
Unit: mm Projection:

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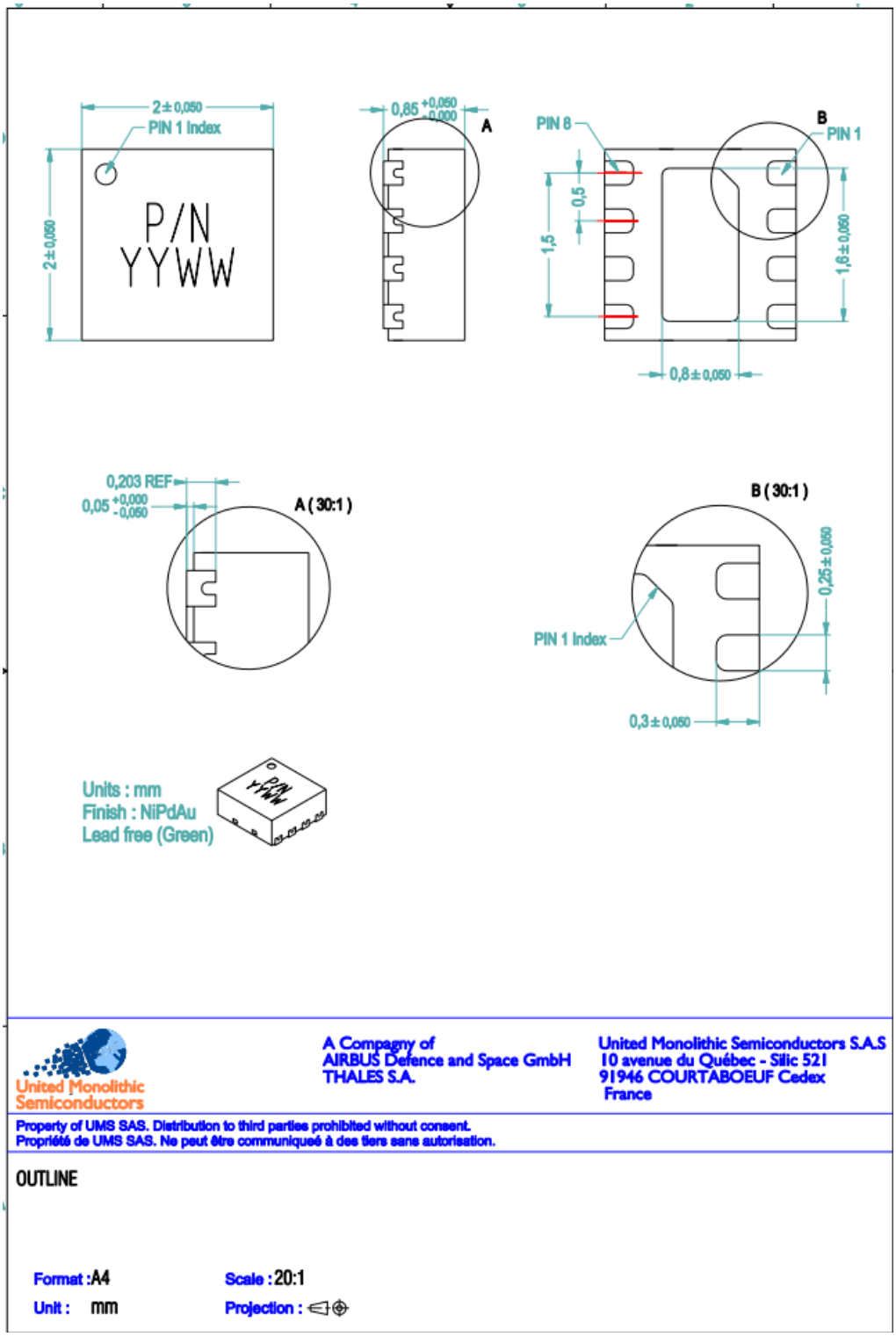
6.9. DFN 2x2, 8 leads (QKA)



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Glossary

SMD :	Surface Mount Device
SMT :	Surface Mount Techniques
DFN :	Dual Flat Non-leaded
QFN :	Quad Flat Non-leaded
PCB :	Printed Circuit Board
BOM :	Bill Of Materials
Sij :	Scattering Parameters
RoHS :	Restriction of the use of certain Hazardous Substances
Lead-free :	Part of the RoHS directive
DI :	Deionised water
MMIC :	Monolithic Microwave Integrated Circuit
THB :	Temperature and Humidity Biased
HOTL :	High Temperature Operating Life
Pb :	Lead
MSL :	Moisture Sensitivity Level
CPW:	Coplanar wave guide

7. References

[1] : JEDEC MO-220. Thermally enhanced plastic very thin and very very thin fin pitch quad flat no lead package.

[2] : IPC/JEDEC J-STD-020E. Moisture/reflow sensitivity classification for non hermetic solid-state surface-mount devices.

[3] : IPC/JEDEC J-STD-033D. Handling, packing shipping and use of moisture/reflow sensitive surface mount devices.

[4] : JEDEC JESD47I. Stress-test-driven qualification of integrated circuits.

[5] : EIA STANDARD – 481C. Taping of SMD.

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Bât. Charmille - Parc SILIC - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34 - www.ums-rf.com

Notes:

Contacts:

Web site: www.ums-rf.com
email: mktsales@ums-rf.com
Phone: 33 (1) 69 86 32 00 (France)
1 781 791 5078 (USA)
65 9298 8316 (Asia)

United Monolithic Semiconductors S.A.S.
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