

## X-band High Power Amplifier

### GaAs Monolithic Microwave IC

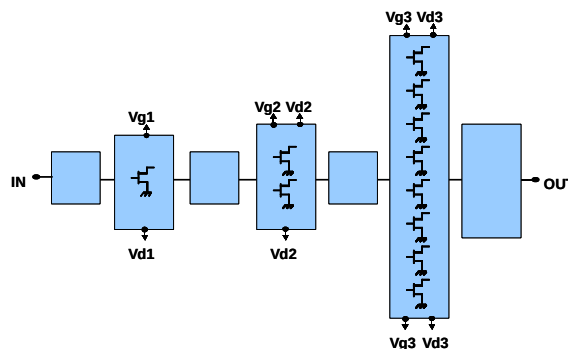
#### Description

The CHA7115-99F is a monolithic three-stage GaAs high power amplifier designed for X-band applications.

The HPA provides typically 8W output power associated to 36% power added efficiency at 4dBcomp and a high robustness on mismatch load.

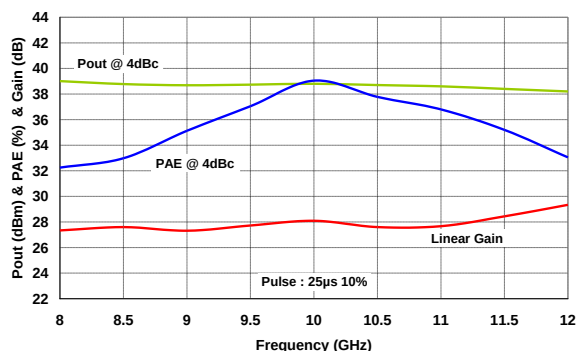
This device is manufactured using 0.25μm Power pHEMT process, including, via holes through the substrate and air bridges.

It is available in chip form.



#### Main Features

- 0.25μm Power pHEMT Technology
- Frequency band: 8.5 – 11.5GHz
- Output power : 39dBm @ 4dBcomp
- High linear gain: > 27dB
- High PAE : 37% @ 4dBcomp
- Quiescent bias point: Vd=8V, Id=2.2A
- Chip size: 4.59 x 3.31 x 0.07mm



#### Main Characteristics

Tamb.= +25°C

Vd = 8V, Id (Quiescent) = 2.2A, Drain Pulse width = 25μs, Duty cycle = 10%

| Symbol  | Parameter                              | Min | Typ  | Max  | Unit |
|---------|----------------------------------------|-----|------|------|------|
| Fop     | Operating frequency range              | 8.5 |      | 11.5 | GHz  |
| PAE_4dB | Power added efficiency @4dBcomp @ 20°C |     | 37   |      | %    |
| P_4dB   | Output power @ 4dBcomp @ 20°C          |     | 39   |      | dBm  |
| G       | Small signal gain @ 20°C               |     | 27.5 |      | dB   |

ESD Protections: Electrostatic discharge sensitive device. Observe handling precautions!

**Electrical Characteristics on wafer**

Tamb = 20°C, Vd = 8V, Id (Quiescent) = 2.2A, Drain Pulse width = 25µs, Duty cycle = 10%

| Symbol        | Parameter                        | Min | Typ  | Max  | Unit |
|---------------|----------------------------------|-----|------|------|------|
| Fop           | Operating frequency              | 8.5 |      | 11.5 | GHz  |
| G             | Small signal gain                |     | 27.5 |      | dB   |
| RLin          | Input Return Loss                |     | 10   |      | dB   |
| RLout         | Output Return Loss               |     | 12   |      | dB   |
| P_4dBc        | Output power @ 4dBcomp (2)       |     | 39   |      | dBm  |
| PAE_4dB       | Power Added Efficiency @ 4dBcomp |     | 37   |      | %    |
| Id_4dB        | Supply drain current @ 4dBcomp   |     | 2.6  |      | A    |
| Vd1, Vd2, Vd3 | Drain supply voltage (2)         |     | 8    |      | V    |
| Id            | Supply quiescent current (1)     |     | 2.2  |      | A    |
| Vg            | Gate supply voltage              |     | -1.4 |      | V    |

- (1) Parameter can be adjusted by tuning of Vg.
- (2) 0.5V variation on Vd leads to around 0.4dB variation of the output power (impact on robustness see Maximum ratings).

**Absolute Maximum Ratings (1)**

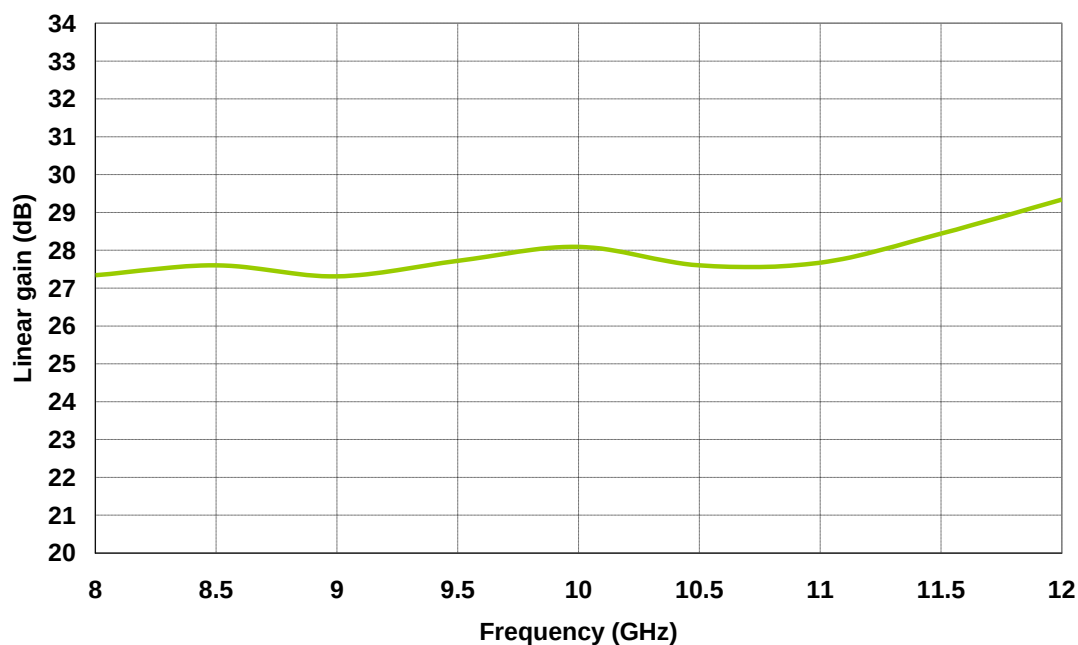
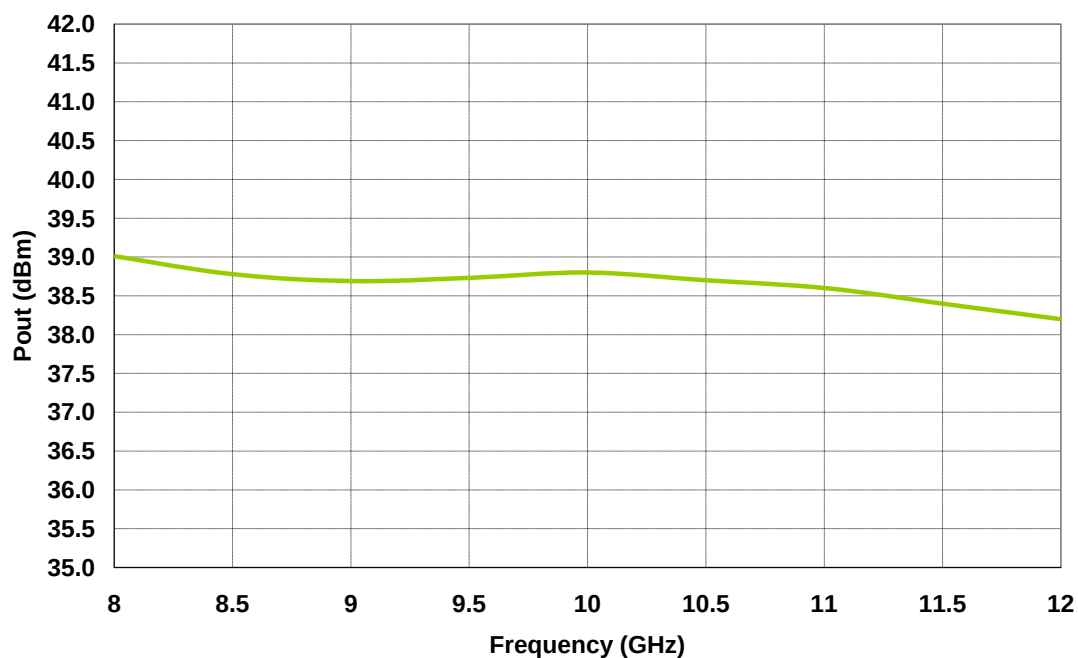
Tamb = 20°C

| Symbol | Parameter                    | Values      | Unit |
|--------|------------------------------|-------------|------|
| Cmp    | Compression level (2)        | 6           | dB   |
| Vd     | Supply voltage (3)           | 10          | V    |
| Id     | Supply quiescent current     | 2.8         | A    |
| Id_sat | Supply current in saturation | 4           | A    |
| Vg     | Supply voltage               | -0.8        | V    |
| Tj     | Maximum junction temperature | 175         | °C   |
| Tstg   | Storage temperature range    | -55 to +150 | °C   |
| Top    | Operating temperature range  | -40 to +80  | °C   |

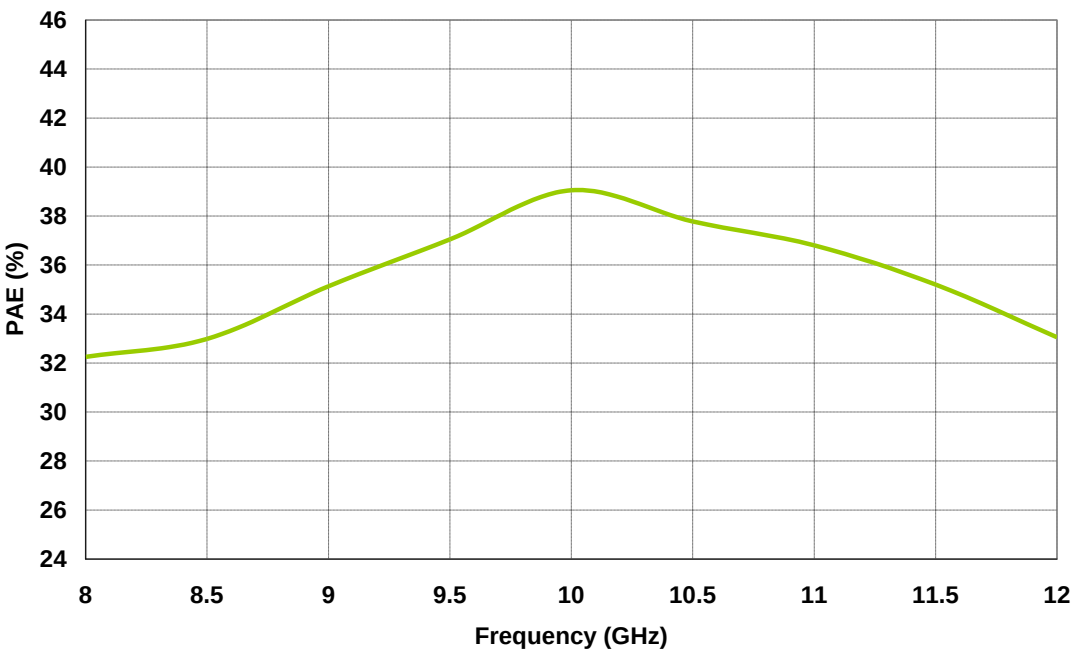
- (1) Operation of this device above anyone of these parameters may cause permanent damage.
- (2) For higher compression the level limit can be increased by decreasing the voltage Vd using the rate 0.5V/dBc.
- (3) Without RF input power.

**Typical measured characteristics****Measurements on Wafer:**

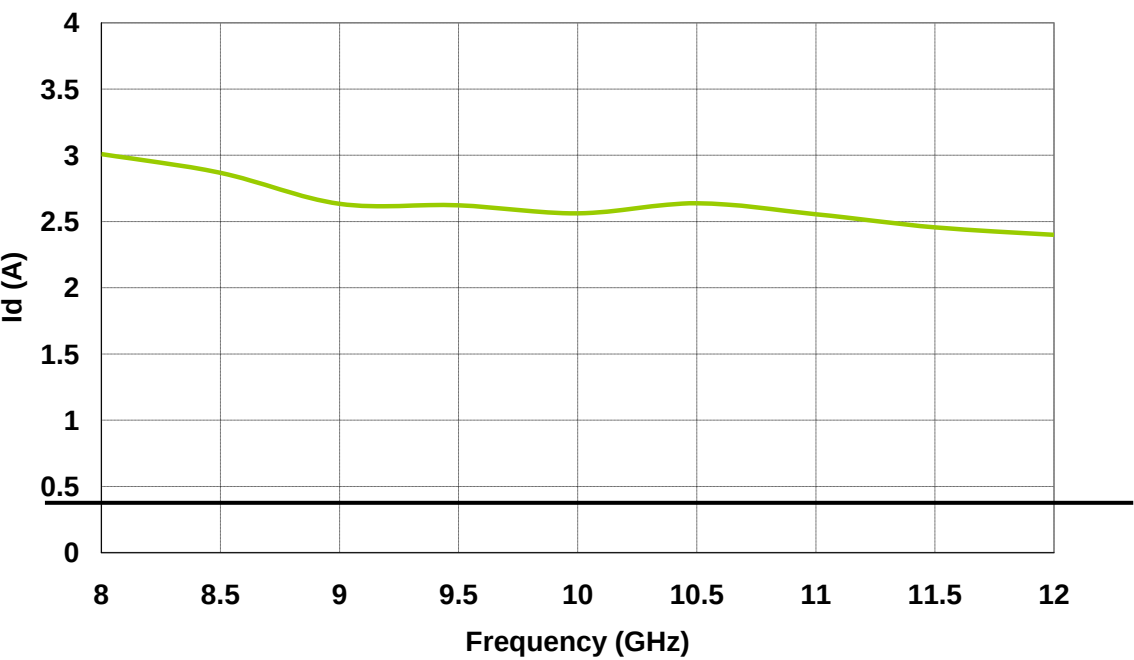
Vd = 8V, Id (Quiescent) = 2.2A, Drain Pulse width = 25μs, Duty cycle = 10%

***Linear gain versus frequency******Output Power @ 4dBcomp versus frequency***

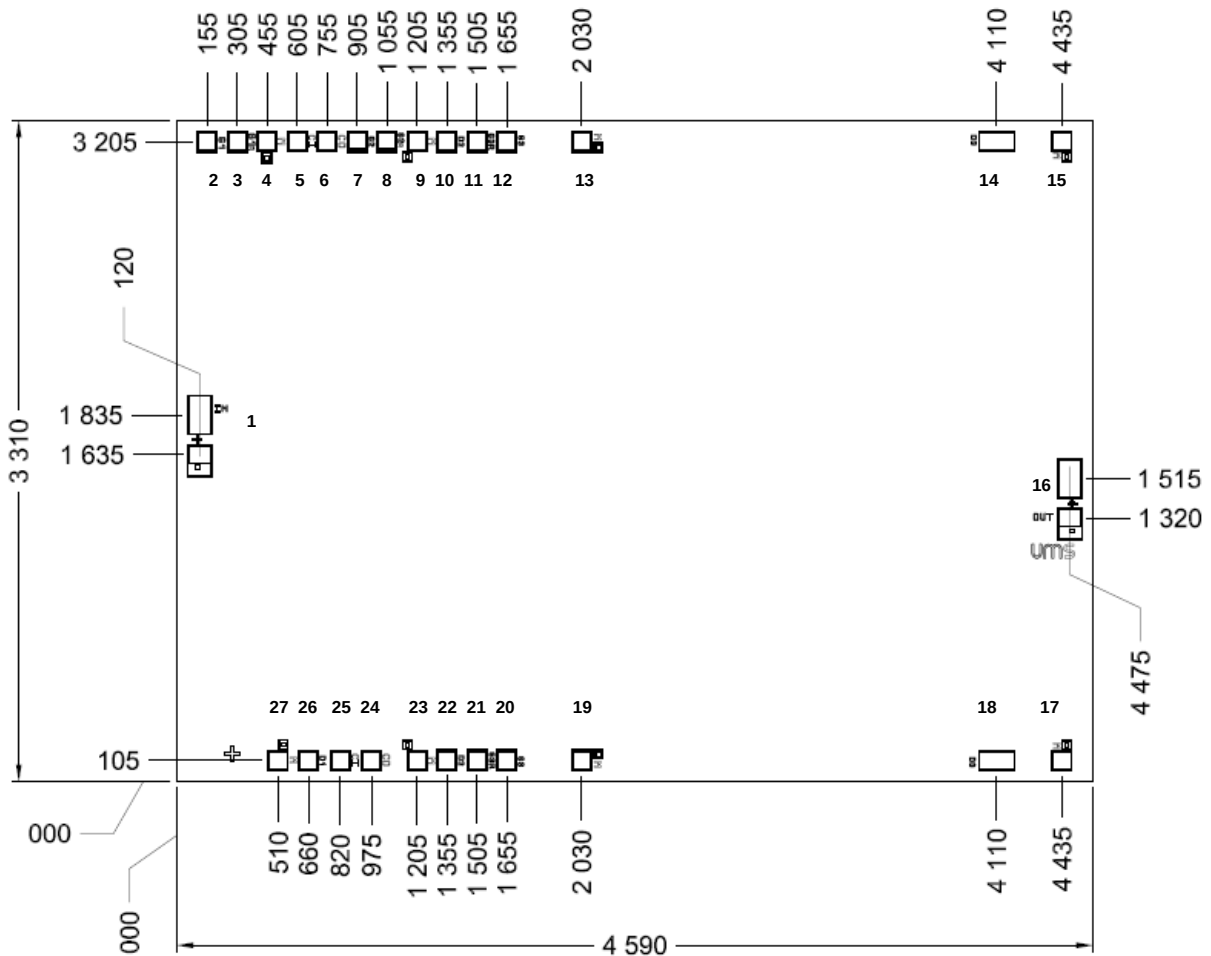
Power added efficiency @ 4dBcomp versus frequency



Drain Current @ 4dBcomp versus frequency



## Chip Mechanical Data and Pin references



Cotation :  $\mu\text{m}$   
Tolerance :  $\pm 35\mu\text{m}$

Chip width and length are given with a tolerance of  $\pm 35\mu\text{m}$

Chip thickness =  $70\mu\text{m} \pm 10\mu\text{m}$

RF pads (1, 16) =  $118 \times 196\mu\text{m}^2$

DC pads wide (14, 18) =  $186 \times 100\mu\text{m}^2$

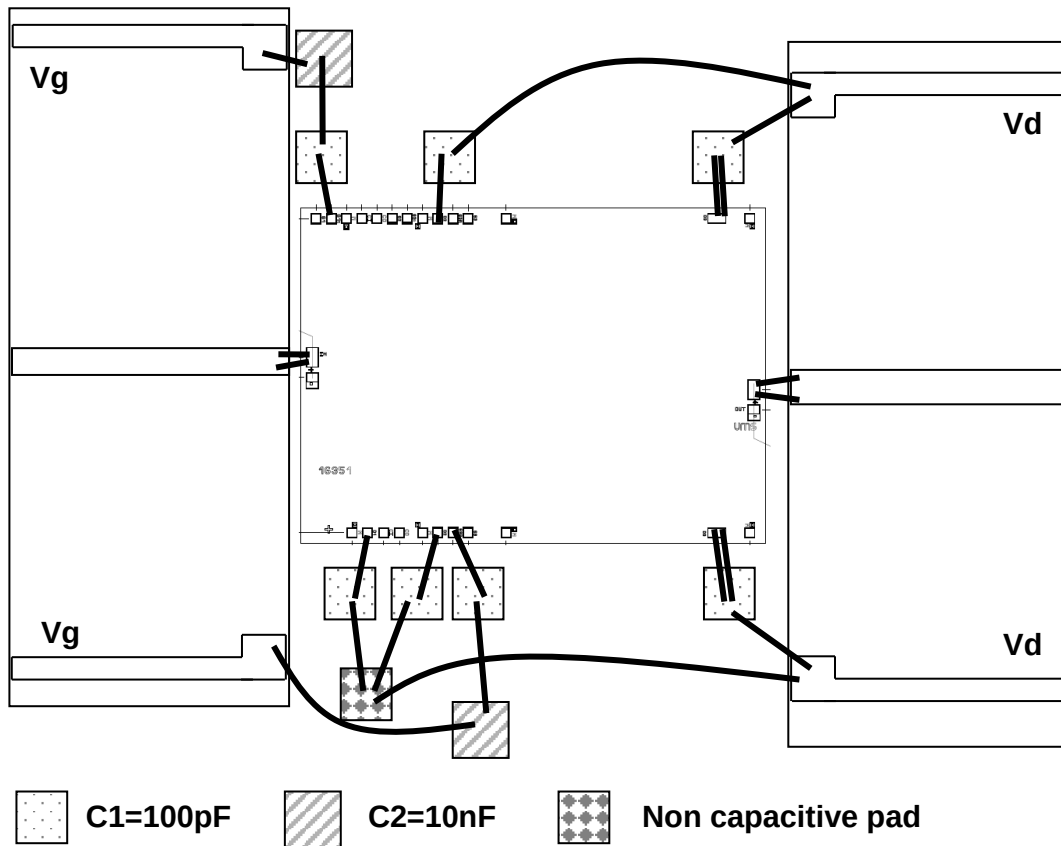
DC pads (others, 2 to 27) =  $100 \times 100\mu\text{m}^2$

| Pin number                        | Pin name | Description          |
|-----------------------------------|----------|----------------------|
| 1                                 | IN       | Input RF             |
| 2, 5, 6, 7, 8, 11, 12, 20, 24, 25 | G        | NC                   |
| 3, 21                             | GR       | Gate supply voltage  |
| 4, 9, 13, 15, 17, 19, 23, 27      | GND      | Ground (NC)          |
| 10, 14, 18, 22, 26                | VD       | Drain supply voltage |
| 16                                | OUT      | Output RF            |

## Bonding recommendations

| Port | Connection                                                                                                | External capacitor    |
|------|-----------------------------------------------------------------------------------------------------------|-----------------------|
| IN   | Inductance ( $L_{\text{bonding}}$ ) = 0.3nH<br>2 gold wires with diameter of 25 $\mu$ m (550 $\mu$ m max) |                       |
| OUT  | Inductance ( $L_{\text{bonding}}$ ) = 0.3nH<br>2 gold wires with diameter of 25 $\mu$ m (550 $\mu$ m max) |                       |
| Vg   | Inductance $\leq$ 1nH                                                                                     | C1 ~ 100pF, C2 ~ 10nF |
| Vd   | Inductance $\leq$ 1nH                                                                                     | C1 ~ 100pF            |

## Assembly recommendations in test fixture



## Ordering Information

Chip form : CHA7115-99F/00

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