United Monolithic Semiconductors

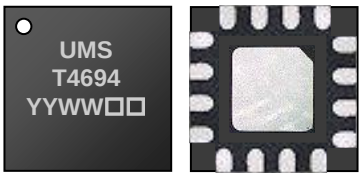
CHT4694-QAG

25-40GHz ATTENUATOR

GaAs Monolithic Microwave IC in SMD leadless package

Description

The CHT4694-QAG is a variable 25-40GHz attenuator designed for a wide range of applications, from military to commercial communication systems.
The circuit is manufactured with a MESFET process, 0.7µm gate length, via holes through the substrate and air bridges.

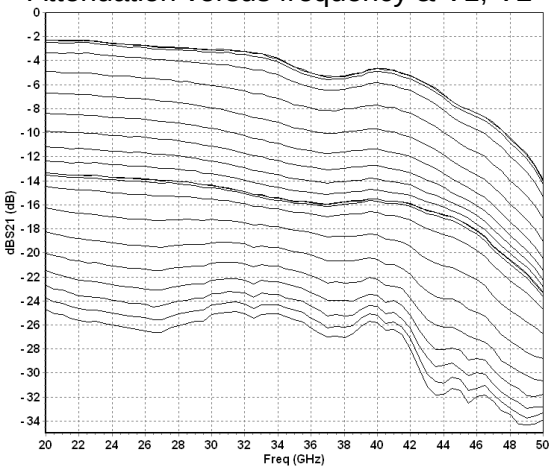


It is supplied in lead-free package.

Main Features

- Broadband performance: 25-40GHz
- 22dBm typical input 1dB compression point (any attenuation)
- 22dB dynamic range
- DC bias: -5V<V1<0V; -5V<V2<0V
- Single bias with V1=V2
- Package type: 16L-QFN3x3
- MSL 1

Attenuation versus frequency & V1, V2



Main Characteristics

Tamb = +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Fin	Input frequency range	25		40	GHz
Min Att.	|S21| (V1=-5V;V2=-5V)		4		dB
Max Att.	|S21| (V1=0V;V2=0V)		26		dB
Pin1dB	Input 1dB compression point (any attenuation)	20	22		dBm

ESD Protections: Electrostatic discharge sensitive device observe handling precautions!

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Electrical Characteristics

Tamb = +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Fin	Input frequency range	25		40	GHz
Min Att.	|S21| (V1=-5V;V2=-5V) (25 to 34GHz) |S21| (V1=-5V;V2=-5V) (34 to 40GHz)		4 5	6 6.5	dB dB
Max Att.	|S21| (V1=0V;V2=0V)	23	26		dB
RLin	Input return loss (any Att) (25 to 34GHz) Input return loss (any Att) (34 to 40GHz)		-10 -8	-8 -7	dB dB
RLout	Output return loss (any Att)		-6	-3.5	dB
Pin1dB	Input 1dB compression point (any Att)	20	22		dBm
I IP3	Input 3rd order Intercept Point (any Att) (Pin DCL > 0dBm)	25	30		dBm
V1,V2	Voltage control range	-5		0	V

These values are representative of onboard measurements as defined on the drawing in paragraph "Evaluation mother board".

Absolute Maximum Ratings (1)

Tamb = +25°C

Symbol	Parameter	Values	Unit
V1	V1 control voltage	-6V to +0.6V	V
V2	V2 control voltage	-6V to +0.6V	V
Pin	RF input power	30	dBm
Ta	Operating temperature range (reference on ground paddle)	-40 to +95	°C
Tstg	Storage temperature range	-55 to +155	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.

Typical Bias Conditions

Tamb = +25°C

Symbol	Pin No.	Parameter	Values	Unit
V1	6	V1 control voltage	-5 to 0	V
V2	7	V2 control voltage	-5 to 0	V

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Typical Package Sij parameters

Tamb = +25°C, V1 = -5V & V2= -5V – Minimum attenuation

Freq (GHz)	dB(S11)	P(S11) (°)	dB(S12)	P(S12) (°)	dB(S21)	P(S21) (°)	dB(S22)	P(S22) (°)
20	-13,5	132	-2,3	-95,7	-2,3	-95,7	-13,1	-139,3
21	-15,4	106,1	-2,3	-120,3	-2,3	-120,2	-13,6	-155,6
22	-19,2	71,9	-2,3	-145,2	-2,3	-145,3	-14,5	-165,4
23	-22,5	-4,7	-2,4	-171,4	-2,3	-171,5	-15	-164,7
24	-19,1	-81,9	-2,5	163,5	-2,5	163,5	-13,9	-166,1
25	-15,3	-121,3	-2,7	138,4	-2,7	138,4	-12,5	-172
26	-13,2	-151,2	-2,7	113,1	-2,7	113,2	-11,3	177,1
27	-11,9	-177,4	-2,9	88	-2,9	88	-10,9	164,4
28	-11,6	154,7	-2,9	63	-2,9	63	-11	152,4
29	-12,3	129	-3	37,3	-3	37,6	-11,6	141,3
30	-13,6	102,2	-3,1	12,2	-3,1	12,2	-12,8	131,6
31	-17	79,1	-3,1	-13,8	-3,1	-13,5	-14,4	127,4
32	-24	84,5	-3,2	-40,4	-3,2	-40,3	-16,2	135,3
33	-22,3	149,9	-3,4	-67,1	-3,4	-67	-14,6	153,5
34	-14,1	138,3	-3,8	-94,5	-3,8	-94,5	-11,2	152,8
35	-10,8	113,7	-4,5	-120,4	-4,5	-120,4	-9	137,7
36	-9,2	91,2	-5	-144,2	-5	-144,2	-7,9	120,2
37	-8,7	70,5	-5,3	-167,3	-5,3	-167,6	-7,2	101,5
38	-9	52,8	-5,3	168,9	-5,3	168,6	-7,4	83,4
39	-10,2	38,6	-4,9	143,4	-5	143,4	-8,7	66,7
40	-12,8	23,3	-4,6	114,2	-4,6	114,2	-11,4	55,7
41	-21,3	26,3	-4,8	82,7	-4,8	82,9	-13,8	70,9
42	-17,3	121,6	-5,3	52	-5,3	51,9	-11,5	85,5
43	-9,8	112,7	-5,9	21,5	-6	21,5	-8,7	84,6
44	-6,7	98	-6,8	-7,9	-6,8	-7,6	-6,9	74,8
45	-5,2	82,5	-7,8	-34,9	-7,8	-35,2	-6,2	62,2
46	-4,8	71,7	-8,3	-62,1	-8,4	-62,1	-6,4	56,3
47	-4,7	65,2	-9,1	-92,6	-9,1	-92,7	-5,3	56,1
48	-4,3	60,6	-10,4	-122	-10,5	-122,1	-4,3	52,5
49	-4	55,7	-11,8	-150,2	-11,8	-150,1	-3,7	47,2
50	-3,7	51	-14	-180	-13,9	-180	-3	39,1

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Typical Package Sij parameters

Tamb = +25°C, V1 = 0V & V2= 0V – Maximum attenuation

Freq (GHz)	dB(S11)	P(S11) (°)	dB(S12)	P(S12) (°)	dB(S21)	P(S21) (°)	dB(S22)	P(S22) (°)
20	-11,4	-161,9	-24,7	-99,8	-24,7	-99,7	-4,3	-137,3
21	-11,3	-170,7	-25,2	-120,6	-25,1	-120,2	-4,2	-152,4
22	-11,3	-178,7	-25,7	-143,8	-25,6	-143,9	-4,1	-166,8
23	-11,2	173	-25,7	-166,9	-25,7	-167	-4,1	179,2
24	-11,1	164,3	-26	168,6	-26	168,7	-4,1	165,7
25	-11,1	154,7	-26,2	145	-26,3	145	-4,3	152,3
26	-11,2	143,6	-26,5	120,9	-26,5	120,6	-4,3	139
27	-11,3	132,6	-26,6	100,7	-26,6	100,5	-4,6	125,4
28	-11,4	120,3	-26	78,4	-26,1	78,2	-5	112,2
29	-11,4	107,4	-25,7	55,4	-25,7	55,6	-5,5	97,6
30	-11,4	94,2	-25,1	33,3	-25,2	33,2	-6,1	82,5
31	-11,5	82	-25	8	-24,9	8,6	-6,8	66,3
32	-11,5	70,7	-25	-16,5	-25,1	-16,4	-7,8	49,8
33	-11,6	57,1	-25,1	-36,6	-25,1	-36,7	-9	30,2
34	-11,6	45,8	-25,1	-61	-25,1	-61,1	-10,6	7,5
35	-11,8	33,7	-25,6	-84,8	-25,5	-84,8	-12,2	-19,2
36	-12,5	20,2	-26,2	-107,5	-26,3	-107,9	-13,5	-51,3
37	-13,7	5,7	-27,1	-126,2	-27	-127,1	-14,4	-90,2
38	-16,5	-14	-27	-147,8	-27,1	-147,9	-13,3	-130,7
39	-23,9	-51,2	-26,1	-170,8	-26,1	-170,9	-10,9	-163,8
40	-24,4	175,2	-25,8	152	-25,8	152,3	-8,9	168,9
41	-16,4	145,6	-26,3	116,6	-26,4	116,6	-7,4	144,3
42	-12	133,5	-27,9	72	-28	71,4	-6,1	124
43	-8,2	121,6	-31	43,1	-31,1	41,2	-5,1	109,5
44	-5,7	108,9	-31,8	22,2	-31,8	22,1	-4	96,4
45	-4,3	93,2	-31,6	-13,9	-31,5	-13,5	-3,3	82,8
46	-3,4	81,7	-32,1	-34,6	-32	-36,3	-2,6	70,8
47	-2,9	70,7	-32,4	-67,4	-32,3	-67,7	-1,8	59,7
48	-2,5	61,3	-33,4	-89,1	-33,4	-89	-1,5	49,3
49	-2,4	51,8	-34,5	-105,4	-34,3	-105,3	-1,6	40,8
50	-2,9	44,8	-33,8	-117,2	-33,9	-117,7	-1,8	30,7

The Sij measurement calibration planes are defined in the paragraph

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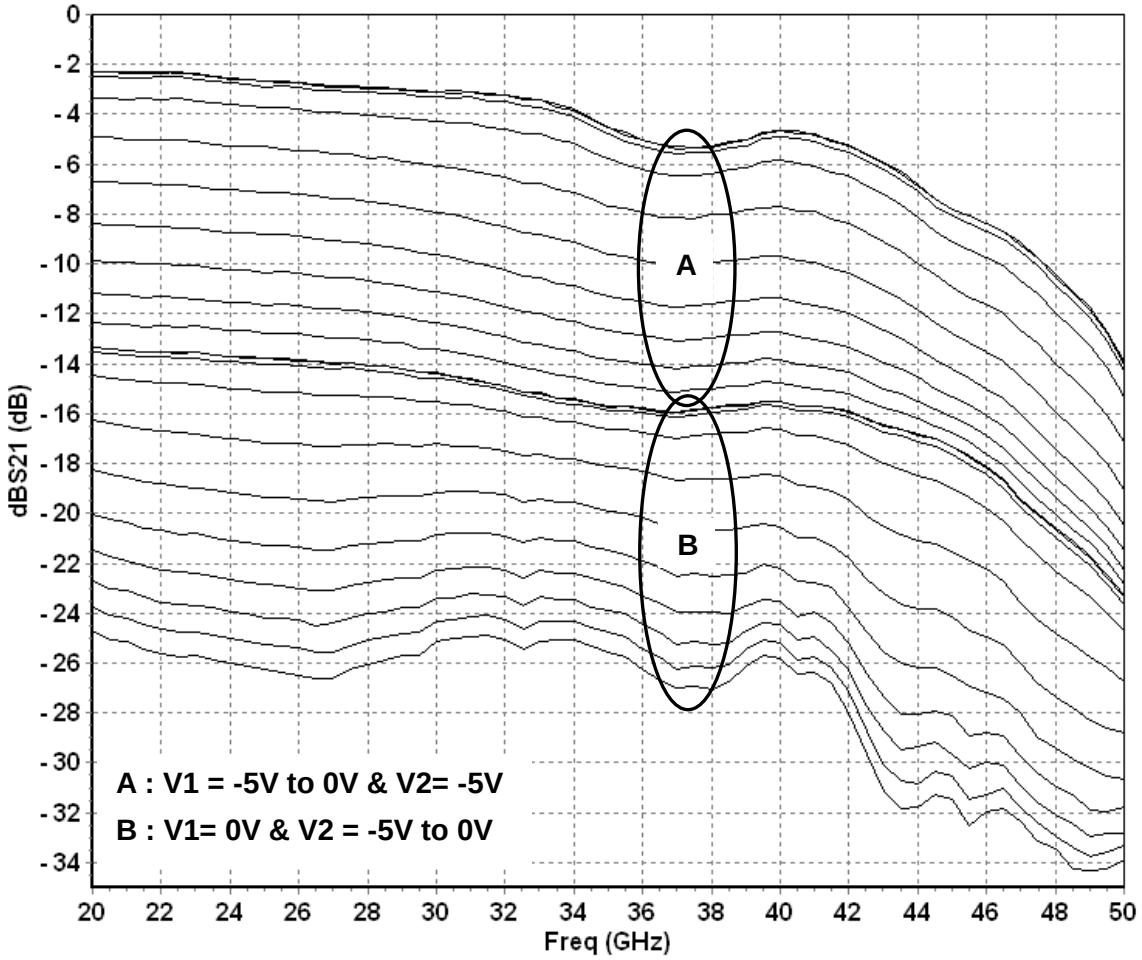
Typical Measured Performances

Tamb = +25°C
Measurements in the package access planes

Attenuation versus frequency
V1 = -5V to 0V & V2= -5V and after V1= 0V & V2 = -5V to 0V



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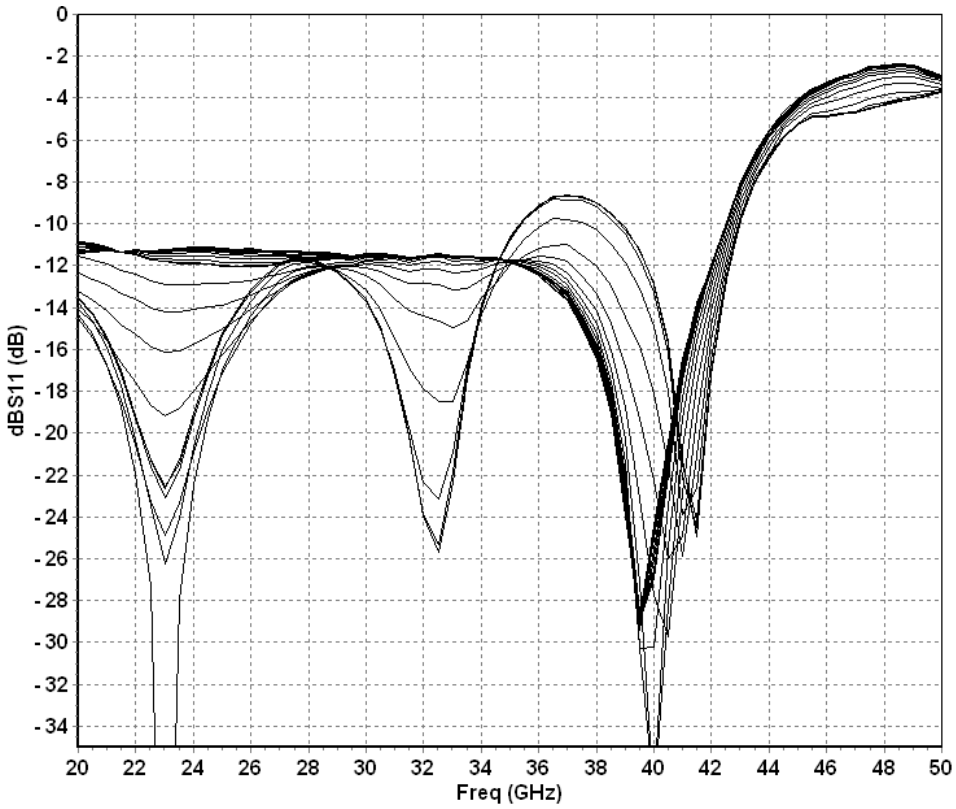
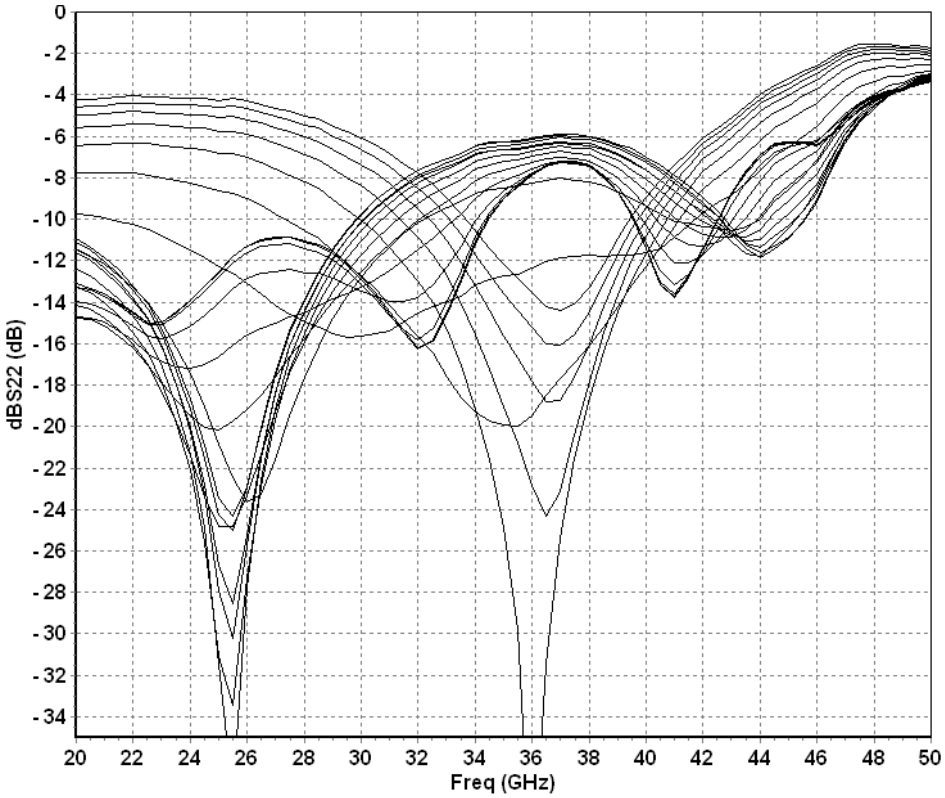
Input Return loss versus frequency in total attenuation range



Output Return loss versus frequency in total attenuation range



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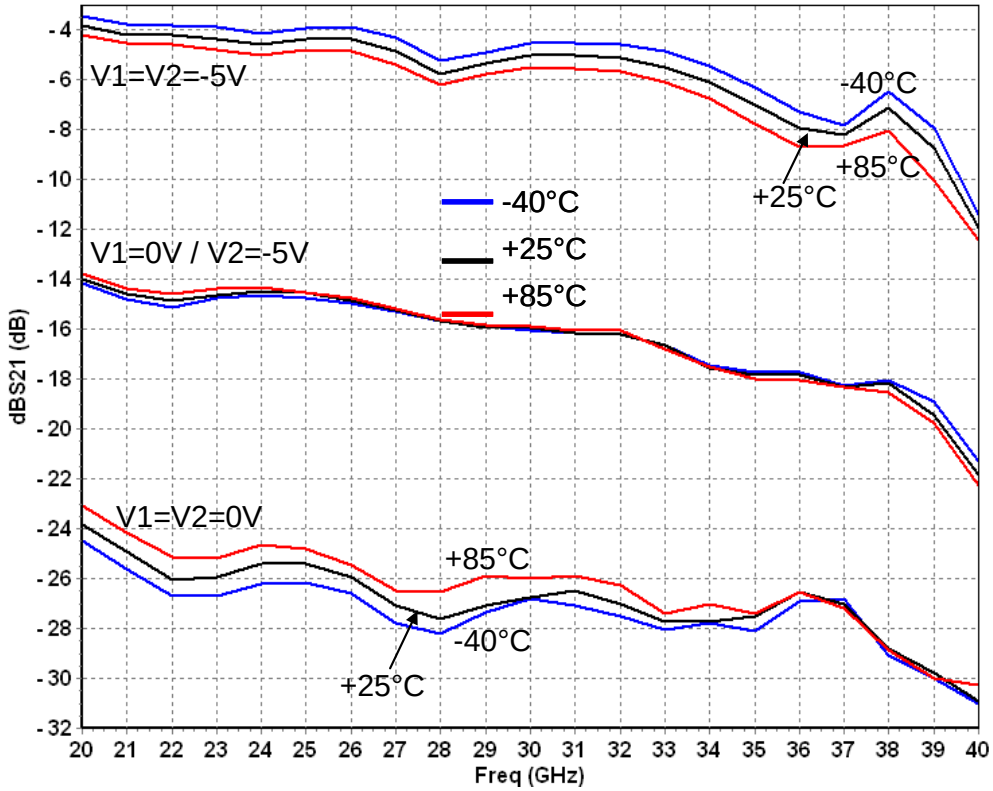
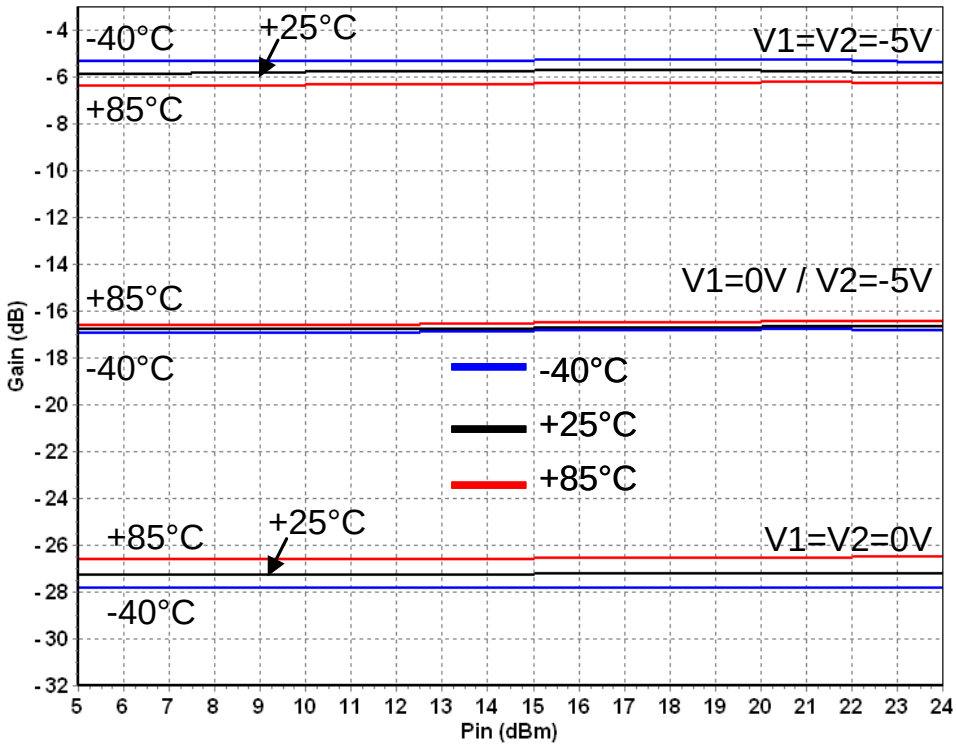
Attenuation versus temperature



Input P1dB versus temperature at 34GHz



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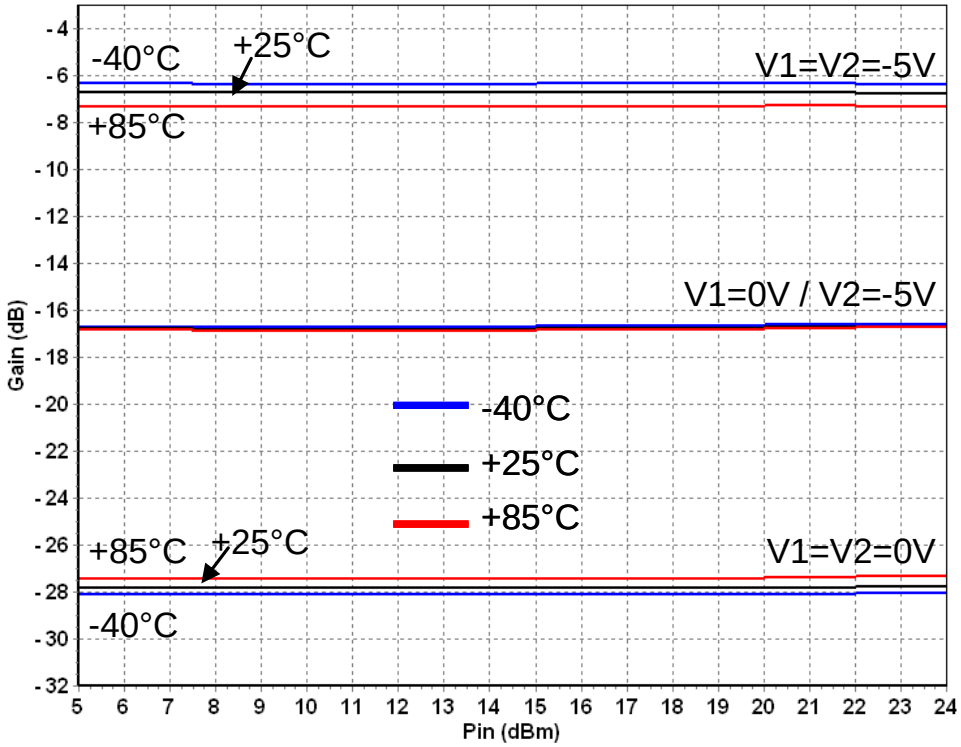
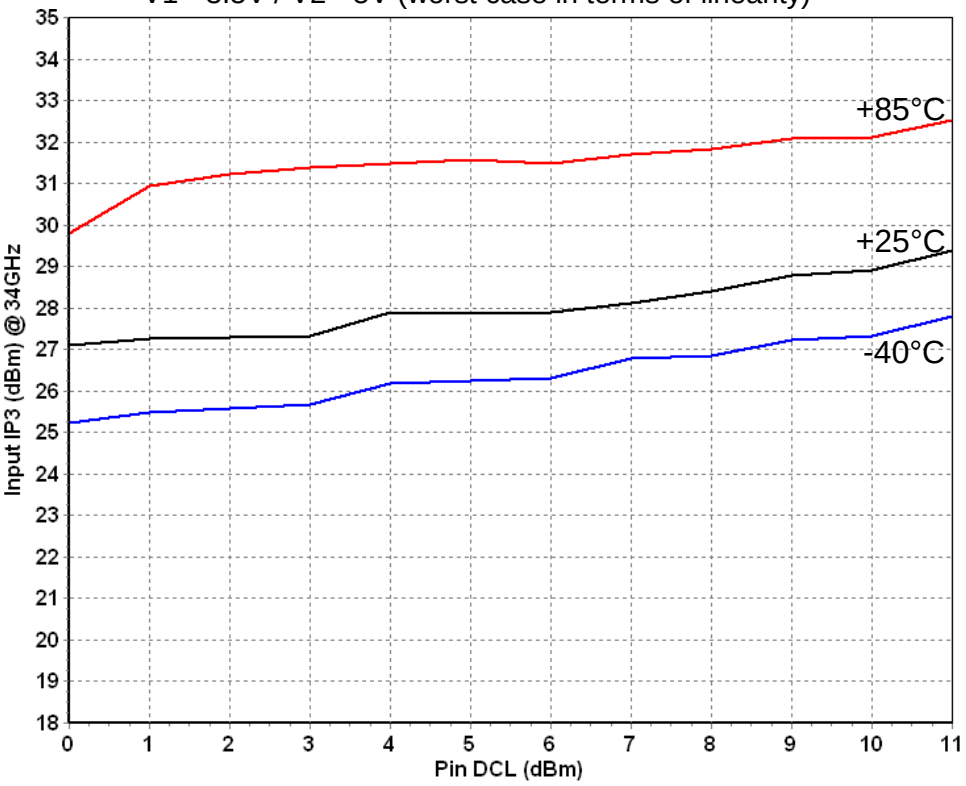
Input P1dB versus temperature at 40GHz



Input IP3 versus temperature at 34GHz

V1=-3.5V / V2=-5V (worst case in terms of linearity)



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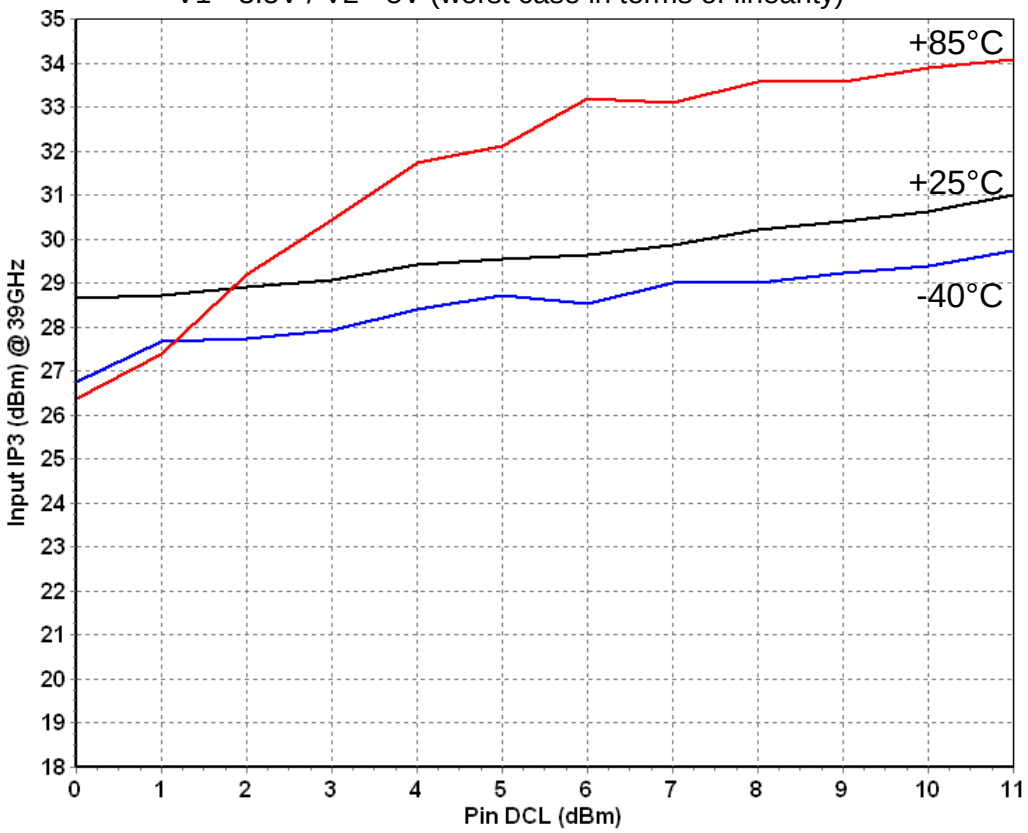
Input IP3 versus temperature at 39GHz
V1=-3.5V / V2=-5V (worst case in terms of linearity)



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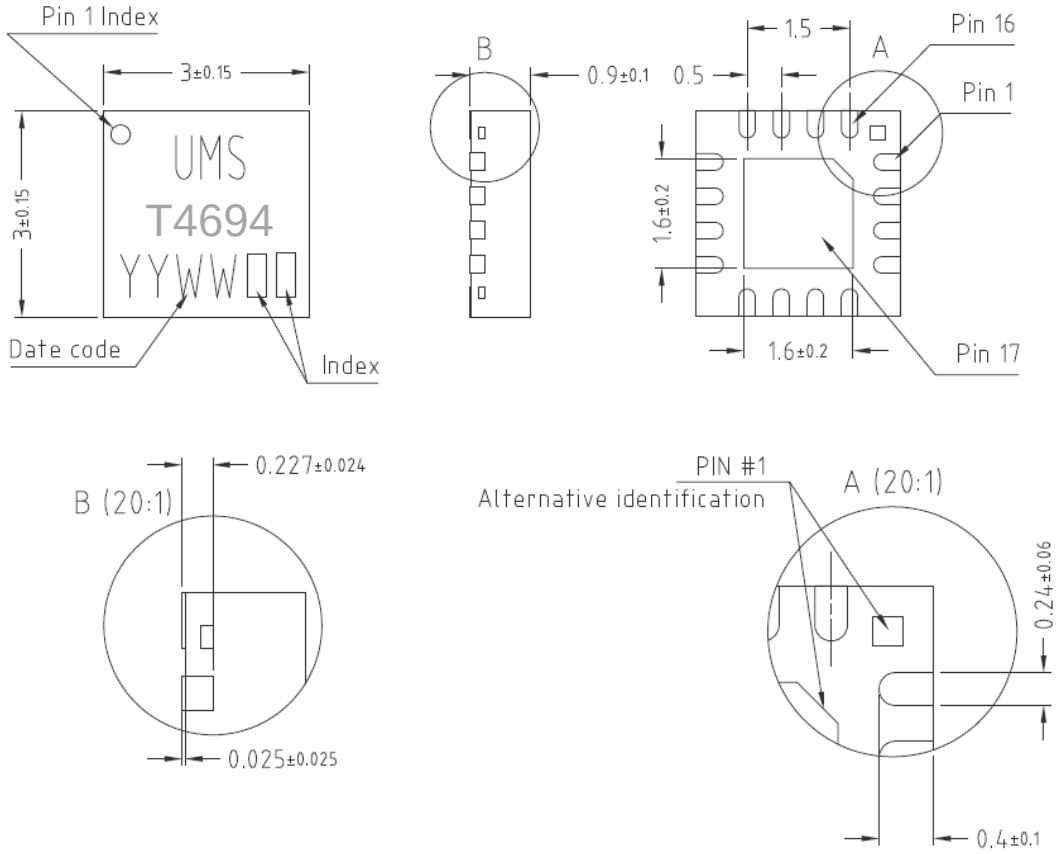
Package outline (1)



Matt tin, Lead Free	(Green)	1-	Gnd(2)	9-	Gnd(2)
Units	mm	2-	Gnd(2)	10-	RF Out
From the standard	JEDEC MO-220	3-	RF In	11-	Gnd(2)
	(VEED)	4-	Gnd(2)	12-	Gnd(2)
17- GND		5-	NC	13-	NC
		6-	V1	14-	NC
		7-	V2	15-	NC
		8-	NC	16-	NC

(1) The package outline drawing included to this data-sheet is given for indication. Refer to the application note AN0017 available at https://www.ums-rf.com for exact package dimensions.

(2) It is strongly recommended to ground the Gnd pins on the PCB board.

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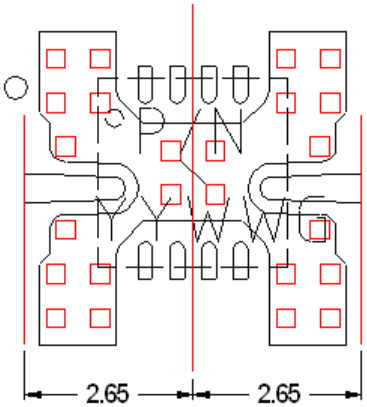
Definition of the Sij reference planes

The reference planes used for Sij measurements given above are symmetrical from the symmetrical axis of the package (see drawing beside). The input and output reference planes are located at 2.65mm offset (input wise and output wise respectively) from this axis. Then, the given Sij parameters incorporate the land pattern of the evaluation motherboard recommended at the page 13.



Recommended package footprint

Refer to the application note AN0017 available at https://www.ums-rf.com for package foot print recommendations.

SMD mounting procedure

The SMD leadless package has been designed for high volume surface mount PCB assembly process. The dimensions and footprint required for the PCB (motherboard) are given in the drawings above.

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

Recommended ESD management

Refer to the application note AN0020 available at https://www.ums-rf.com for ESD sensitivity and handling recommendations for the UMS package products.

Recommended environmental management

Refer to the application note AN0019 available at https://www.ums-rf.com for environmental data on UMS package products.

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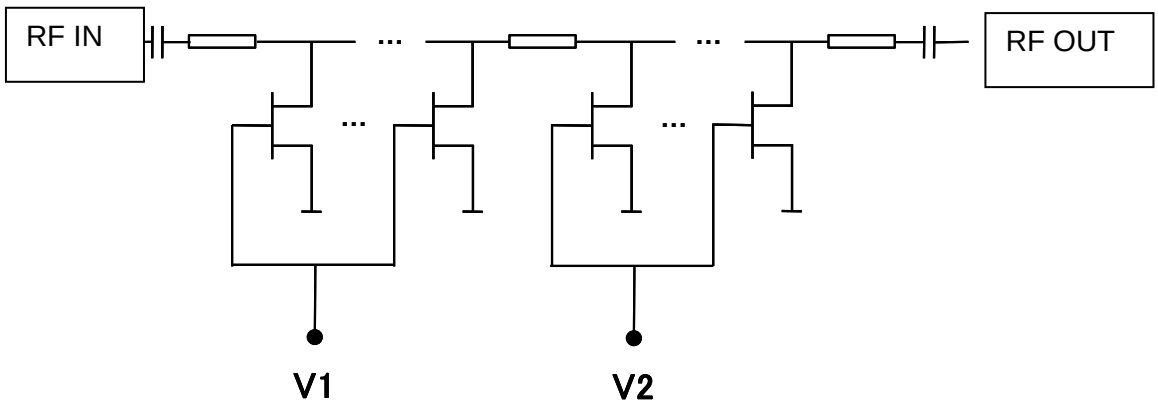
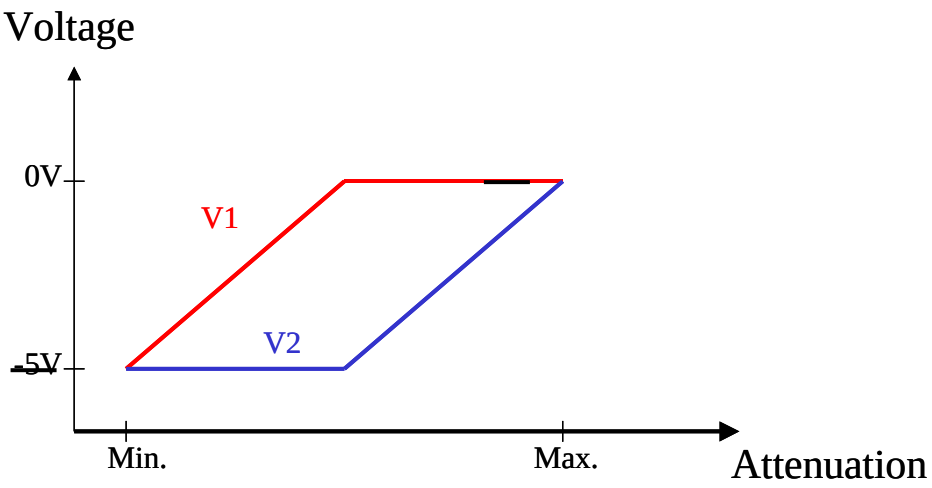
Packaged part biasing options

To obtain good performances in linearity, biasing voltage should be applied as following:

Control of 1st stage attenuation with V1 from –5V to 0V, with V2 fixed at -5V
Control of 2nd stage with V2 from –5V to 0V, with V1 fixed at 0V





This part could be also driven in Single Voltage Control, applying the same voltage from -5V to 0V on V1 and V2.

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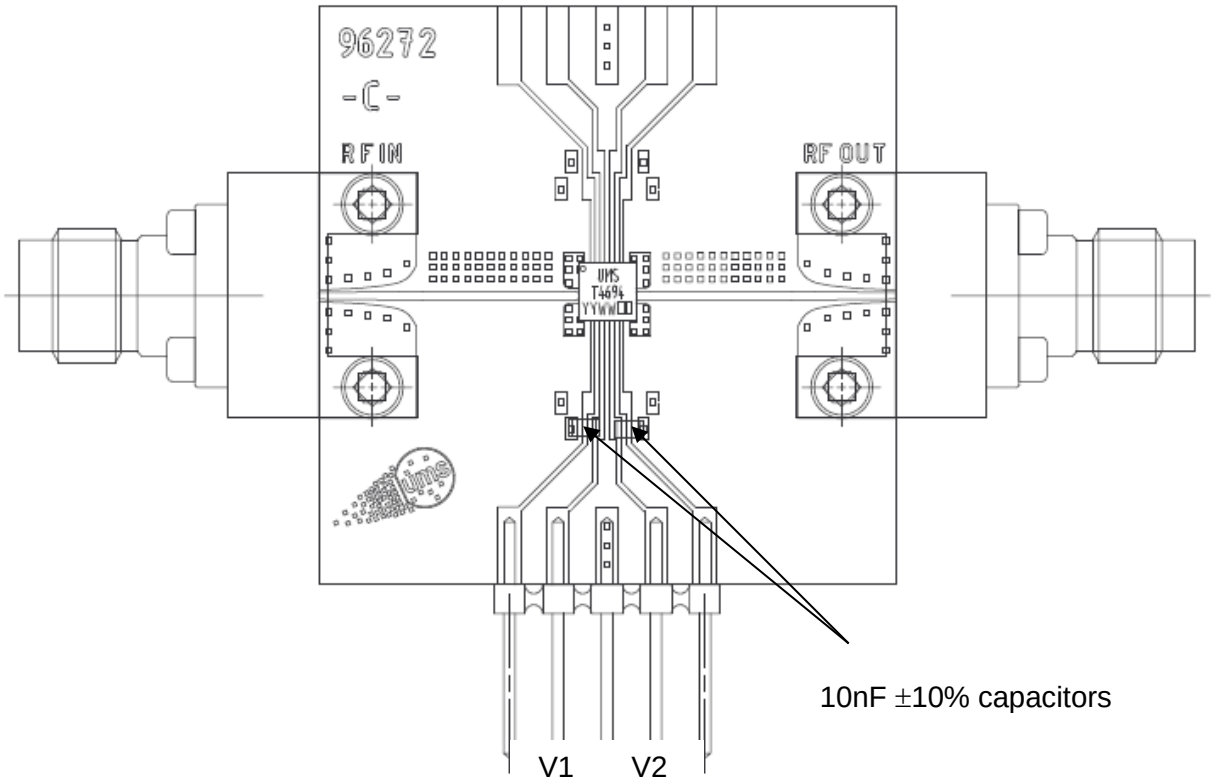
Evaluation mother board

- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a microstrip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 10nF ±10% are recommended for all DC accesses.
- (See application note AN0017 for details).



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Ordering Information

QFN 3x3 RoHS compliant package:	CHT4694-QAG/XY	
	Stick: XY = 20	Tape & reel: XY = 21

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