

9-18GHz Frequency Multiplier

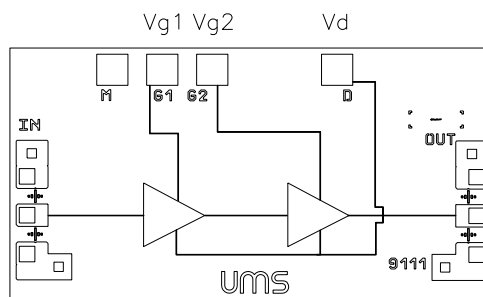
GaAs Monolithic Microwave IC

Description

The CHX2089-99F is a cascaded times 2 frequency multiplier monolithic circuit.

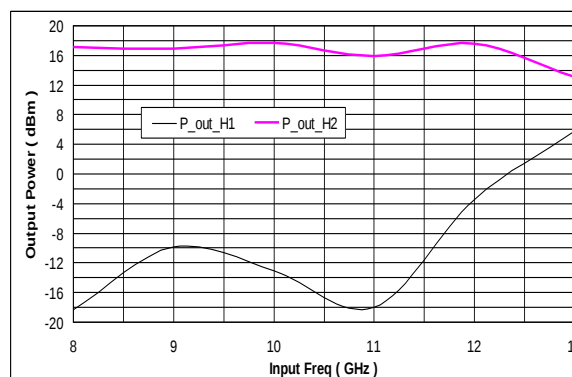
It is designed for a wide range of applications, from ISM to commercial communication systems. The backside of the chip is both RF and DC grounds. This helps simplify the assembly process.

The circuit is manufactured with a pHEMT process.



Main Features

- Broadband Frequency : 8-11.5 GHz
- Pout(H2) = 15dBm @ Pin = 12dBm
- DC bias: Vd = 3.5Volt @ Id = 60mA
- Chip size 1.62 x 0.89 x 0.10mm



Main Electrical Characteristics

T_{backside} = 25°C, Vd=3.5V

Symbol	Parameter	Min	Typ	Max	Unit
Fin	Input frequency range	8	9	11.5	GHz
Fout	Output frequency range	16	18	23	GHz
Pin	Input power		12	15	dBm
Pout	Output power for +12dBm input power	11	15		dBm

Electrical Characteristics

$T_{\text{backside}} = 25^{\circ}\text{C}$, $V_d = 3.5\text{V}$, $V_{g1} = -0.9\text{V}$, V_{g2} adjusted for $I_d = 50\text{ mA}$, no RF ($V_{g2}\text{ typ.} = -0.3\text{V}$).

Symbol	Parameter	Min	Typ	Max	Unit
F_{in}	Input frequency range	8	9	11.5	GHz
F_{out}	Output frequency range	16	18	23	GHz
P_{in}	Input power		12	15	dBm
P_{out}	Output power for +12dBm input power	11	15		dBm
I_s/F_o	F_{in} rejection at the output	15	20		dBc
VSWR _{in}	Input VSWR			2.0:1	
VSWR _{out}	Output VSWR			2.5:1	
I_d	Bias current without RF		50	70	mA
I_{d_RF}	Bias current with RF ($P_{in} = 12\text{ dBm}$)		60	85	mA

These values are representative of on-wafer measurements that are made without bonding wires at the RF ports.

Absolute Maximum Ratings ⁽¹⁾

$T_{\text{backside}} = 25^{\circ}\text{C}$

Symbol	Parameter	Values	Unit
V_d	Drain bias voltage	4.5	V
I_d	Drain bias current	90	mA
V_g	Gate bias voltage	-2 to +0.4	V
P_{in}	Input power	20	dBm
T_a	Operating temperature range	-40 to +85	$^{\circ}\text{C}$
T_{stg}	Storage temperature range	-55 to +150	$^{\circ}\text{C}$

⁽¹⁾ Operation of this device above any one of these parameters may cause permanent damage.

Typical Bias Conditions

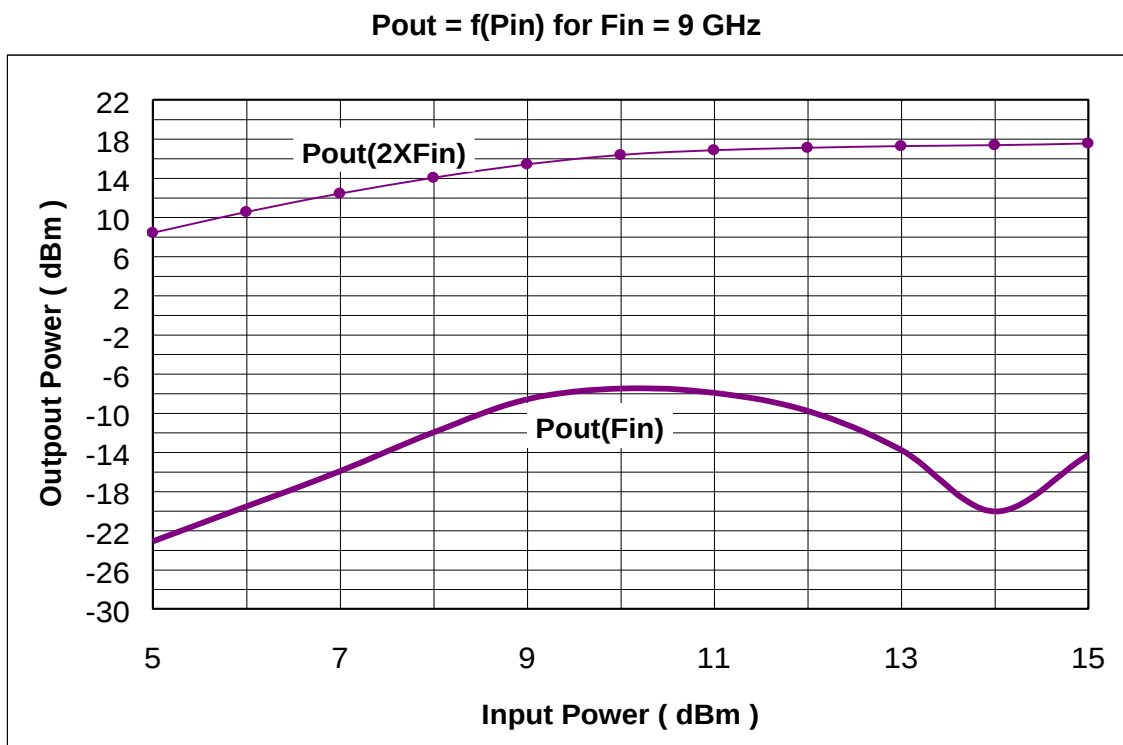
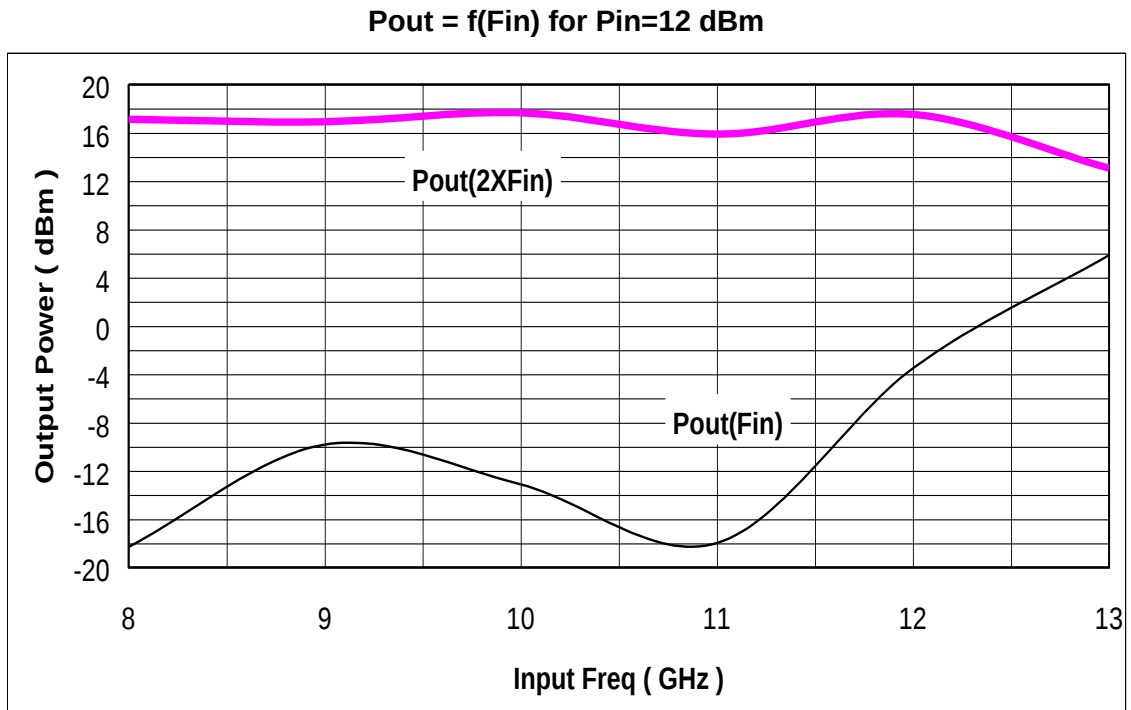
$T_{\text{backside}} = 25^{\circ}\text{C}$

Symbol	Pad N°	Parameter	Values	Unit
V_d	D	Positive Drain voltage	3.5	V
V_{g1}	G1	Negative multiplier stage gate voltage	-0.9	V
V_{g2}	G2	Negative buffer stage gate voltage	(-0.3)	V

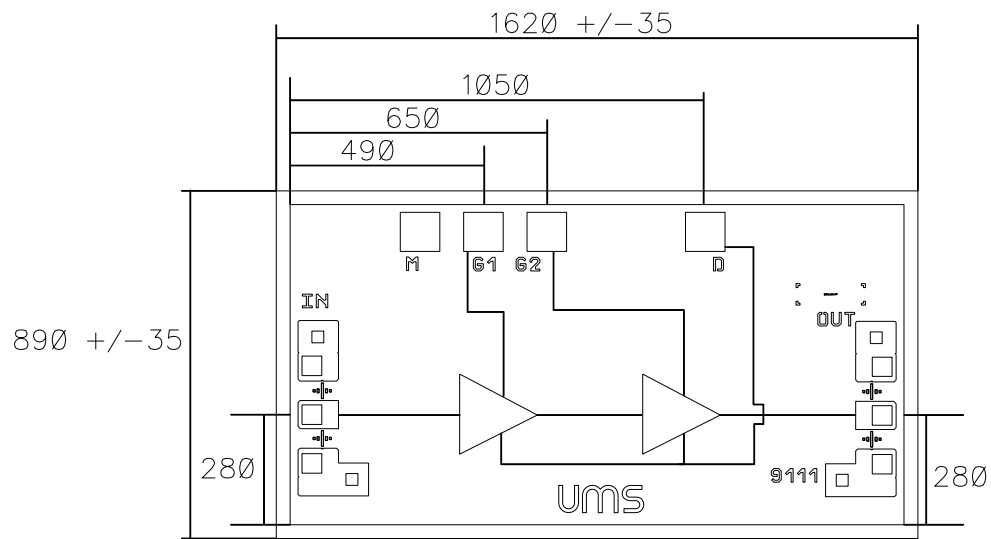
V_{g2} should be adjusted to achieve $I_{dq} = 50\text{mA}$ while no RF applied at the input.

Typical on wafer Measurements

$T_{\text{backside}} = 25^{\circ}\text{C}$, $V_d = 3.5\text{V}$, $V_{g1} = -0.9\text{V}$, $V_{g2} = -0.3\text{V}$.

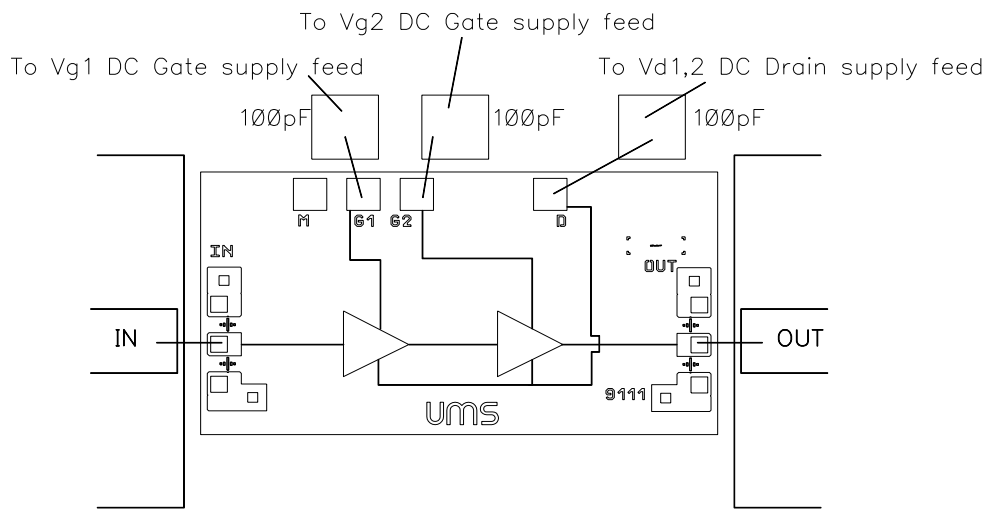


Mechanical data



Chip thickness: 100 μ m.
 Chip size: 890x1620 $\pm$ 35 μ m
 All dimensions are in micrometers

Recommended assembly plan



Note: Supply feed should be bypassed. 25 μ m diameter gold wire is to be preferred.

Recommended circuit bonding table

Label	Type	Decoupling	Comment
D	Vd	100pF	Drain Supply
G1	Vg1	100pF	Multiplier Gate Supply
G2	Vg2	100pF	Buffer amplifier Gate Supply
M	GND	NC	No connection required

Recommended reflow process assembly

Refer to the application note AN0001 available at <https://www.ums-rf.com> for die attach.

Recommended ESD management

Refer to the application note AN0020 available at <https://www.ums-rf.com> for ESD sensitivity and handling recommendations.

Ordering Information

Chip form:

CHX2089-99F/00

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