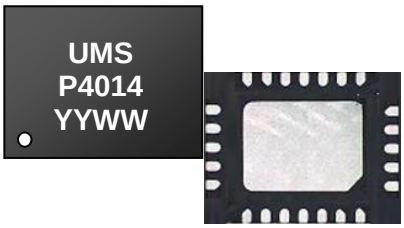
CHP4014-QEG

5-6GHz 6-bit Phase-Shifter

GaAs Monolithic Microwave IC in SMD leadless package

Description

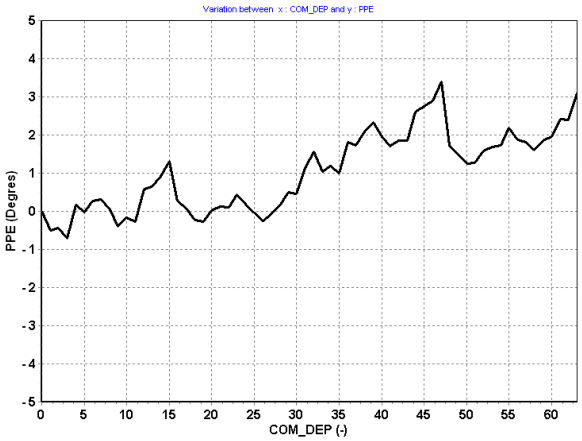
The CHP4014-QEG is a 6-bit digital phase shifter MMIC with a 0°-360° range. It is designed for 5 to 6GHz frequency range applications. The circuit supports a variety of C-band phased array applications including industrial sensors and military radars.
The circuit is manufactured with a Power pHEMT process, 0.25µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.



It is available in lead-free SMD package.

Main Features

- C-Band
- 5.625° phase step
- 6dB Losses
- 26dBm input power at -1dB comp.
- I/O reversible
- TTL compatible control inputs
- 24 leads QFN4x5 SMD package



Peak Phase Error versus state @ 5.5GHz
(packaged device, board measurement)

Main Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	5		6	GHz
G	Small signal gain	-7	-6		dB
P1dB	Input power at 1dB compression		26		dBm
VAi(1)	Voltage control	0		7	V

(1) (1, 2, 3, 4, 5, and 6)

ESD Protection: Electrostatic discharge sensitive device. Observe handling precautions!

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Main Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	5		6	GHz
PhS	Phase Shifting Range	0		360	deg
PhS step	Phase Shifting Step		5.625		deg
PPE	Peak Phase Error		+/- 4	+/- 7	deg
RMSPE	RMS Phase Error		1	2	deg
Ls	Insertion Loss		6	7	dB
LsV	Insertion Loss variation		+/- 0.4	+/- 0.7	dB
VSWR_In	Input Return Loss	10	15		dB
VSWR_Out	Output Return Loss	10	15		dB
P1dB	Input power @ 1dBc (CW)		26		dBm
IIP3	Input Third Order Intercept		32		dBm
Ts	Switching time		20	50	ns
V_low	Control Input (A1-A6) – low level	0		0.4	V
V_high	Control Input (A1-A6) – high level	2.4		7	V
V+	Positive Supply Voltage		5		V
V-	Negative Supply Voltage		- 5		V
I+	Positive Supply Current		3.5	10	mA
I-	Negative Supply Current		3.5	10	mA
Top	Operating temperature	-40		+85	deg

Peak Phase Error (PPE) definition

$PPE_{(i)}$ =measured_phase$(S21)_{(i)}$ – measured_phase$(S21)_{(0)}$ – theoretical_phase$_{(i)}$

where (i) is the state (from 0 to 63)

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RMS Peak Phase Error (RMSPE) definition

$$\text{RMSPE} = \sqrt{\frac{\sum_{i=0}^{63}(PPE(i) - \overline{PPE})^2}{64}}$$

Where $\overline{PPE} = \frac{\sum_{i=0}^{63} PPE(i)}{64}$

Insertion Losses Variation (LsV) definition

$LsV_{(i)}$ =measured_dB(S21)$_{(i)}$ – measured_dB(S21)$_{(0)}$

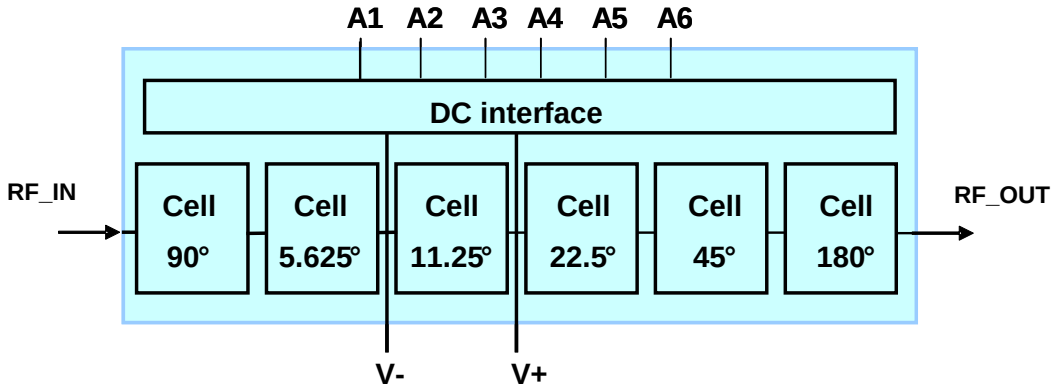
where (i) is the state (from 0 to 63)

Absolute Maximum Ratings (1)

Tamb.= +25°C

Symbol	Parameter	Values	Unit
V+	Maximum DC positive supply voltage	+8	V
V-	Maximum DC positive supply voltage	-8	V
Ai(2)	Phase Shifter CTRL voltage (V_low, V_high)	-2 , +8	V
Pin	Maximum peak input power overdrive	+30	dBm
Top	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +150	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.
(2) = (1, 2, 3, 4, 5, and 6)



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Phase Shifter Control Interface

The 6-bit phase shifter is controlled by 6 voltages (A1 to A6). Reference state is “0”. State is “0” when 0V is applied, state is “1” when +3.3V is applied.

State	A1	A2	A3	A4	A5	A6	Phase (deg)
0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	5,625
2	0	1	0	0	0	0	11,25
3	1	1	0	0	0	0	16,875
4	0	0	1	0	0	0	22,5
5	1	0	1	0	0	0	28,125
6	0	1	1	0	0	0	33,75
7	1	1	1	0	0	0	39,375
8	0	0	0	1	0	0	45
9	1	0	0	1	0	0	50,625
10	0	1	0	1	0	0	56,25
11	1	1	0	1	0	0	61,875
12	0	0	1	1	0	0	67,5
13	1	0	1	1	0	0	73,125
14	0	1	1	1	0	0	78,75
15	1	1	1	1	0	0	84,375
16	0	0	0	0	1	0	90
17	1	0	0	0	1	0	95,625
18	0	1	0	0	1	0	101,25
19	1	1	0	0	1	0	106,875
20	0	0	1	0	1	0	112,5
21	1	0	1	0	1	0	118,125
22	0	1	1	0	1	0	123,75
23	1	1	1	0	1	0	129,375
24	0	0	0	1	1	0	135
25	1	0	0	1	1	0	140,625
26	0	1	0	1	1	0	146,25
27	1	1	0	1	1	0	151,875
28	0	0	1	1	1	0	157,5
29	1	0	1	1	1	0	163,125
30	0	1	1	1	1	0	168,75
31	1	1	1	1	1	0	174,375
32	0	0	0	0	0	1	180
33	1	0	0	0	0	1	185,625
34	0	1	0	0	0	1	191,25
35	1	1	0	0	0	1	196,875
36	0	0	1	0	0	1	202,5
37	1	0	1	0	0	1	208,125
38	0	1	1	0	0	1	213,75
39	1	1	1	0	0	1	219,375
40	0	0	0	1	0	1	225
41	1	0	0	1	0	1	230,625
42	0	1	0	1	0	1	236,25
43	1	1	0	1	0	1	241,875
44	0	0	1	1	0	1	247,5
45	1	0	1	1	0	1	253,125
46	0	1	1	1	0	1	258,75
47	1	1	1	1	0	1	264,375
48	0	0	0	0	1	1	270
49	1	0	0	0	1	1	275,625
50	0	1	0	0	1	1	281,25
51	1	1	0	0	1	1	286,875
52	0	0	1	0	1	1	292,5
53	1	0	1	0	1	1	298,125
54	0	1	1	0	1	1	303,75
55	1	1	1	0	1	1	309,375
56	0	0	0	1	1	1	315
57	1	0	0	1	1	1	320,625
58	0	1	0	1	1	1	326,25
59	1	1	0	1	1	1	331,875
60	0	0	1	1	1	1	337,5
61	1	0	1	1	1	1	343,125
62	0	1	1	1	1	1	348,75
63	1	1	1	1	1	1	354,375

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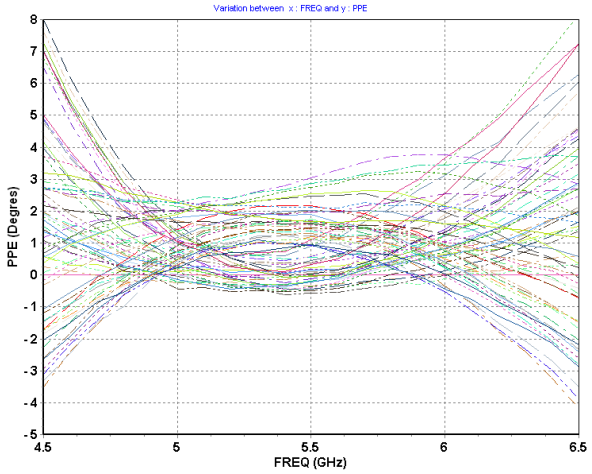
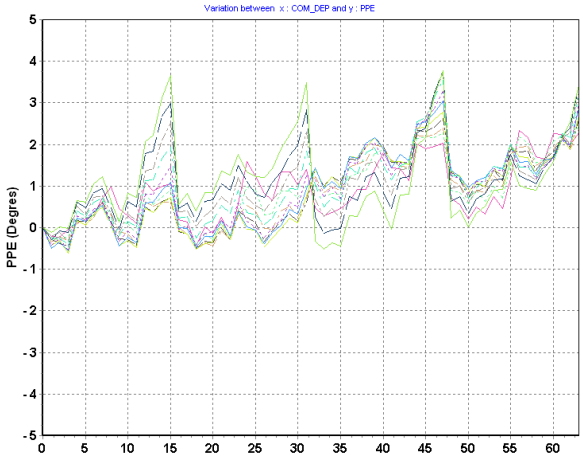
Typical S-parameter results

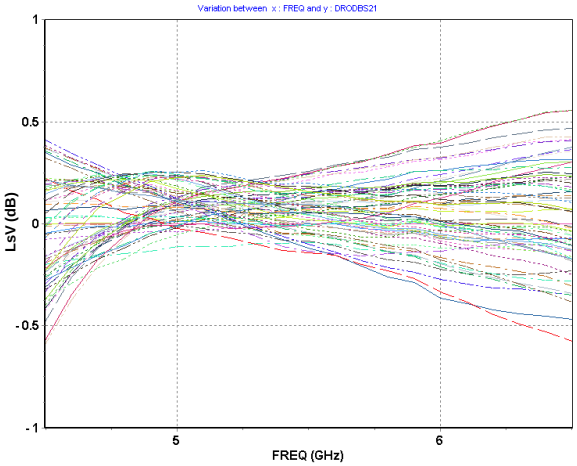
Tamb.= +25°C, packaged device, de-embedded board measurement (board drawing 98015)



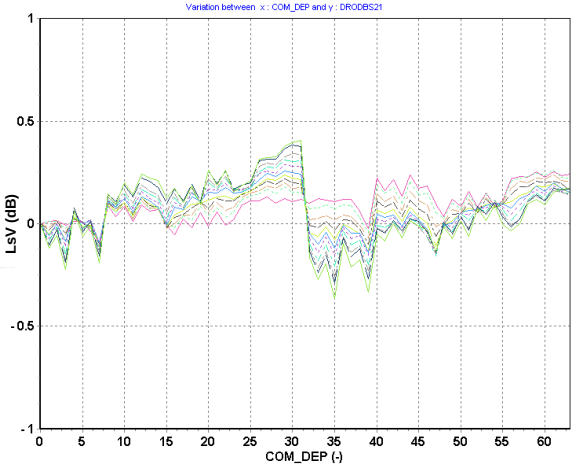
Peak phase error (deg) versus frequency (all states)



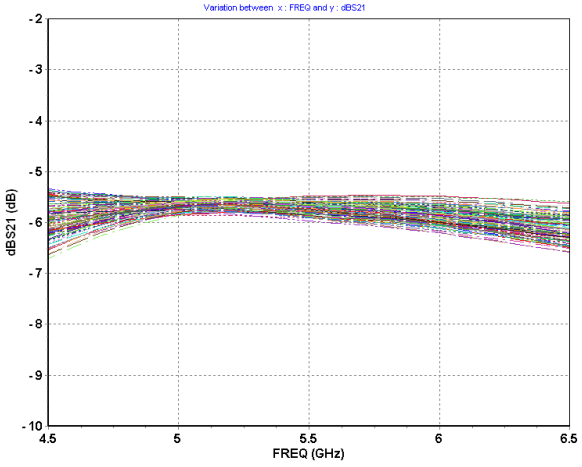
Peak phase error (deg) versus state 5GHz < frequency < 6GHz



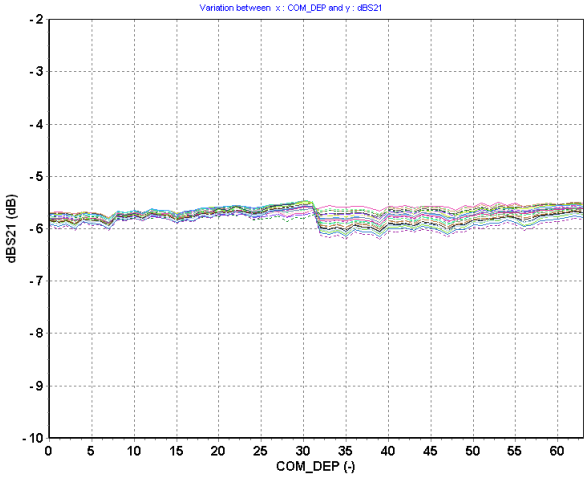
Insertion loss variation (dB) versus frequency (all states)



Insertion loss variation (dB) versus state 5GHz < frequency < 6GHz



dB(S21) versus frequency (all states)



dB(S21) versus states 5GHz < frequency < 6GHz

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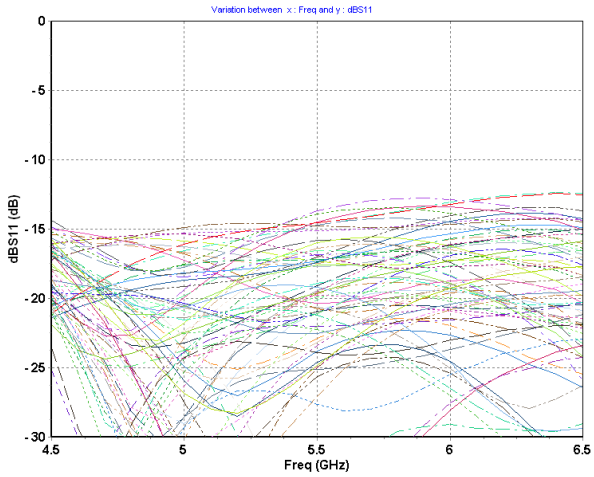
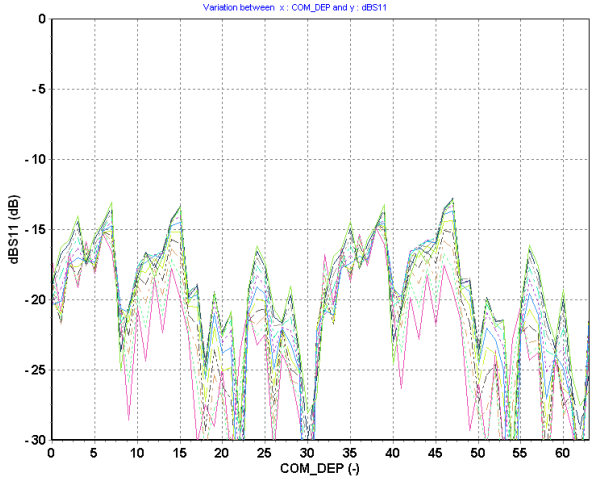
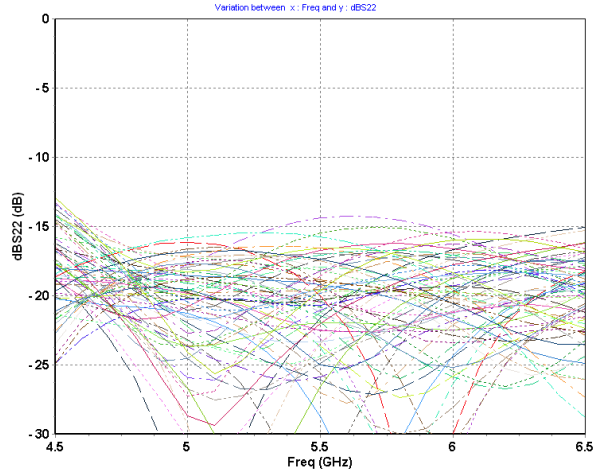
Tamb.= +25°C, packaged device, de-embedded board measurement (board drawing 98015)



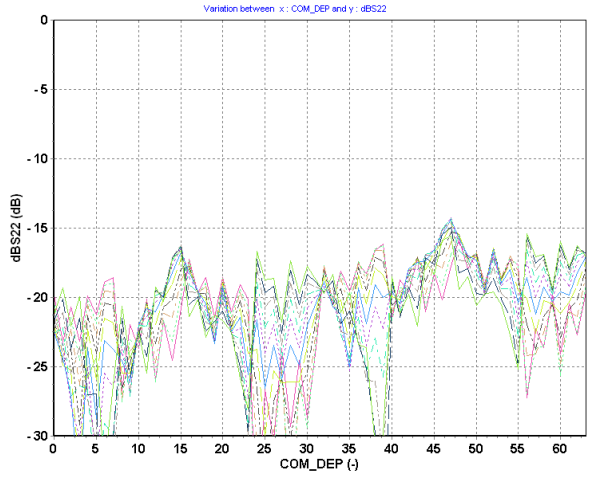
dB(S11) versus frequency (all states)



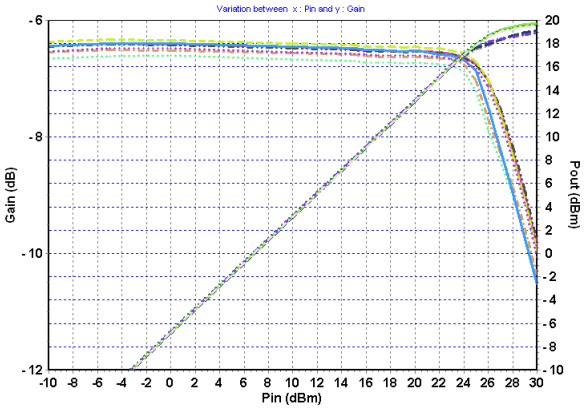
dB(S11) versus state
5GHz < frequency < 6GHz



dB(S22) versus frequency (all states)



dB(S22) versus states
5GHz < frequency < 6GHz



Gain and output power versus input power
(packaged device, board measurement, elementary states, frequency = 5.5GHz)

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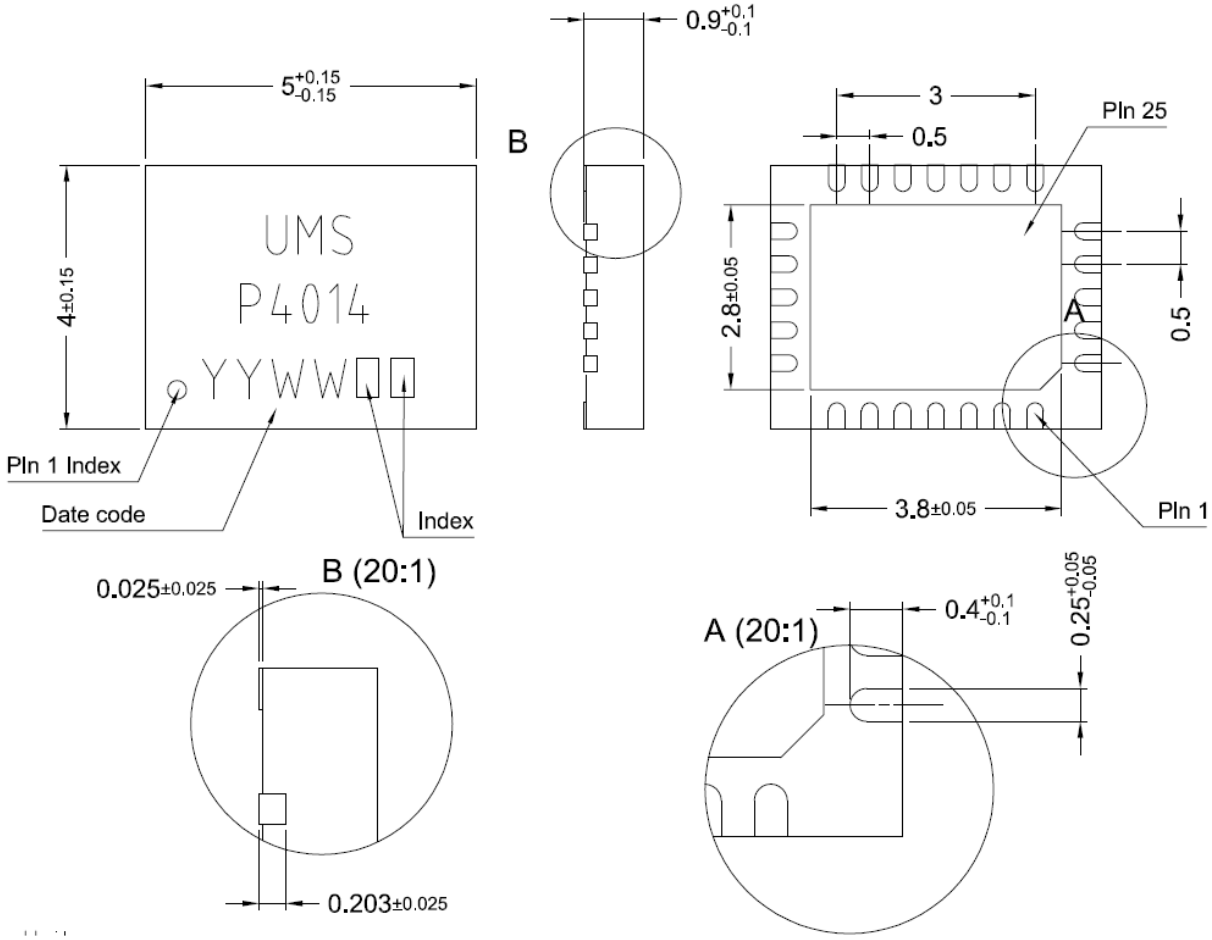
Package outline



Matt tin, Lead Free (Green)	1- Gnd(2)	9- Gnd(2)	17- A2
Units : mm	2- Nc	10- RF out	18- A1
From the standard : JEDEC MO-220	3- V+	11- Gnd(2)	19- Gnd(2)
(VGGD)	4- V-	12- Nc	20- Nc
25- GND	5- Nc	13- A6	21- Gnd(2)
	6- Nc	14- A5	22- RF in
	7- Nc	15- A4	23- Gnd(2)
	8- Nc	16- A3	24- Nc

RF_in and RF_out are AC coupled (serie capacitances inside the circuit).

(1) The package outline drawing included to this data-sheet is given for indication. Refer to the application note AN0017 (https://www.ums-rf.com) for exact package dimensions.

(2) It is strongly recommended to ground all pins marked “Gnd” through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

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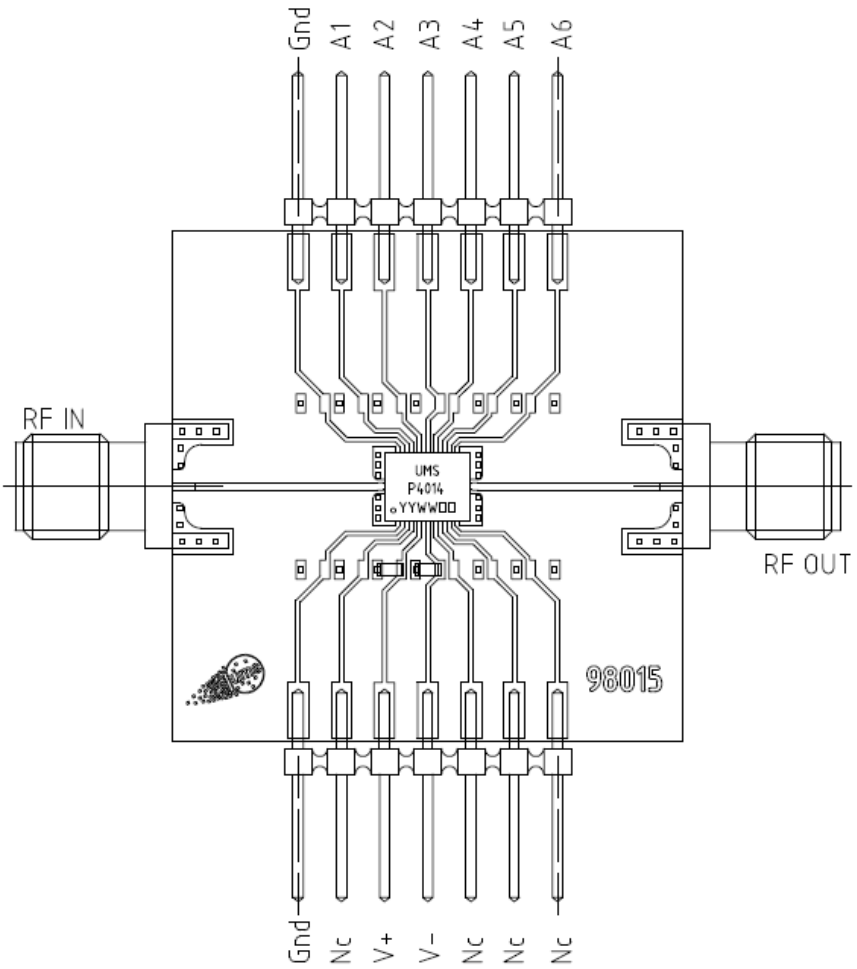
Evaluation Mother board 98015



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Notes

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Recommended package footprint

Refer to the application note AN0017 available at https://www.ums-rf.com for package foot print recommendations.

SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

Recommended environmental management

Refer to the application note AN0019 available at https://www.ums-rf.com for environmental data on UMS package products.

Recommended ESD management

Refer to the application note AN0020 available at https://www.ums-rf.com for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

QFN 4x4 RoHS compliant package:	CHP4014-QEG/XY	
	Stick: XY = 20	Tape & reel: XY = 21

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