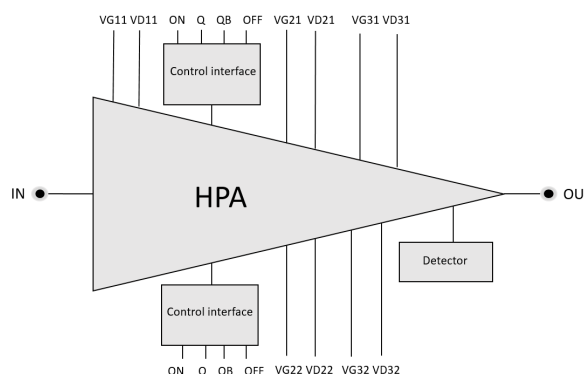


6-18 GHz High Power Amplifier

GaN Monolithic Microwave IC

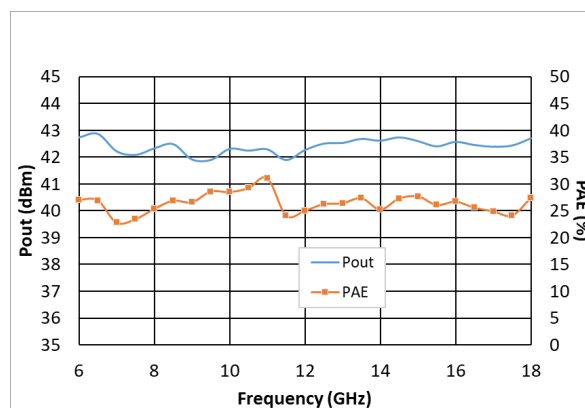
Description

The CHA8618-99F is a monolithic GaN High Power Amplifier in the frequency band 6-18GHz with a control interface for fast switching. This driver provides 42.5 dBm of Output Power. The circuit exhibits a small signal gain of 33dB. The overall power supply is of 20V/1.2A (quiescent current). It is designed for a wide range of applications, for defense systems, such as electronic warfare, and test instrumentation. The part is manufactured on robust GaN HEMT technology and is available as a bare die.



Main Features

- Broadband performances: 6-18GHz
- Linear Gain = 33dB
- Pout = 42.5dBm for +23dBm Input Power
- Id associated current = 3.6A
- DC bias: Vd=20V @Idq = 1.2A
- 3.6x5.6mm²



Main Electrical Characteristics

T_{backside} = +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	6		18	GHz
Gain	Linear Gain		33		dB
Psat	Output Power @saturation (Pin = 23dBm)		42.5		dBm
Id	Drain current @saturation (Pin = 23dBm)		3.6		A

Specifications

$T_{\text{backside}} = +25^{\circ}\text{C}$, $V_d = +20\text{V}$, $I_{dq} = 1.2\text{A}$

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	6		18	GHz
Gain	Linear Gain		33		dB
Psat	Output Power @saturation ($P_{in} = 23\text{dBm}$)		42.5		dBm
Id	Drain current @saturation ($P_{in} = 23\text{dBm}$)		3.6		A
S11	Input return loss		-15		dB
S22	Output return loss		-12		dB
Idq	Quiescent current		1.2		A
Vd	Drain voltage		20		V
Vg	Gate voltage		-2.7		V

These values are representative of measurements done in test fixture with a bonding wire of typically 0.25nH to 0.3nH.

Absolute Maximum Ratings ⁽¹⁾

$T_{\text{backside}} = +25^{\circ}\text{C}$

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	27	V
Pin	Maximum peak input power overdrive	25	dBm

⁽¹⁾ Operation of this device above anyone of these parameters may cause permanent damage.

Recommended Operating Range

$T_{\text{backside}} = +25^{\circ}\text{C}$

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	10-20	V
Idq	Quiescent drain bias current	1.2	A
Pin	Peak input power	23	dBm
Tj	Maximum Junction temperature ⁽²⁾	200	$^{\circ}\text{C}$

These values are representative of measurements done in test fixture with a bonding wire of typically 0.25nH to 0.3nH.

⁽²⁾ See Device thermal performances section page 5/20

Temperature Range

Tcase	Operating temperature range	-40 to +85	$^{\circ}\text{C}$
Tstg	Storage temperature range	-55 to +150	$^{\circ}\text{C}$

Typical Bias Conditions

Two biasing procedures are available:

1. By using standard VG biasing
2. By using the control interface

Standard VG biasing

$T_{\text{backside}} = +25^{\circ}\text{C}$

Symbol	Pad N°	Parameter	Values	Unit
VG11	40	Gate voltage tuned for $I_{dq} \approx 1.2\text{A}$	-2.7	V
VG21	32	Gate voltage tuned for $I_{dq} \approx 1.2\text{A}$	-2.7	V
VG31	15	Gate voltage tuned for $I_{dq} \approx 1.2\text{A}$	-2.7	V
VD11	38	1 st stage drain voltage	20	V
VD21	30	2 nd stage drain voltage	20	V
VD31	26	3 rd stage drain voltage	20	V

“Power ON” sequence

1. Bias HPA gate voltage close to $V_{\text{pinch-off}}$ (Typically: $VG11 = VG21 = VG31 \sim -5\text{V}$)
2. Apply VD bias voltage (Typically: $VD = VD11 = VD21 = VD31 = 20\text{V}$)
3. Increase VG up to quiescent bias drain current I_{dq}
4. Apply RF signal

“Power OFF” sequence

1. Turn off RF signal
2. Bias HPA gate voltage at VG close to $V_{\text{pinch-off}}$ (Typically: $VG11 = VG21 = VG31 \sim -5\text{V}$)
3. Turn VD bias voltage to 0V
4. Turn VG bias voltage to 0V

Typical Bias Conditions

Control interface

T_{backside}=+25°C

Symbol	Pad N°	Parameter	Values	Unit
VGON	37	Gate voltage tuned for Idq ≈ 1.2A	~ -2.7V	V
VGOFF	33	Gate pinch off voltage	-5	V
VD11	38	1 st stage drain voltage	20	V
VD21	30	2 nd stage drain voltage	20	V
VD31	26	3 rd stage drain voltage	20	V

Truth table

State	Q	QB	VGON	VGOFF
Mode ON	-4V	-11V	~ -2.7V	-5V
Mode OFF	-11V	-4V	~ -2.7V	-5V

“Power ON” sequence

1. HPA gate voltage at VGON & VGOFF close to Vpinch-off (Typically: VG ≈ -5V)
2. Bias PA gate voltage at QB = -11V
3. Bias PA gate voltage at Q = -4V
4. Apply VD bias voltage (Typically: VD11 = VD21 = VD31 = 20V)
5. Increase VGON up to quiescent bias drain current Idq
6. Apply RF signal

“Power OFF” sequence

1. Turn off RF signal
2. Bias HPA gate voltage at VGON close to Vpinch-off (Typically: VG ≈ -5V)
3. Turn VD bias voltage to 0V
4. Turn VGON bias voltage to 0V
5. Turn VGOFF bias voltage to 0V
6. Turn Q & QB voltage to 0V

Device thermal performances

All the figures given in this section are obtained assuming that the die is only cooled down by conduction through the chip backside.

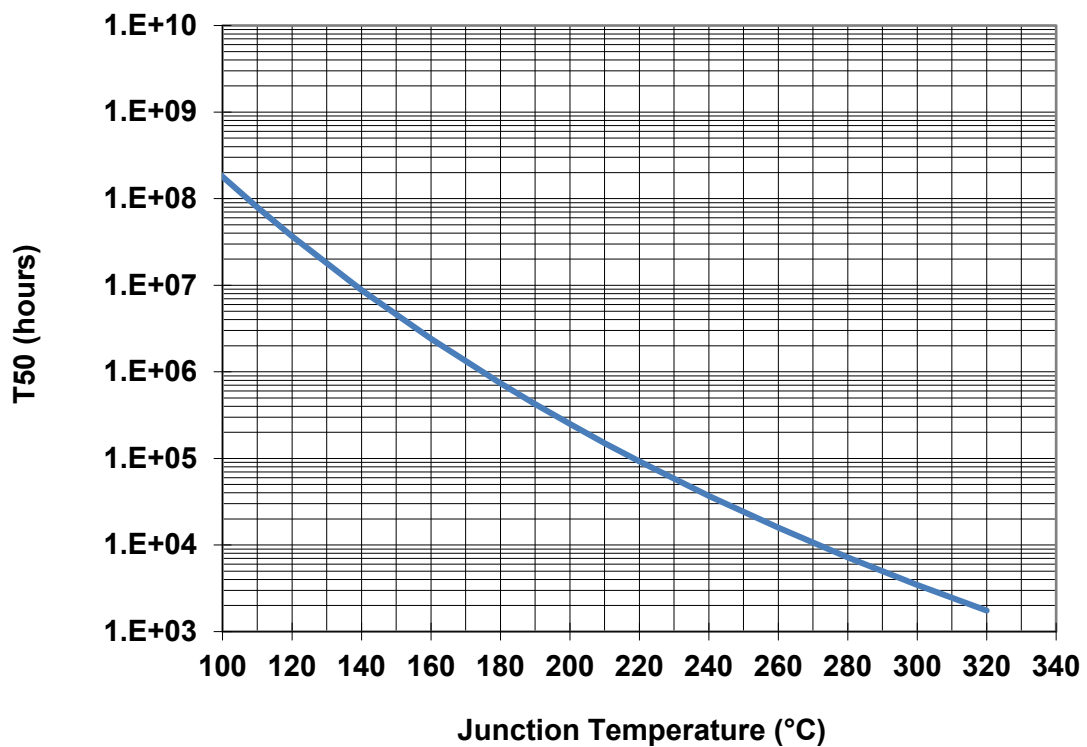
The temperature is monitored at the chip back-side interface (T_{backside}).

For nominal operating, the system maximum temperature must be adjusted in order to guarantee that T_{junction} remains below the maximum value specified in the Recommended Operating Ratings table.

So, the system PCB must be designed to comply with this requirement.

Parameter	Biasing conditions	T_{junction} (°C)	R_{TH} (°C/W)	T_{50} (hours)
$R_{\text{TH}}^{(1)}$ Thermal Resistance (Junction to Case)	$V_d = 20\text{V}$ $P_{\text{out}} = 42.5\text{dBm}$ $P_{\text{diss}} = 56.5\text{W}$	200	2.04	$3\text{E}+05$

¹ Assuming 85°C T_{backside}



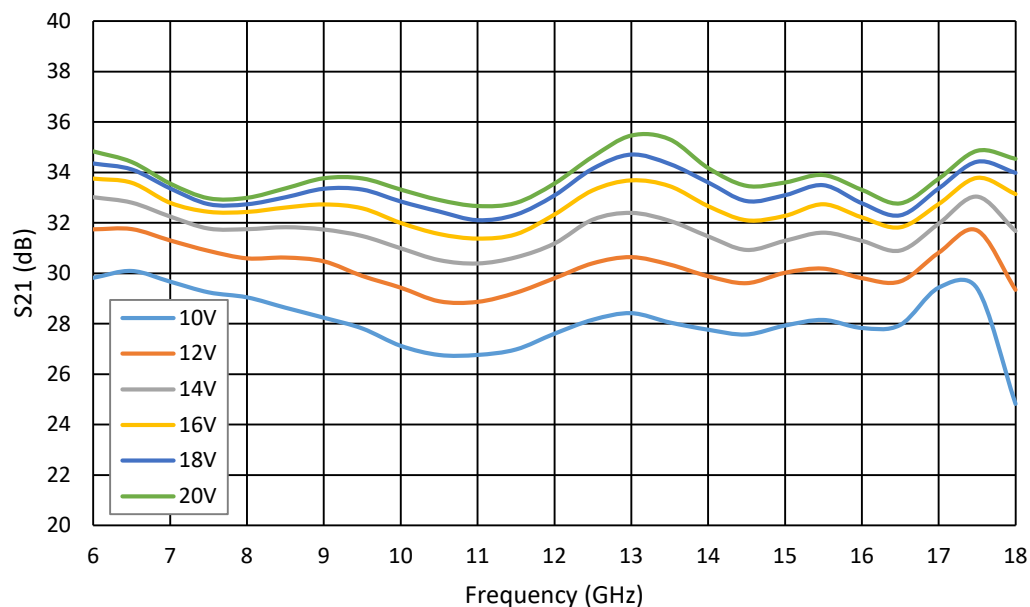
Typical On wafer measurements: Sij parameters

T_{backside} = +25°C, V_d = +20V, I_{dq} = 1.2A

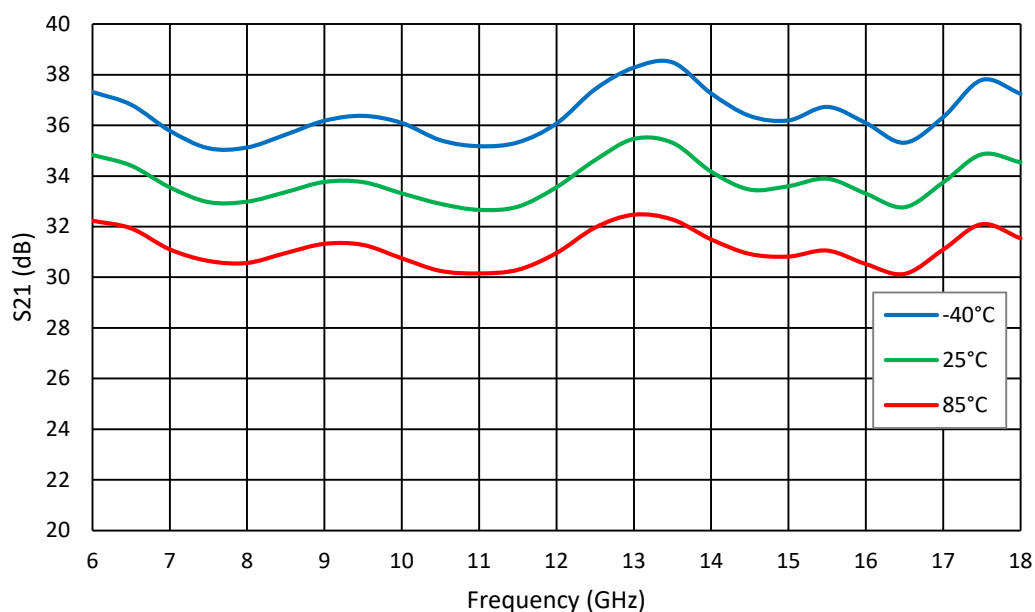
Freq (GHz)	S11 (dB)	PhS11 (°)	S21 (dB)	PhS21 (°)	S12 (dB)	PhS12 (°)	S22 (dB)	PhS22 (°)
6	-9.67	-169.94	33.26	-46.41	-84.97	-0.76	-4.49	179.97
6.5	-11.66	-172.22	32.60	-106.68	-69.21	-163.26	-8.07	159.53
7	-13.88	-166.91	31.81	-157.11	-74.62	-103.47	-10.54	148.79
7.5	-14.78	-154.76	31.57	157.57	-74.00	-94.45	-12.62	133.19
8	-14.16	-143.59	31.78	112.80	-68.83	165.77	-14.99	100.02
8.5	-12.72	-144.52	32.21	66.52	-71.08	127.62	-16.49	45.32
9	-12.03	-152.18	32.45	19.16	-67.30	-38.55	-14.31	-6.55
9.5	-12.74	-160.07	32.25	-29.10	-71.44	-2.79	-11.50	-44.81
10	-14.29	-160.46	31.66	-74.17	-72.45	101.89	-9.12	-67.60
10.5	-15.43	-152.16	31.14	-116.07	-78.25	-69.76	-8.07	-88.50
11	-15.06	-140.35	30.91	-156.22	-69.25	176.40	-7.00	-108.21
11.5	-13.21	-135.40	31.12	164.70	-62.54	-81.24	-6.47	-125.09
12	-11.76	-136.46	31.76	123.98	-66.71	-133.56	-6.67	-145.04
12.5	-10.42	-144.08	32.79	81.38	-68.50	-96.48	-7.42	-171.34
13	-9.53	-153.28	33.77	32.64	-72.56	-31.34	-9.23	164.43
13.5	-9.22	-168.17	34.38	-20.30	-67.17	-120.84	-10.75	134.30
14	-10.06	175.07	34.19	-74.44	-70.98	124.39	-13.32	94.97
14.5	-12.38	158.67	33.31	-127.66	-69.95	178.61	-13.84	45.63
15	-16.60	144.91	32.17	-175.85	-78.01	153.58	-11.32	-0.10
15.5	-25.09	137.35	31.36	137.99	-77.21	160.50	-9.80	-27.40
16	-31.19	-87.35	31.12	93.00	-66.95	164.07	-8.03	-50.20
16.5	-20.52	-85.61	31.50	44.62	-74.18	-30.25	-6.98	-67.93
17	-17.16	-108.22	32.28	-9.58	-75.26	-143.56	-5.91	-83.93
17.5	-19.87	-113.85	32.98	-72.23	-65.59	153.75	-6.39	-101.35
18	-18.24	-65.98	33.00	-142.12	-62.92	82.84	-8.21	-116.40

Typical Evaluation Board measurements with control interface

$T_{\text{backside}} = +25^{\circ}\text{C}$; $V_d = 10, 12, 14, 16, 18 \text{ \& } 20\text{V}$, $I_{dq} = 1.2\text{A}$

Linear Gain S21 (dB) vs. Frequency (GHz) and drain voltage variation

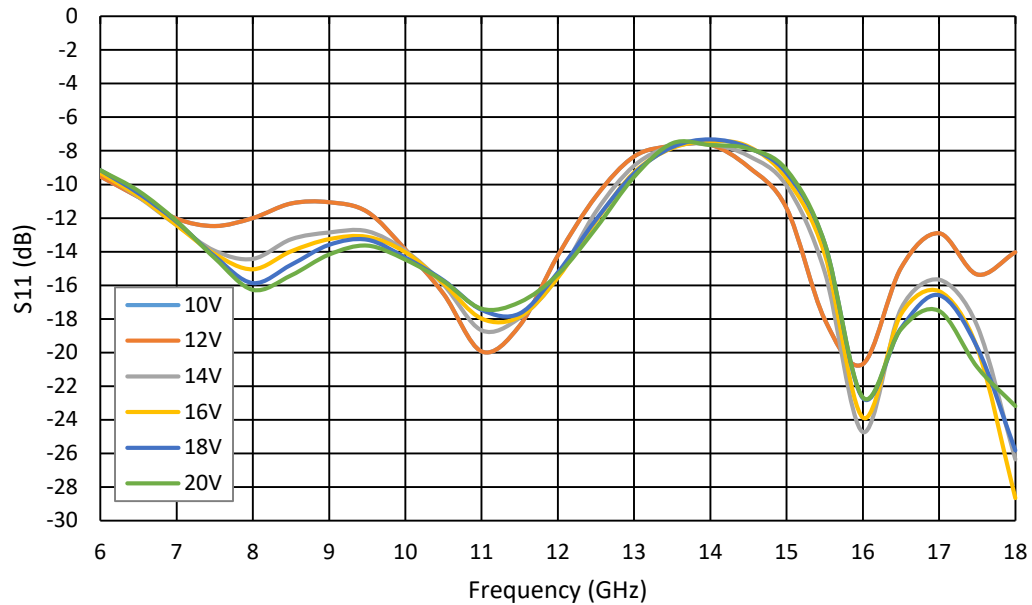
$T_{\text{backside}} = -40^{\circ}\text{C}, +25^{\circ}\text{C} \text{ \& } 85^{\circ}\text{C}$; $V_d = +20\text{V}$, $I_{dq} = 1.2\text{A @ } 25^{\circ}\text{C}$

Linear Gain S21 (dB) vs. Frequency (GHz) and drain temperature variation

Typical Evaluation Board measurements with control interface

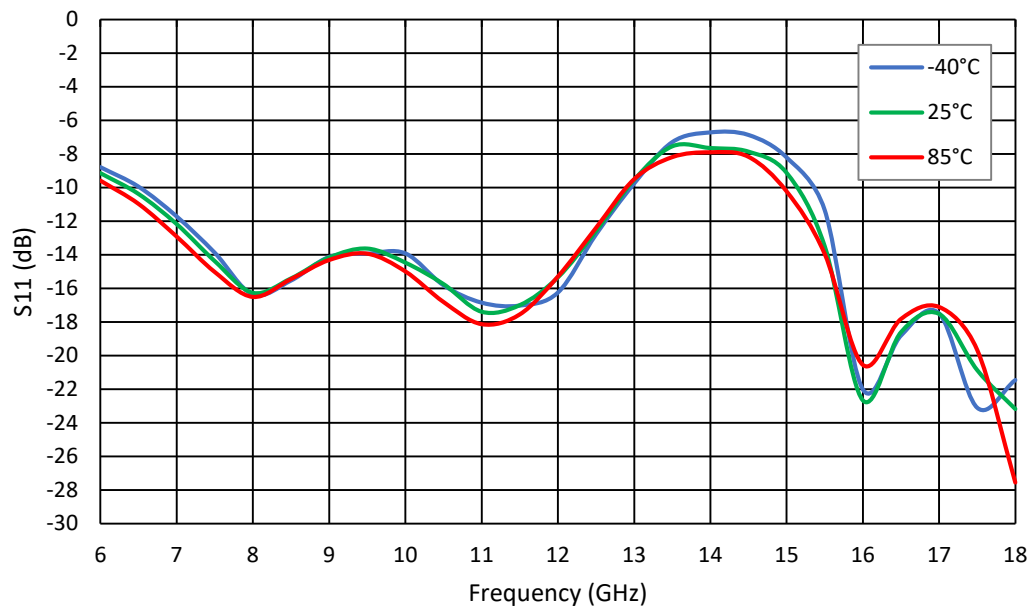
$T_{\text{backside}} = +25^{\circ}\text{C}$; $V_d = 10, 12, 14, 16, 18 \text{ \& } 20\text{V}$, $I_{dq} = 1.2\text{A}$

Input return loss S11 (dB) vs.. Frequency (GHz) and drain voltage variation



$T_{\text{backside}} = -40^{\circ}\text{C}, +25^{\circ}\text{C} \text{ \& } 85^{\circ}\text{C}$; $V_d = +20\text{V}$, $I_{dq} = 1.2\text{A @ } 25^{\circ}\text{C}$

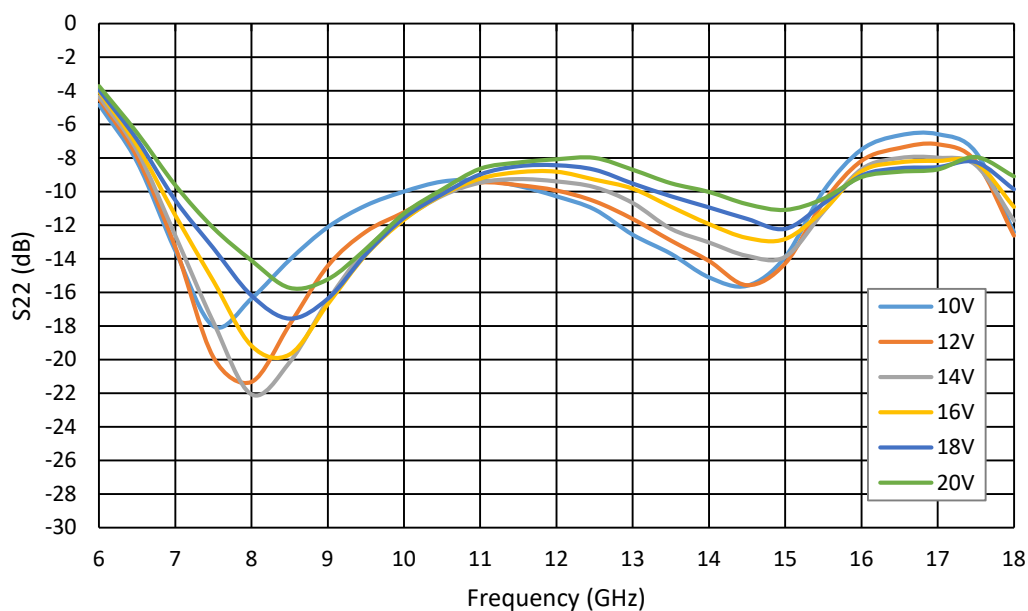
Input return loss S11 (dB) vs.. Frequency (GHz) and temperature variation



Typical Evaluation Board measurements with control interface

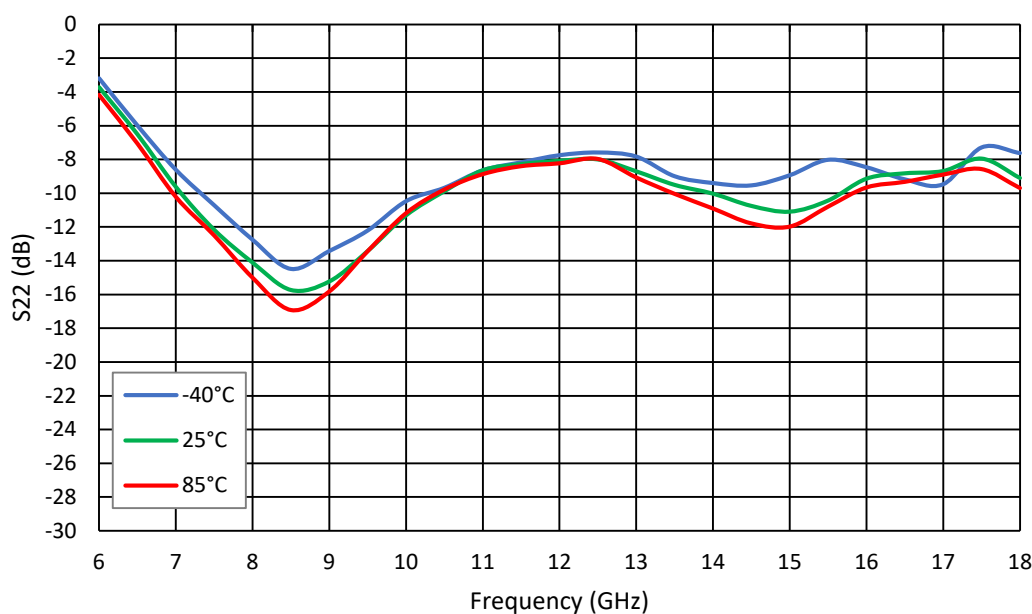
$T_{\text{backside}} = +25^{\circ}\text{C}$; $V_d = 10, 12, 14, 16, 18 \text{ \& } 20\text{V}$, $I_{dQ} = 1.2\text{A}$

Output return loss S22 (dB) vs.. Frequency (GHz) and drain voltage variation



$T_{\text{backside}} = -40^{\circ}\text{C}, +25^{\circ}\text{C} \text{ \& } 85^{\circ}\text{C}$; $V_d = +20\text{V}$, $I_{dQ} = 1.2\text{A @ } 25^{\circ}\text{C}$

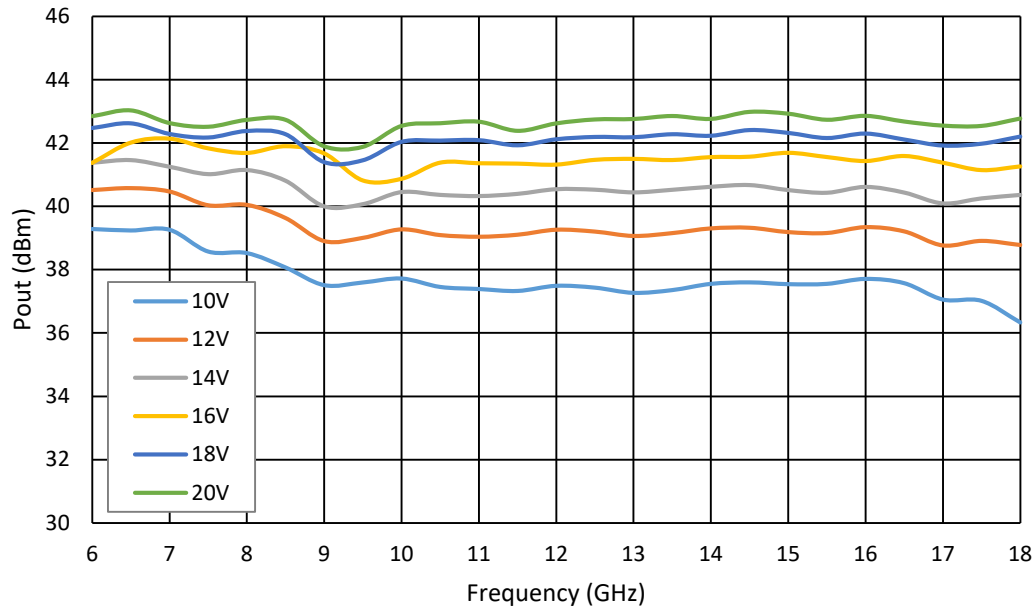
Output return loss S22 (dB) vs.. Frequency (GHz) and temperature variation



Typical Evaluation Board measurements with control interface

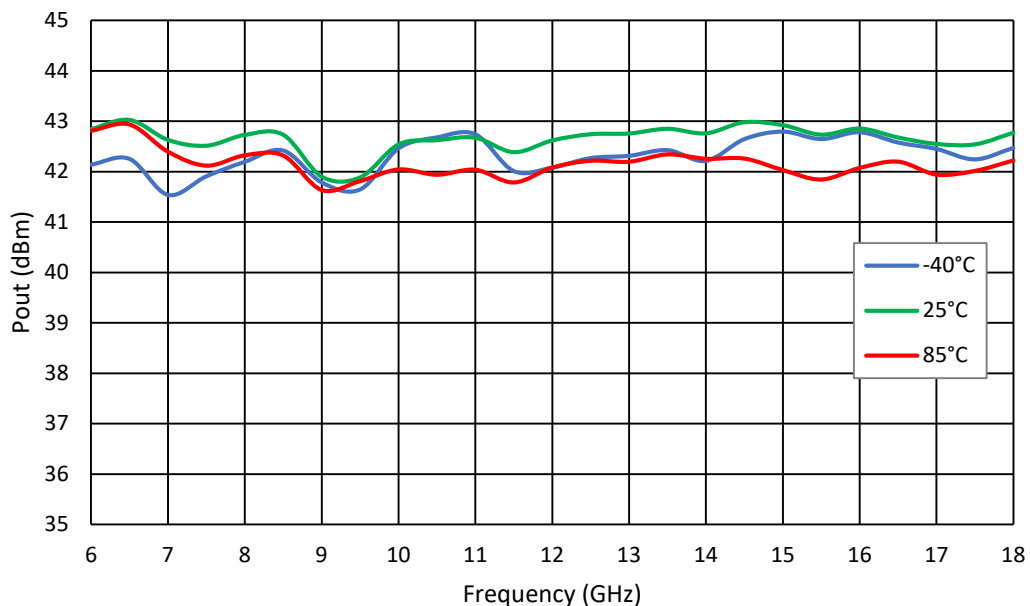
$T_{\text{backside}} = +25^{\circ}\text{C}$, $V_d = +20\text{V}$, $I_{dQ} = 1.2\text{A}@ 25^{\circ}\text{C}$; $P_{\text{in}} = 23\text{dBm}$

Pout (dBm) vs. Frequency (GHz) and drain voltage variation



$T_{\text{backside}} = -40^{\circ}\text{C}$, $+25^{\circ}\text{C}$ & 85°C ; $V_d = +20\text{V}$, $I_{dQ} = 1.2\text{A} @ 25^{\circ}\text{C}$; $P_{\text{in}} = 23\text{dBm}$

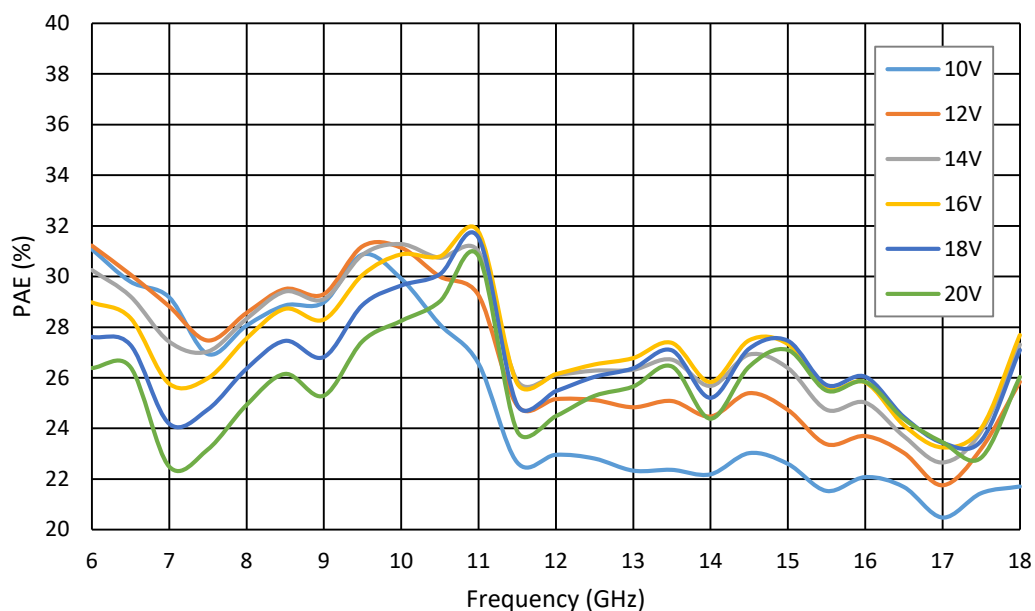
Pout (dBm) vs. Frequency (GHz) and temperature variation



Typical Evaluation Board measurements with control interface

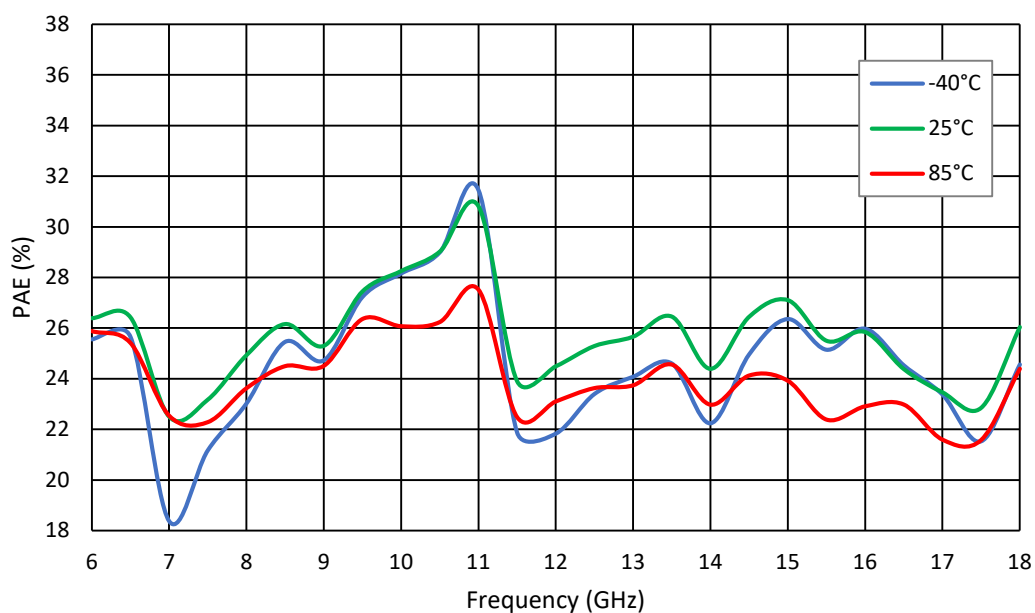
$T_{\text{backside}} = +25^{\circ}\text{C}$, $V_d = +20\text{V}$, $I_{dQ} = 1.2\text{A}$ @ 25°C ; $P_{\text{in}} = 23\text{dBm}$

PAE (%) vs. Frequency (GHz) and drain voltage variation



$T_{\text{backside}} = -40^{\circ}\text{C}$, $+25^{\circ}\text{C}$ & 85°C ; $V_d = +20\text{V}$, $I_{dQ} = 1.2\text{A}$ @ 25°C ; $P_{\text{in}} = 23\text{dBm}$

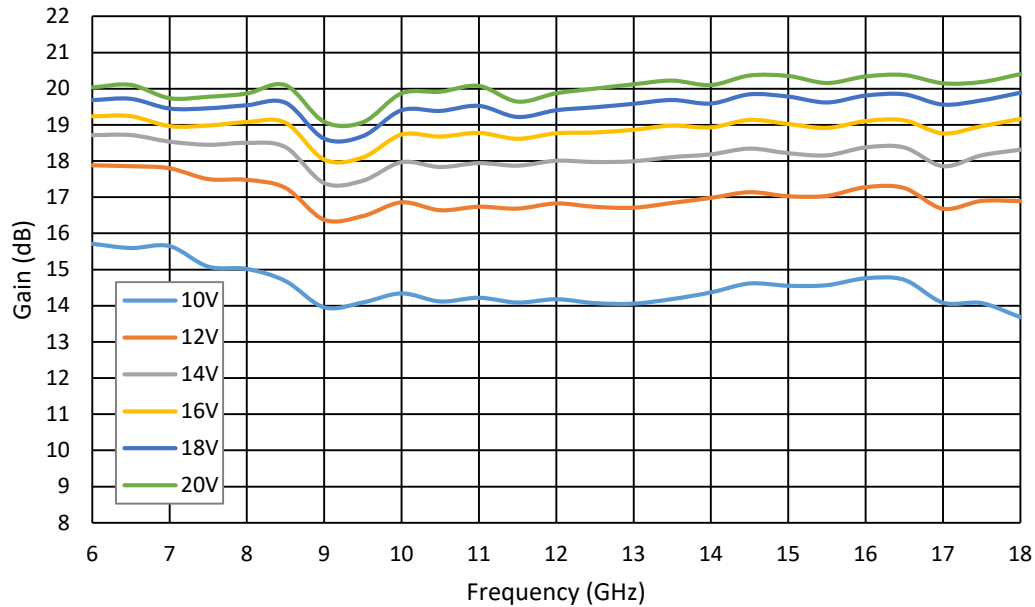
PAE (%) vs. Frequency (GHz) and temperature variation



Typical Evaluation Board measurements with control interface

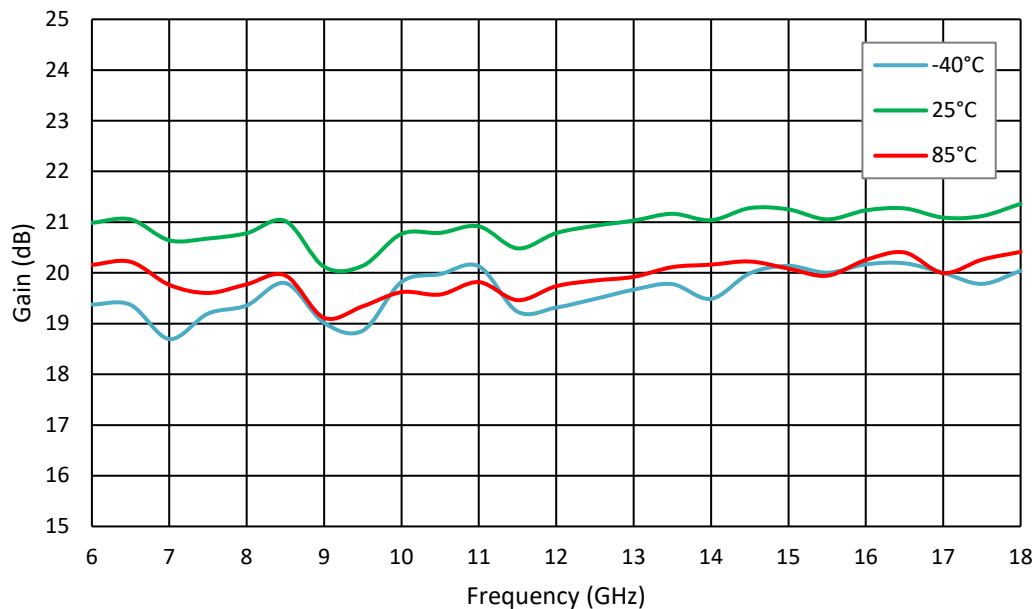
$T_{\text{backside}} = 25^{\circ}\text{C}$, $V_d = 10, 12, 14, 16, 18 \text{ \& } 20 \text{ V}$, $I_{dq} = 1.2\text{A}$; $P_{in} = 23\text{dBm}$

Gain (dB) vs. Frequency (GHz) and drain voltage variation



$T_{\text{backside}} = -40^{\circ}\text{C}$, $+25^{\circ}\text{C}$ & 85°C ; $V_d = +20\text{V}$, $I_{dq} = 1.2\text{A @ } 25^{\circ}\text{C}$; $P_{in} = 23\text{dBm}$

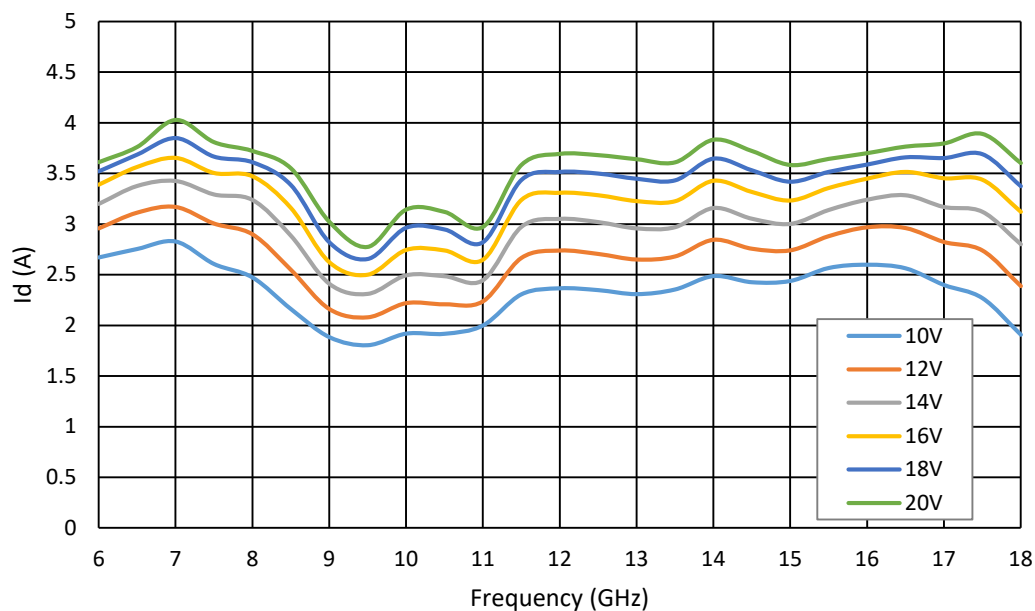
Gain (dB) vs. Frequency (GHz) and temperature variation



Typical Evaluation Board measurements with control interface

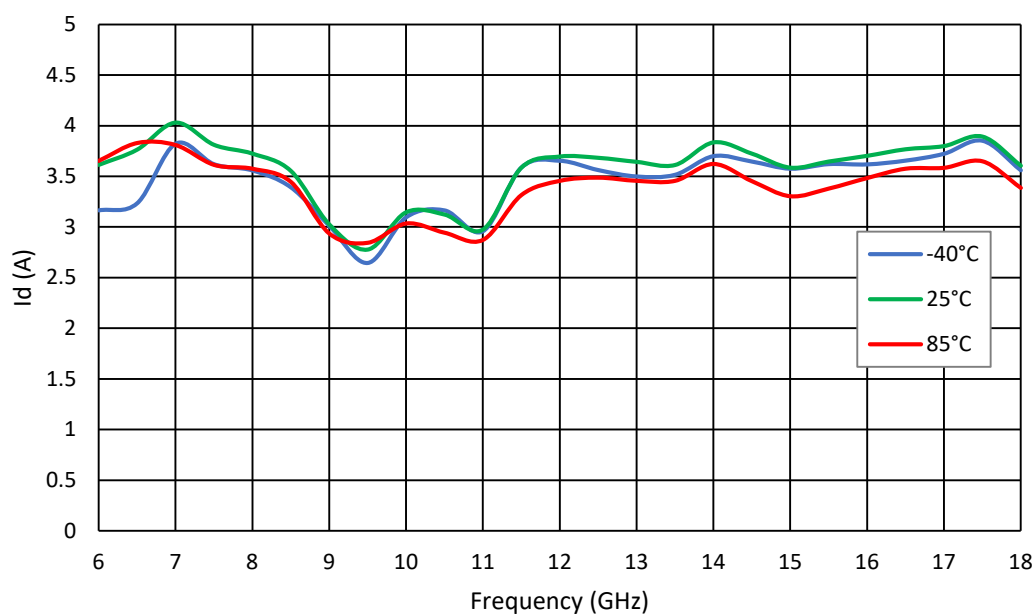
$T_{\text{backside}} = +25^{\circ}\text{C}$, $V_d = 10, 12, 14, 16, 18 \text{ \& } 20\text{V}$, $I_{dq} = 1.2\text{A @ } 25^{\circ}\text{C}$; $P_{in} = 23\text{dBm}$

I_d (A) vs. Frequency (GHz) and voltage variation



$T_{\text{backside}} = -40^{\circ}\text{C}, +25^{\circ}\text{C} \text{ \& } 85^{\circ}\text{C}$; $V_d = +20\text{V}$, $I_{dq} = 1.2\text{A @ } 25^{\circ}\text{C}$; $P_{in} = 23\text{dBm}$

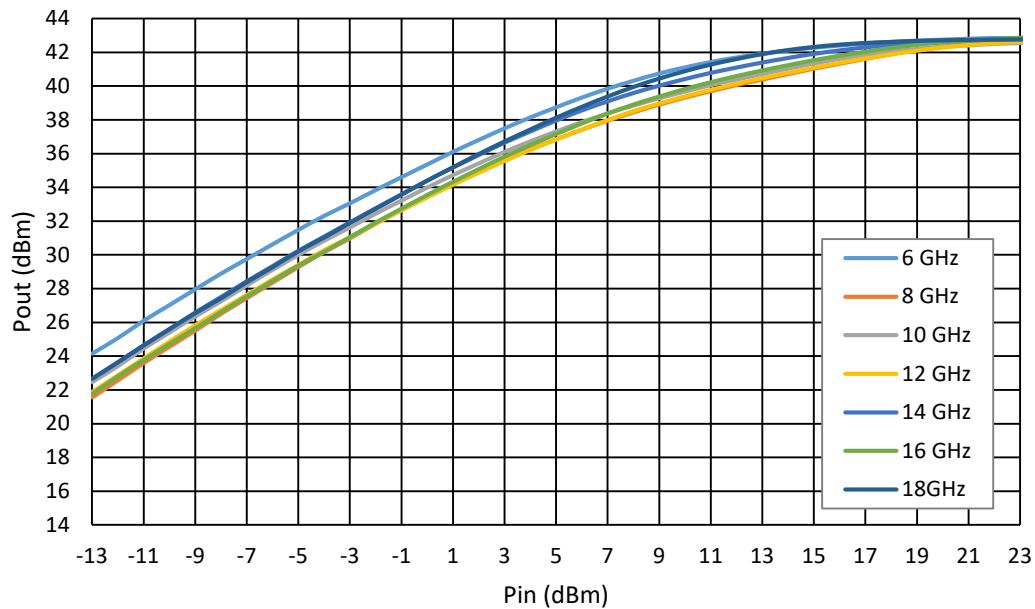
I_d (A) vs. Frequency (GHz) and temperature variation



Typical Evaluation Board measurements with control interface

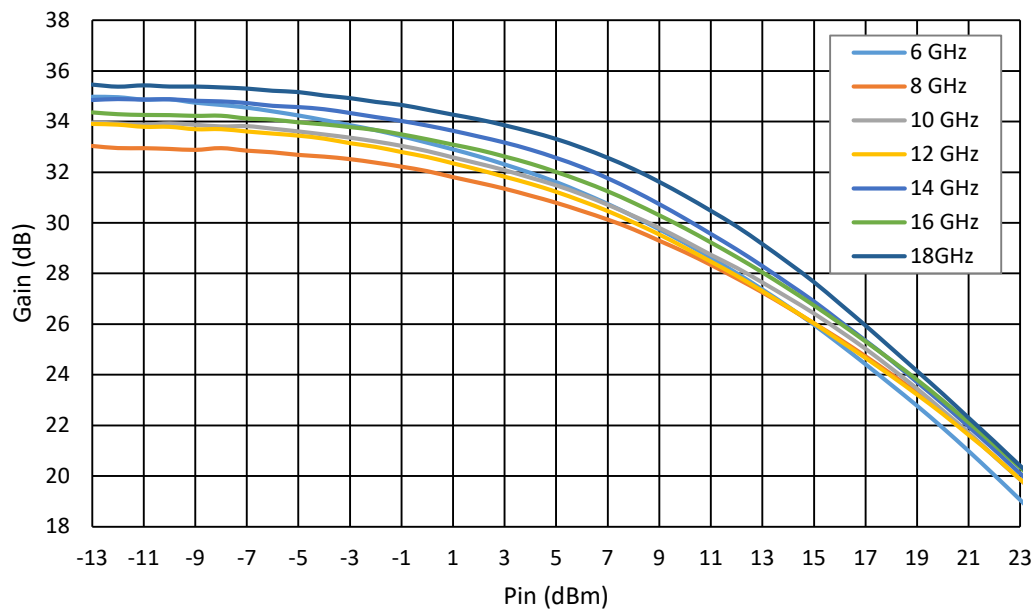
$T_{\text{backside}} = +25^{\circ}\text{C}$, $V_d = +20\text{V}$, $I_{dq} = 1.2\text{A}$;

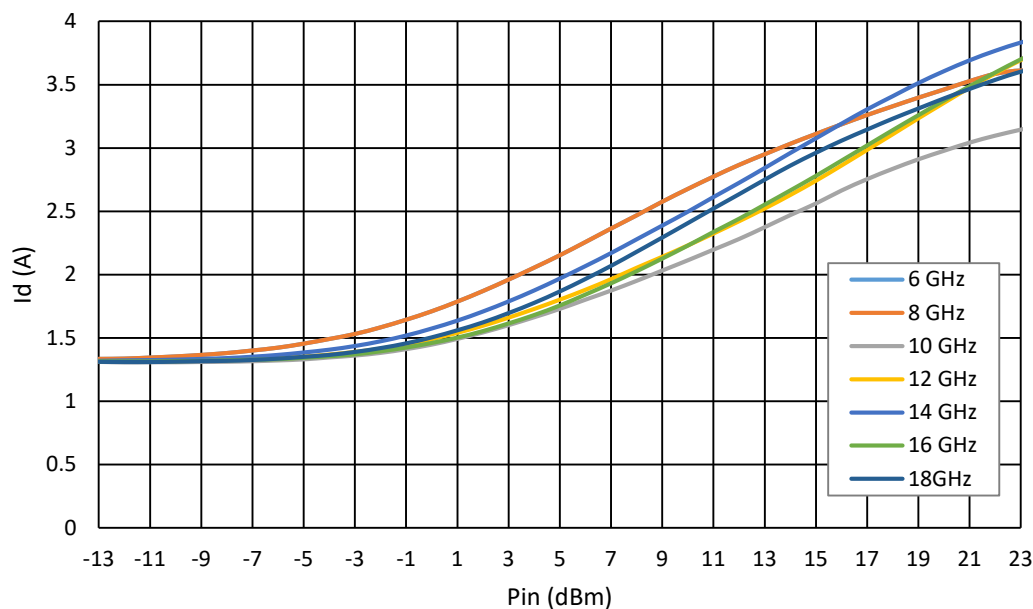
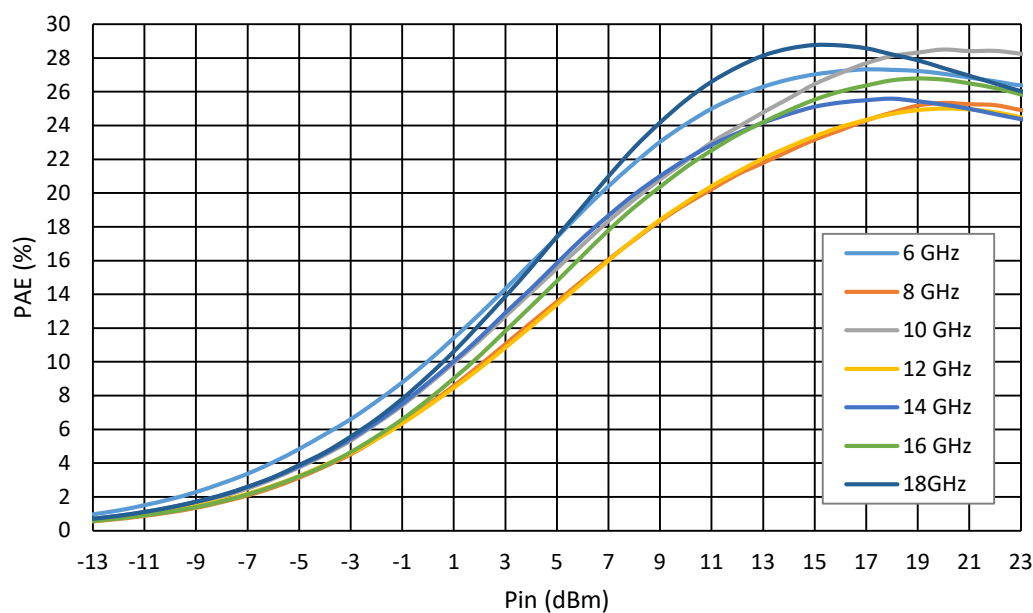
Pout (dBm) vs. Pin (dBm) and Frequency



$T_{\text{backside}} = +25^{\circ}\text{C}$; $V_d = +20\text{V}$, $I_{dq} = 1.2\text{A}$ @ 25°C

Gain (dB) vs. Pin (dBm) and Frequency



Typical Evaluation Board measurements with control interface $T_{\text{backside}} = +25^{\circ}\text{C}$, $V_d = +20\text{V}$, $I_{dQ} = 1.2\text{A}$ **I_d (A) vs. P_{in} (dBm) and Frequency** $T_{\text{backside}} = +25^{\circ}\text{C}$; $V_d = +20$, $I_{dQ} = 1.2\text{A}$ **PAE (%) vs. P_{in} (dBm) and Frequency**

Typical Bias Conditions for Power detector

Power detector

$T_{\text{backside}} = +25^{\circ}\text{C}$

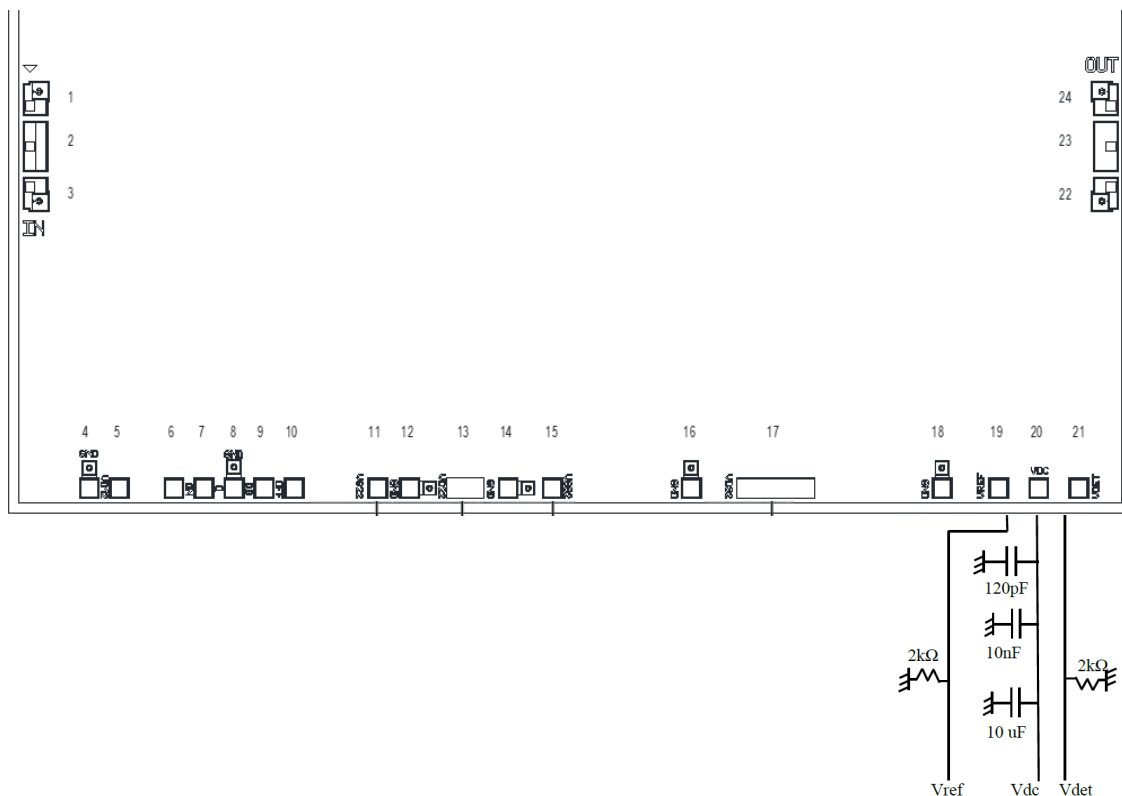
Symbol	Pad N°	Parameter	Values	Unit
VDC	20	Voltage to bias power detector	4V	V
VREF	19	Detector voltage reference (To be readen)		V
VDET	21	Detector voltage detection (To be readen)		V

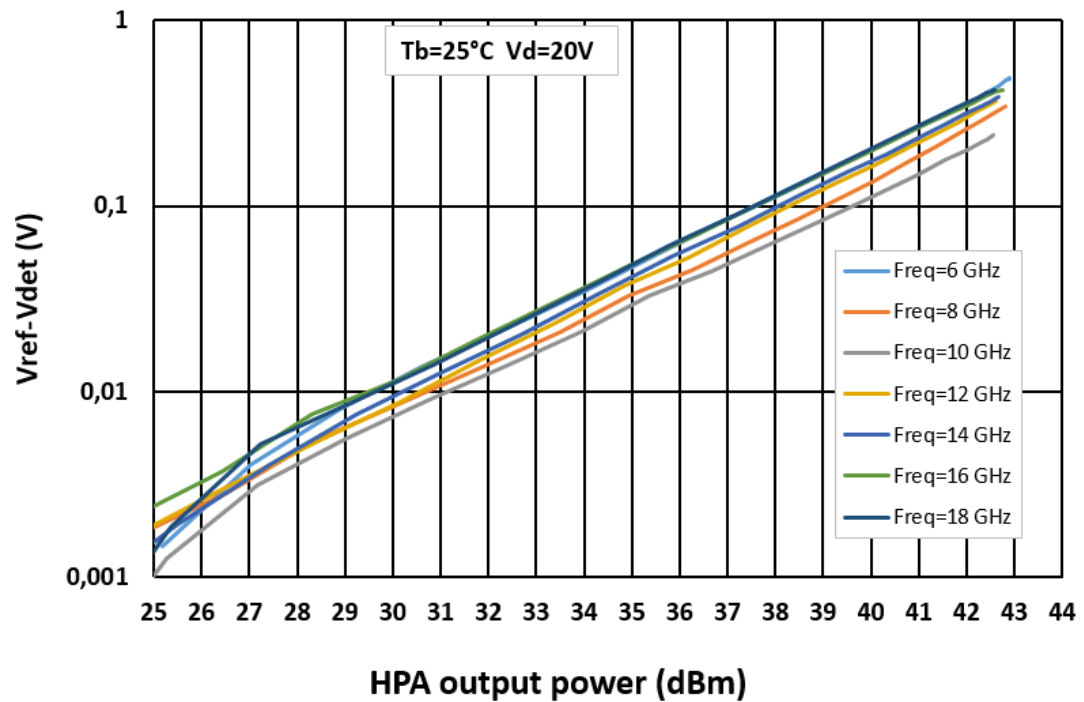
A proper decoupling will be applied on VDC access (see proposal below).

Shunt resistors will be added on VREF and VDET accesses.

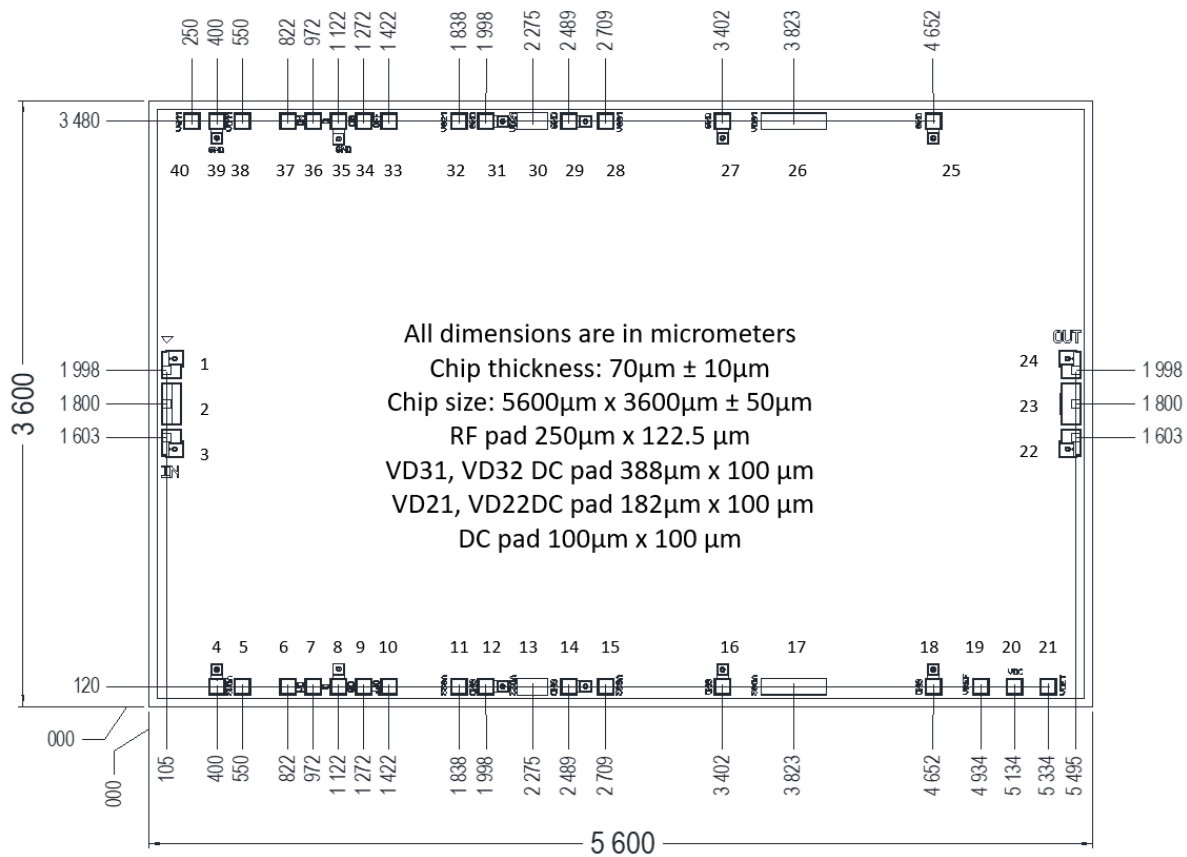
Apply VDC on detector in the range of 4V in order to get $I_{\text{Vdc}} = 2\text{mA}$

Voltage values on Vref (reference) and Vdet (detection) will be readen by multimeter:



Typical Evaluation Board measurements for power detector $T_{\text{backside}} = +25^{\circ}\text{C}$, $V_d = +20\text{V}$, $V_{DC}=4\text{V}$ **Vref-Vdet (V) vs. Pout (dBm) and Frequency**

Chip mechanical data



Pad number	Pad name	Pad type	Description
1,3, 22 & 24	GND	GND	
4, 8, 12, 14, 16, 18, 25, 27, 29, 31, 35 & 39	GND	GND	
2	IN	RF IN	RF input signal
23	OUT	RF OUT	RF output signal
40	VG11	Supply	1 st stage gate supply
32, 11	VG21, VG22	Supply	2 nd stage gate supply
28, 15	VG31, VG32	Supply	3 rd stage gate supply
38	VD11	Supply	1 st stage drain supply
30, 13	VD21, VD22	Supply	2 nd stage drainsupply
26, 17	VD31, VD32	Supply	3 rd stage drain supply
33	VGOFF		Gate pinch off voltage (Notrh)
34	QB		Gate control voltage (Notrh)
36	Q		Gate control voltage (Notrh)
37	VGON		Gate bias voltage (Notrh)
5, 19, 20, 21	-	Not connected	
6	VGON		Gate bias voltage (South)
7	Q		Gate control voltage (South)
9	QB		Gate control voltage (South)
10	VGOFF		Gate pinch off voltage (South)

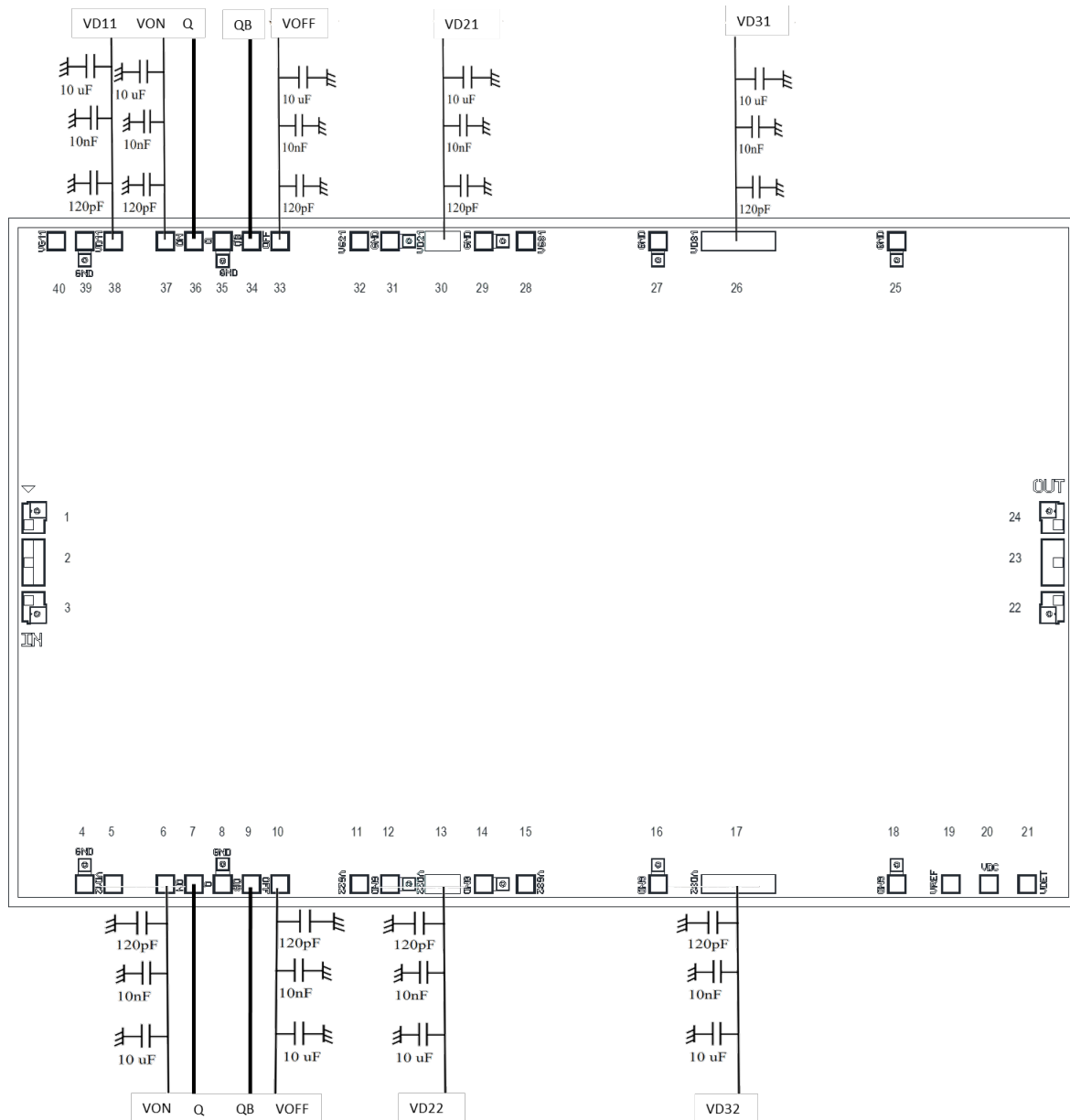
Recommended assembly plan using direct gate biasing

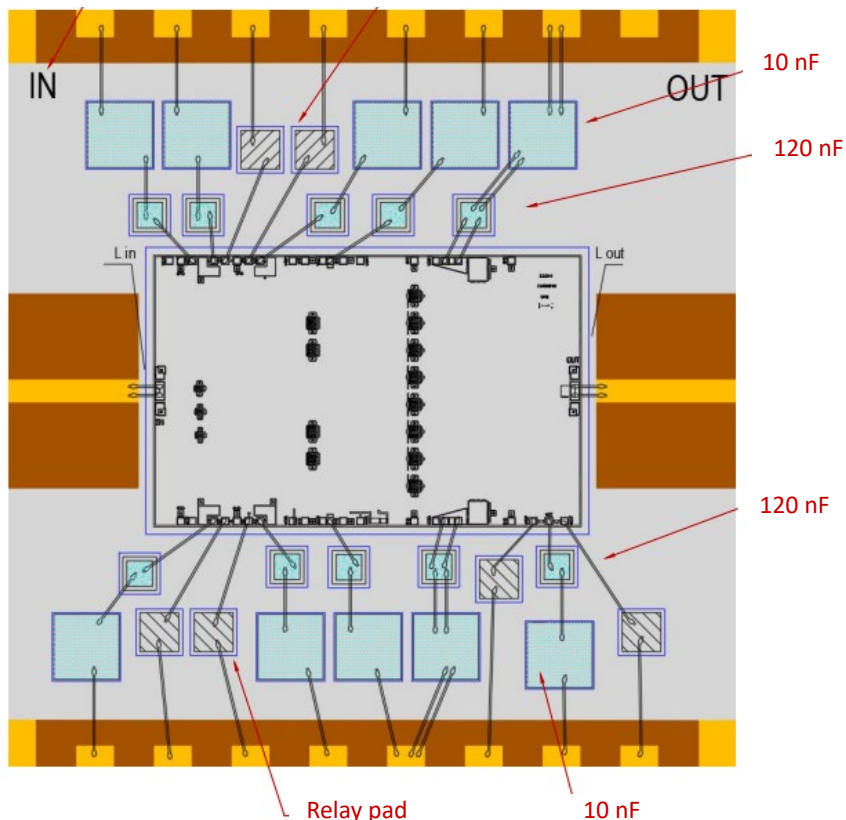
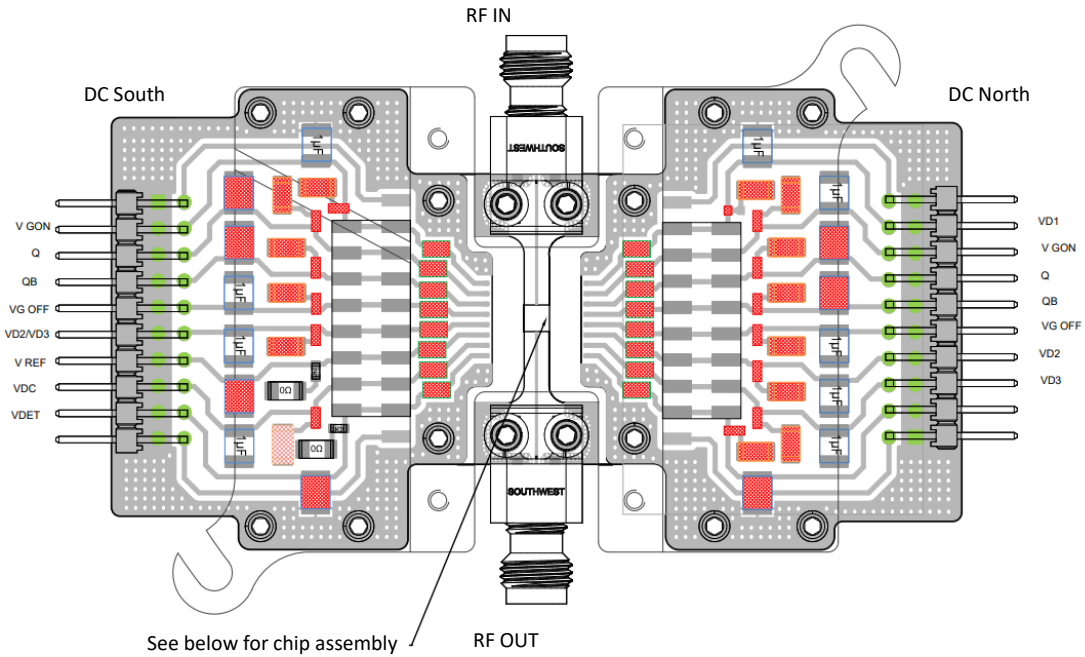
- Compatible with the proposed footprint.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 120pF, 10nF and 10μF are recommended for all DC accesses.
- See application note AN0030 for details.



Recommended assembly plan using control interface

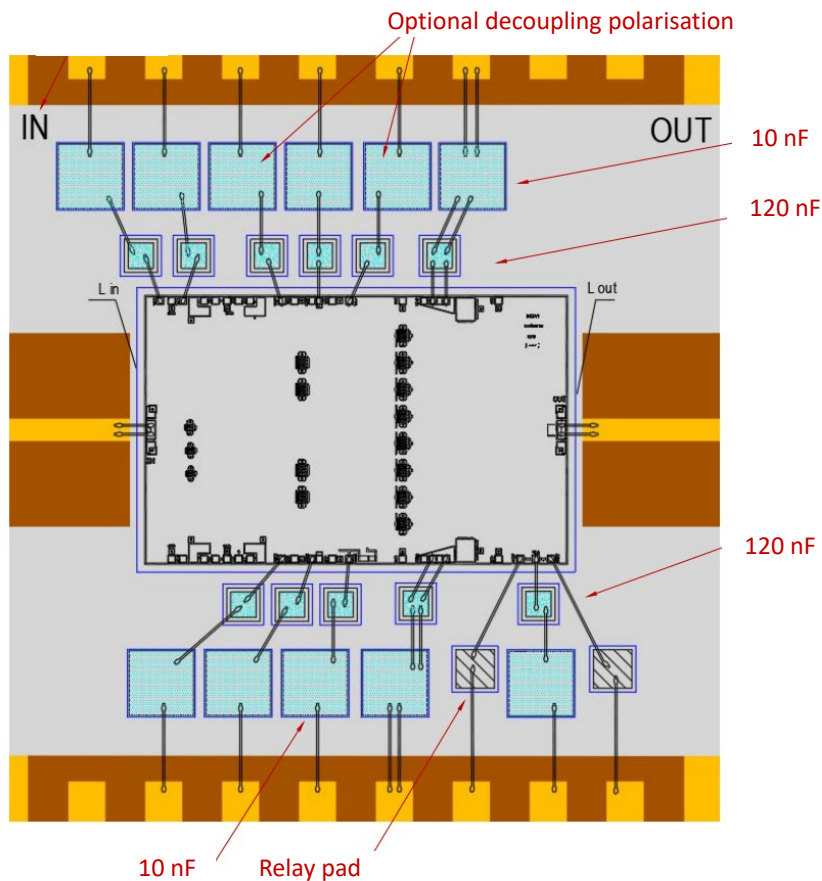
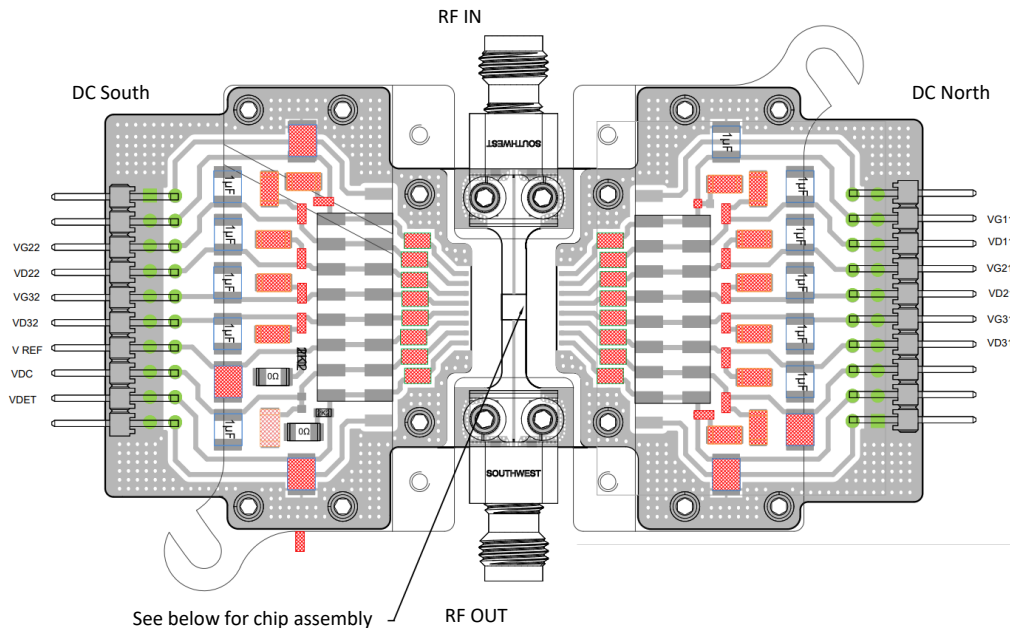
- Compatible with the proposed footprint.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 120pF, 10nF and 10μF are recommended for all DC accesses.
- See application note AN0030 for details.



Evaluation Board (EVB) with control interface

Three levels of decoupling capacitors have been used: two on the tab, one on the board. The first level is composed of 120nF chip capacitors. The second level is composed of 10nF chip capacitors. The third level is composed of 1µF capacitors. The first two levels should be as close as possible to the die.

Evaluation Board (EVB) *without* control interface



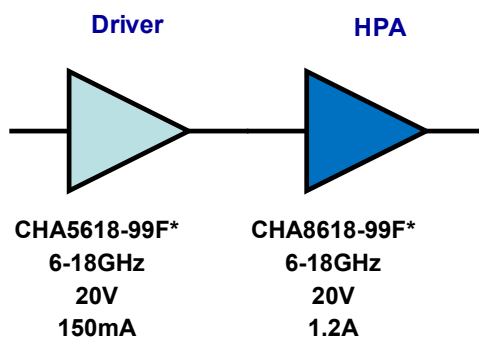
Three levels of decoupling capacitors have been used: two on the tab, one on the board. The first level is composed of 120nF chip capacitors. The second level is composed of 10nF chip capacitors. The third level is composed of 1µF capacitors. The first two levels should be as close as possible to the die.

Recommended UMS Power chain

The CHA8618-99F is recommended with the CHA5618-99F as driver.

Total Gain: > 55dB

For more information about the CHA5618-99F, see our web site www.ums-rf.com



*The driver output is 28 dBm at Psat, customer need to use the driver (CHA5618-99F) below maximum peak input power overdrive (25 dBm) of HPA (CHA8618-99F).

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACH N°1907/2006. More environmental data are available in the application note AN0019 also available at <https://www.ums-rf.com>.

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Recommended ESD management

Refer to the application note AN0020 available at <https://www.ums-rf.com> for ESD sensitivity and handling recommendations for the UMS products.

Recommended Evaluation board EVB assembly

Refer to the application note AN0030 available at <https://www.ums-rf.com> Evaluation board EVB.

Ordering Information

Chip form:

CHA8618-99F/00

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