United Monolithic Semiconductors

# CHA8454-99F

# 10W 37.5-43.5GHz High Power Amplifier

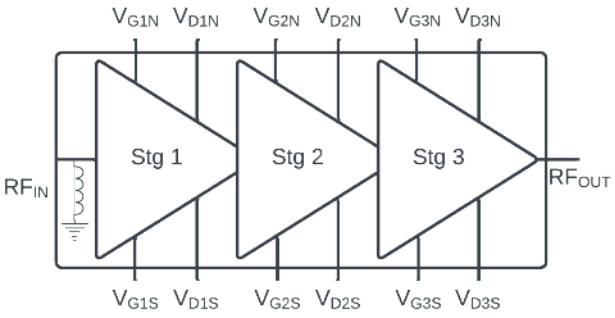
## GaN Monolithic Microwave IC

## Description

The CHA8454-99F is a three stages High Power Amplifier operating between 37.5 and 43.5GHz and providing typically 10W of saturated output power and more than 24% of Power Added Efficiency. The typical power supply is 20V/540mA (quiescent current). Thanks to a low drain voltage biasing, the CHA8454-99F provides a junction temperature below 160°C, even in saturation.

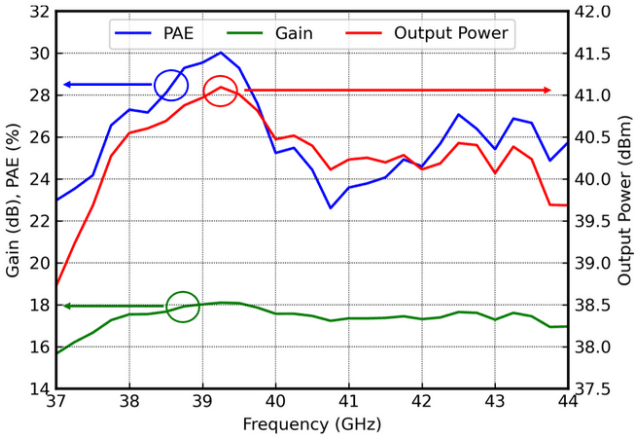
The circuit is manufactured on a space evaluated GaN-on-SiC HEMT process and is available in bare die form.

It is firstly dedicated to space, military and telecom applications and well suited for a wide range of microwave applications and systems.




## Main Features

- Frequency range: 37.5 – 43.5GHz
- High output power: 10W
- High PAE > 24%
- Linear Gain: above 23dB
- DC bias: Vd=20V @Id=540mA
- Chip size: 3.6x2.9mm²
- Available in bare die




## Main Electrical Characteristics

TB = +25°C (TB : Chip backside temperature)

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Freq | Frequency range | 37.5 | | 43.5 | GHz |
| Gain | Linear Gain | | 24 | | dB |
| Pout | Saturated Output Power | | 40.5 | | dBm |
| PAE | Power Added Efficiency | | 25 | | % |



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## Specifications

TB = +25°C, Vd = +20V, CW excitation

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Freq | Frequency range | 37.5 | | 43.5 | GHz |
| Gain | Linear Gain | | 24 | | dB |
| Pout | Saturated Output Power | | 40.5 | | dBm |
| PAE | Power Added Efficiency | | 25 | | % |
| Plin | Linear Power (1) | | 35.5 | | dBm |
| S11 | Input Return Loss | | -12 | | dB |
| S22 | Output Return Loss | | -8 | | dB |
| Idq | Quiescent Drain bias current | | 540 | | mA |
| Vd | Drain voltage | | 20 | | V |

These values are representative of on-board measurements as defined on the drawing in paragraph "Recommended assembly plan".

(1) Linear Power defined at 19dBc Noise Power Ratio, 40MHz signal bandwidth, 10% notch

## Absolute Maximum Ratings (2)

TB = +25°C

| Symbol | Parameter | Values | Unit |
|---|---|---|---|
| Vd | Drain bias voltage | 27 | V |
| Id | Drain current | 3 | A |
| Vg | Gate bias voltage | -7 to -1 | V |
| Pin | Maximum Input Power | 32 | dBm |

(2) Operation of this device above anyone of these parameters may cause permanent damage.

## Recommended Operating Range (3), (4)

| Symbol | Parameter | Values | Unit |
|---|---|---|---|
| Vd | Drain bias voltage | 18 to 25 | V |
| Id | Drain bias current | 100 to 540 | mA |
| Vg | Gate bias voltage | -5 to -2.5 | V |
| Tj | Maximum Junction temperature (5) | 200 | °C |

(3) Electrical performances are defined for specified test conditions

(4) Electrical performances are not guaranteed over all recommended operating conditions

(5) See Device thermal performances section

## Temperature Range

| | | | |
|---|---|---|---|
| TB | Operating temperature range at MMIC backside level | -40 to +95 | °C |
| $T_{stg}$ | Storage temperature range | -55 to +150 | °C |



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## Typical Bias Conditions

### TB=+25°C

| Symbol | Pad N° | Parameter | Values | Unit |
|---|---|---|---|---|
| Vg | 3, 5, 7, 25, 27, 29 | Gate voltage tuned for Idq~560mA | -3.1 | V |
| Vd | 9, 11, 13, 19, 21, 23 | Drain Voltage | 20 | V |

## “Power ON” sequence

1. Bias HPA gate voltage at Vg close to Vpinch-off (Vg~-5V)
2. Set Vd bias voltage to 0V: Id=0mA
3. Apply Vd bias voltage, Vd = 20V: Id=0mA
4. Increase Vg up to quiescent bias drain current Idq=540mA
5. Apply RF input Power

## “Power OFF” sequence

1. Turn off RF input power
2. Bias HPA Gate voltage at Vg~-5V: Id=0mA
3. Decrease Vd bias voltage down to 0V
4. Turn Vg bias voltage to 0V



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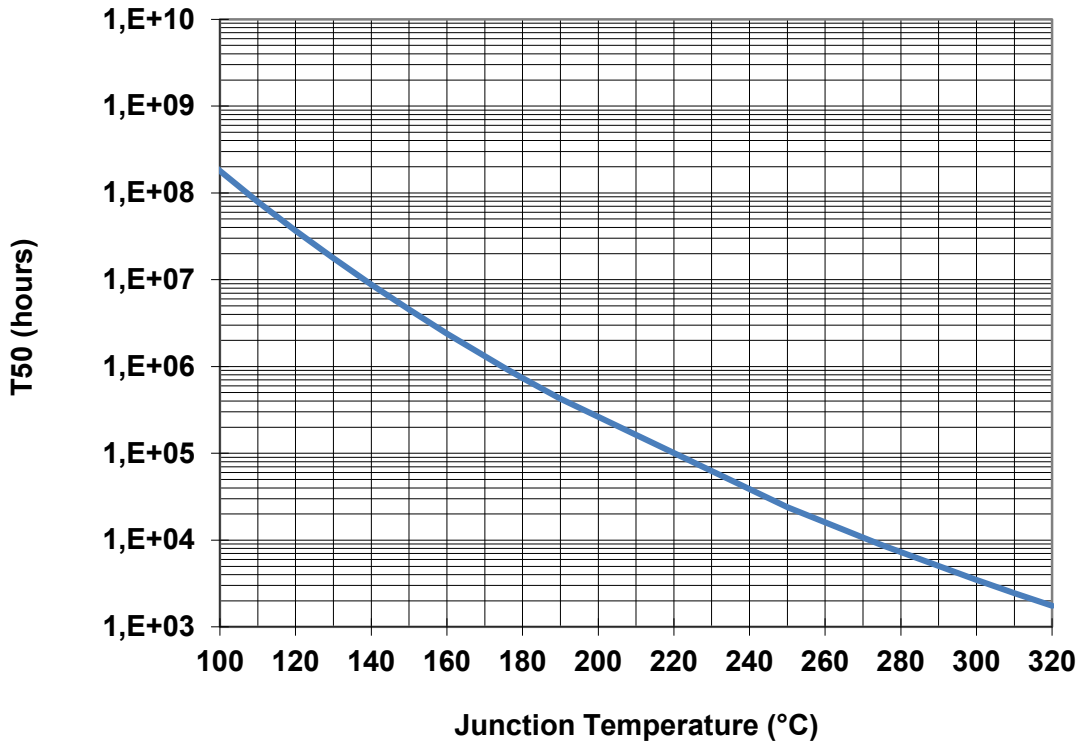
## Device thermal performance

All the figures given in this section are obtained assuming that the device is only cooled down by conduction through the thermal pad (no convection mode considered).
The temperature is monitored at the chip back-side interface (TB).
For nominal operating, the system maximum temperature must be adjusted in order to guarantee that the Junction Temperature remains below the maximum value specified in the Recommended Operating Ratings table.
Therefore, the system PCB must be designed to comply with this requirement.

| | | | | |
|---|---|---|---|---|
| Thermal Resistance (1) | $R_{th\_eq}$ | Pin at max PAE<br>TB = 85°C, Vd = 20V, Idq = 560 mA,<br>Pin = 26 dBm, Freq = 40GHz,<br>Pdiss = 32 W | 1.99 | °C/W |
| Junction Temperature | $T_j$ | | 147 | °C |
| Median Life | T50 | | 4E6 | Hrs |
| Thermal Resistance (1) | $R_{th\_eq}$ | Pin at max PAE + 4dB<br>TB = 85°C, Vd = 20V, Idq = 560 mA,<br>Pin = 30 dBm, Freq = 40GHz,<br>Pdiss = 39 W | 2.61 | °C/W |
| Junction Temperature | $T_j$ | | 186 | °C |
| Median Life | T50 | | 4E5 | Hrs |

(1) Thermal resistance measured at the backside of the chip



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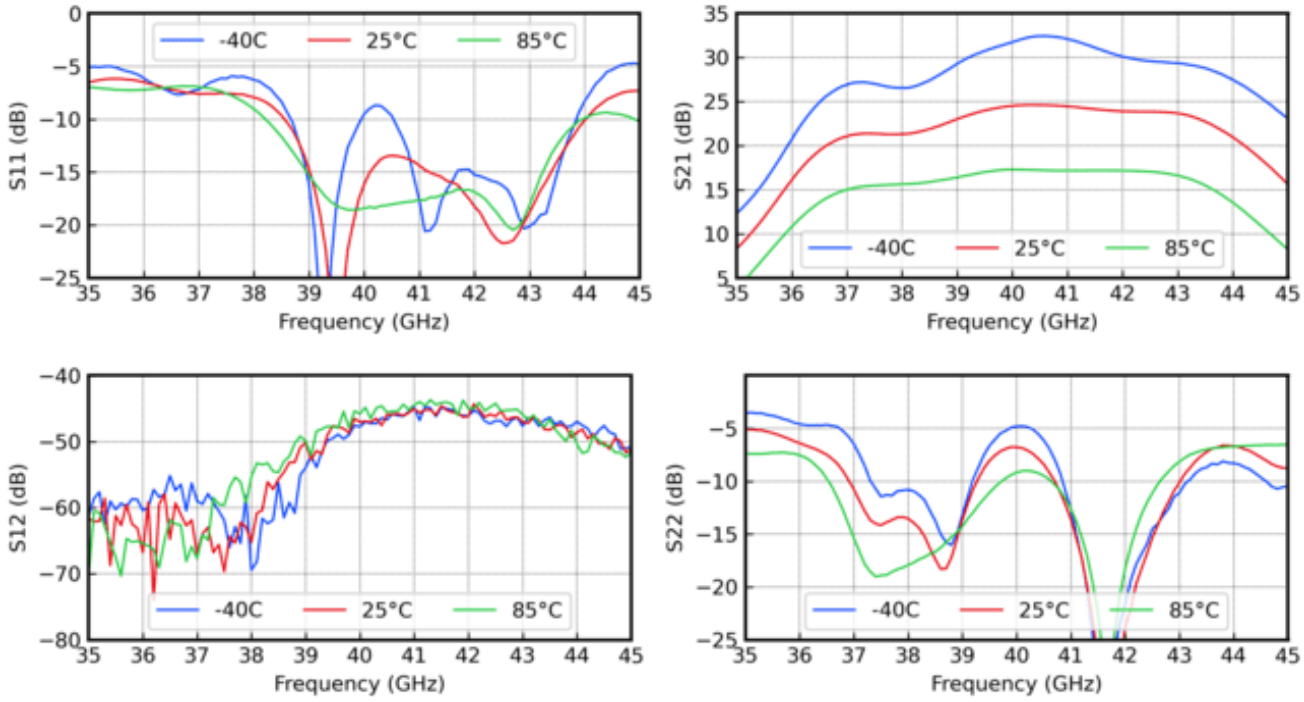
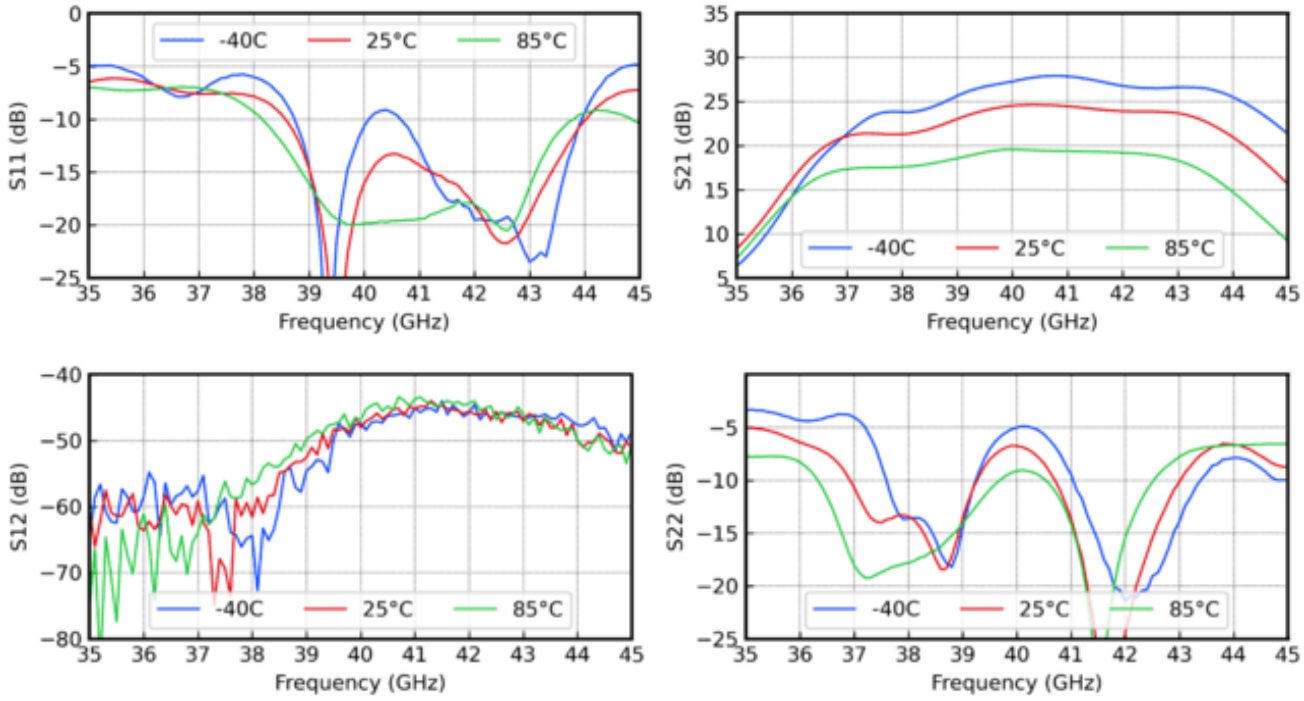
## Typical Board Measurements : Small Signal Performance

Measurements reference is at the connector plane for S11 and S22, and de-embedded at the wire-bondings planes of the RF lines for S21 and S12.

**S Parameters versus frequency and temperature**
**Test conditions** : $V_D$ = 20V, $I_{dq}$ = 560mA, TB = -40°C / 25°C / 85°C




**S Parameters versus frequency and temperature**
**Test conditions** : $V_D$ = 20V, VG fixed at $I_{dq}$ = 560mA at 25°C TB, TB = -40°C / 25°C / 85°C



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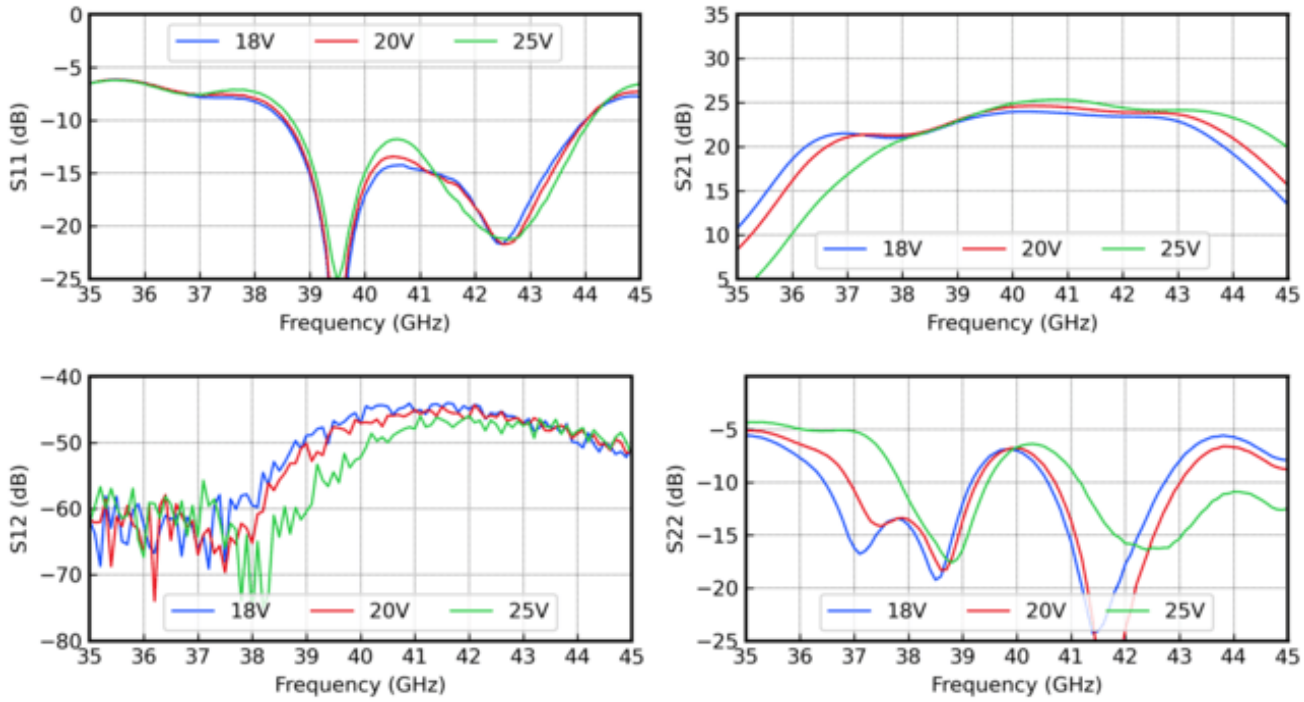
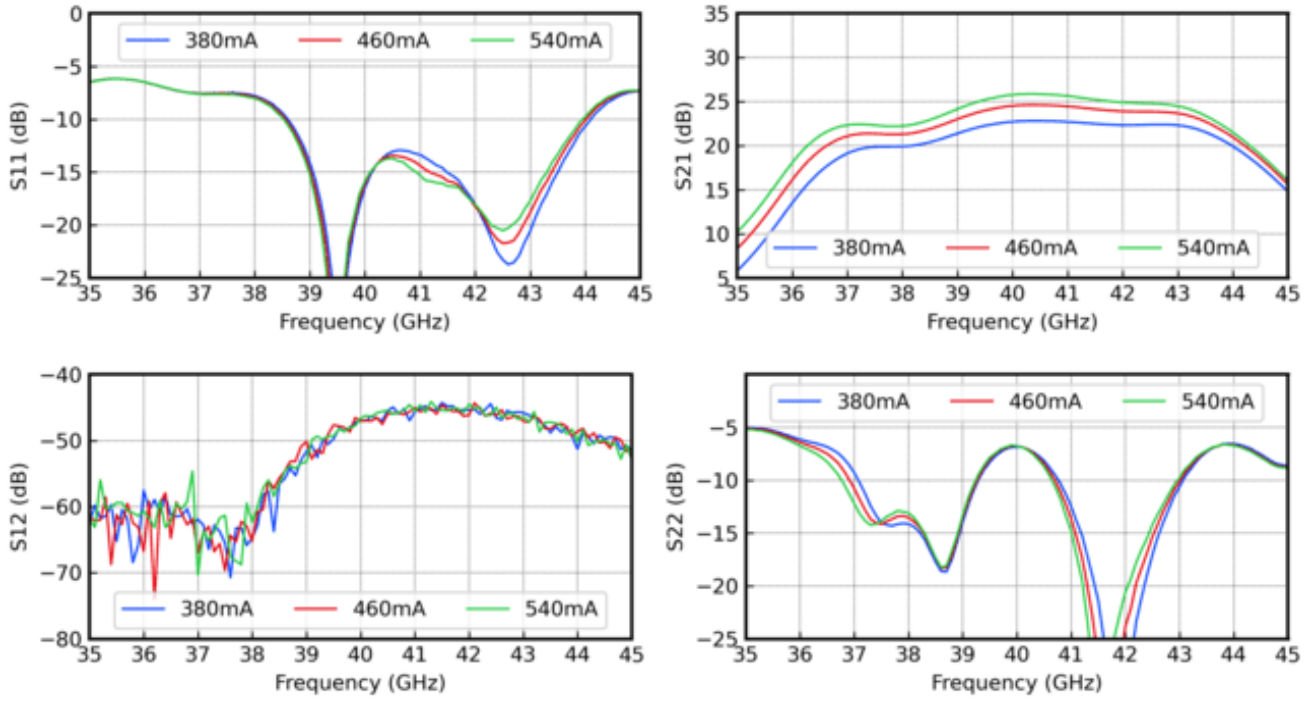
## Typical Board Measurements : Small Signal Performance

Measurements reference is at the connector plane for S11 and S22, and de-embedded at the wire-bondings planes of the RF lines for S21 and S12.

**S Parameters versus frequency and Drain Voltage**
**Test conditions** : $I_{dq}$ = 560mA, TB = 25°C




**S Parameters versus frequency and Quiescent Drain Current**
**Test conditions** : VD = 20V, TB = 25°C



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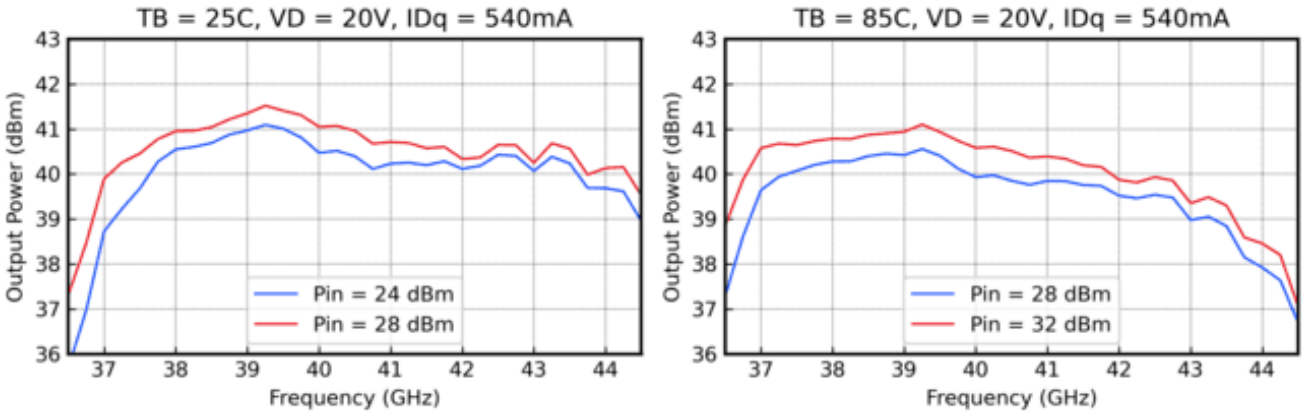
## Typical Board Measurements : Large Signal Performance

Measurements reference plane is de-embedded at the wire-bondings planes of the RF lines.

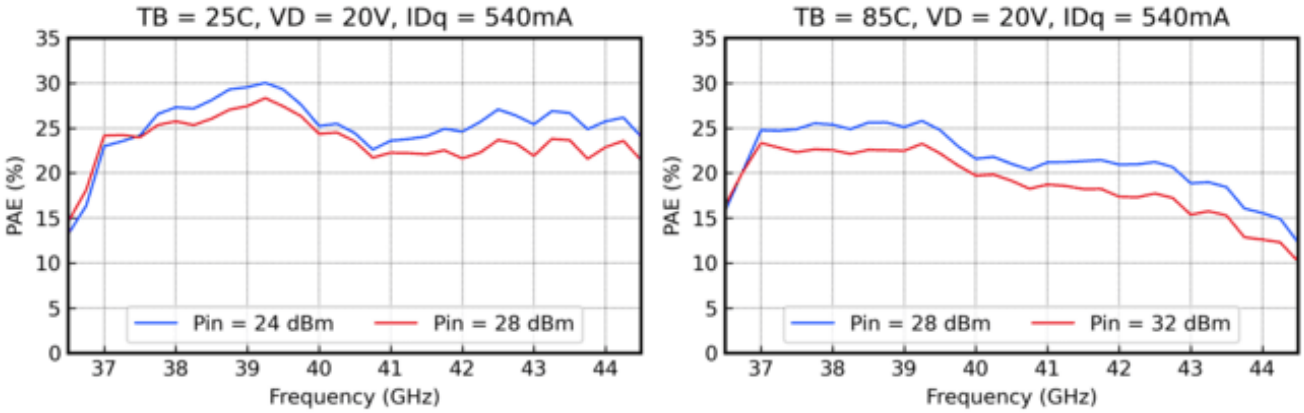
**Performance versus frequency and temperature**

**Test conditions** : $V_D$ = 20V, $I_{dq}$ = 540mA, TB = 25°C / 85°C

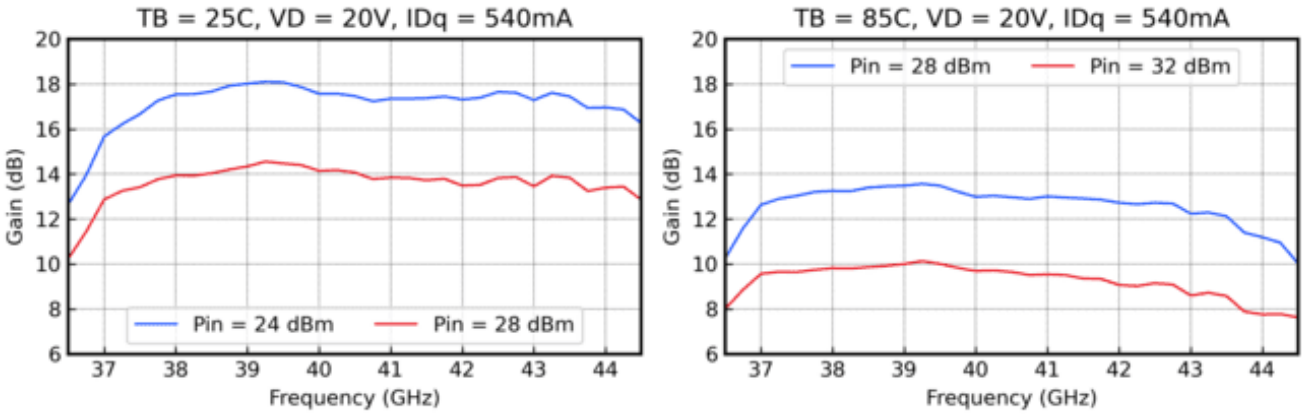
### Output Power versus Frequency and Input Power




### Power Added Efficiency versus Frequency and Input Power




### Gain versus Frequency and Input Power



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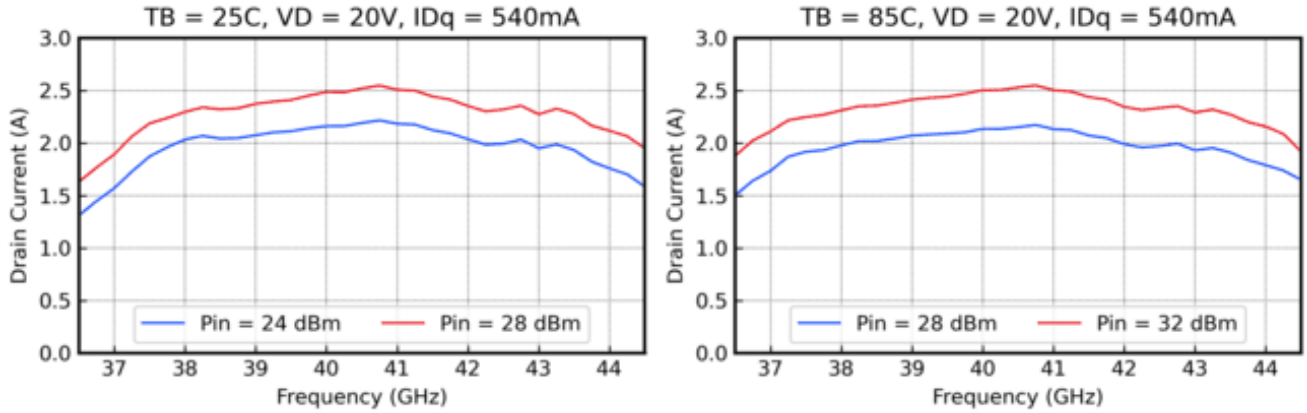
## Typical Board Measurements : Large Signal Performance

Measurements reference plane is de-embedded at the wire-bondings planes of the RF lines.

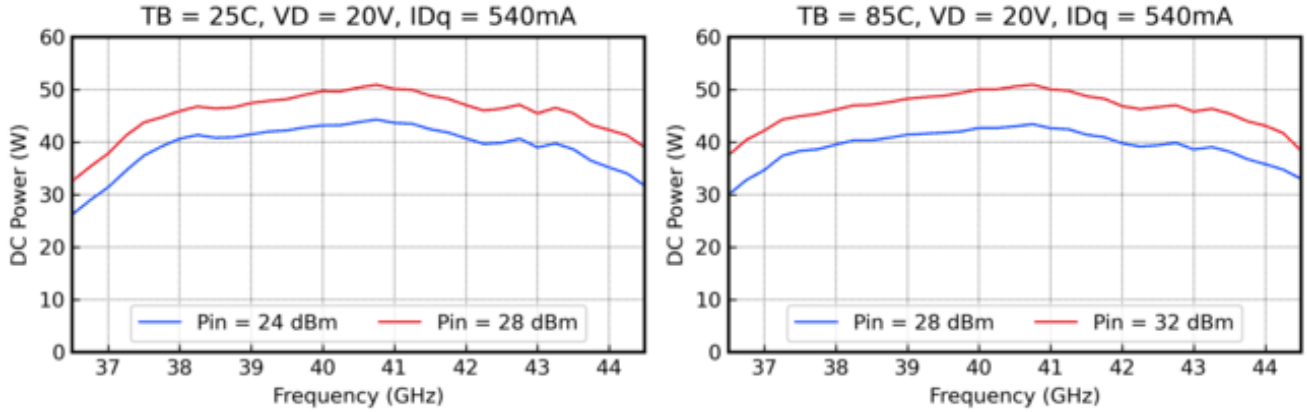
**Performance versus frequency and temperature**

**Test conditions** : $V_D$ = 20V, $I_{dq}$ = 540mA, TB = 25°C / 85°C, Pin chosen at max PAE and Psat

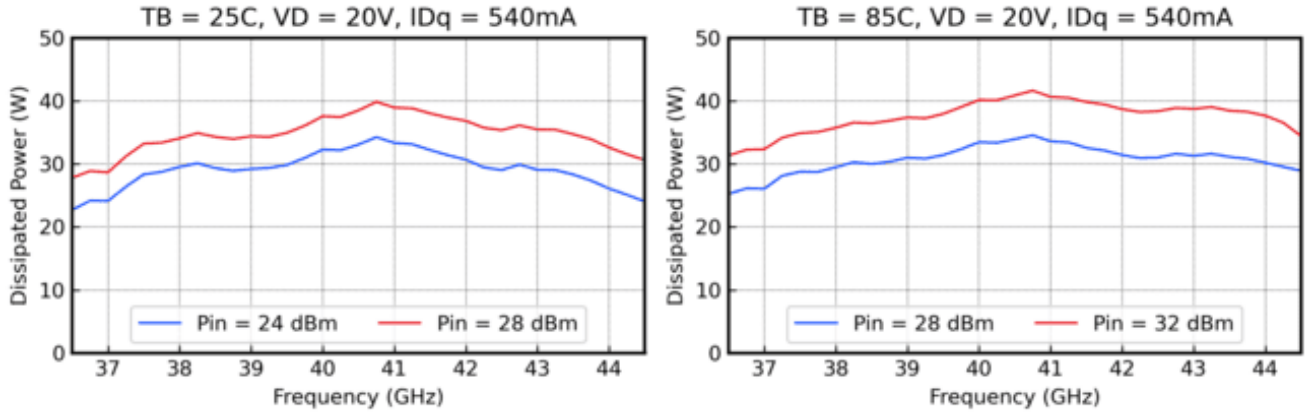
### Drain Current versus Frequency and Input Power




### DC Power Consumption versus Frequency and Input Power




### Dissipated Power versus Frequency and Input Power



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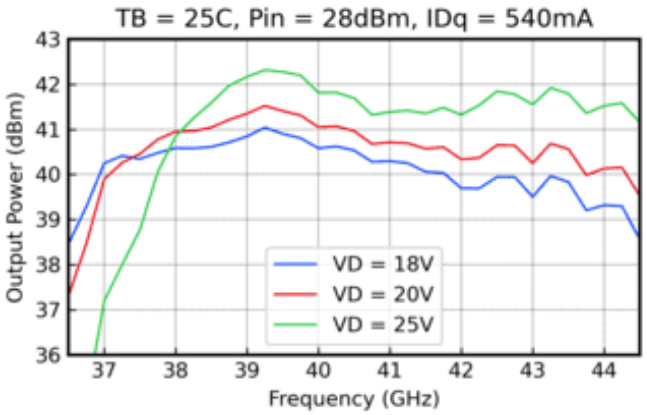
## Typical Board Measurements : Large Signal Performance

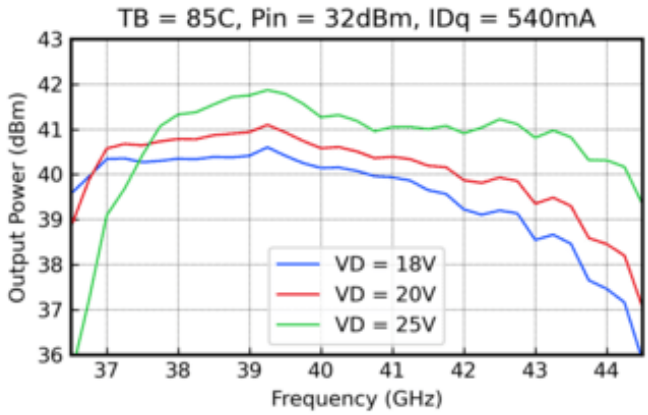
Measurements reference plane is de-embedded at the wire-bondings planes of the RF lines.

**Performance versus frequency and temperature**

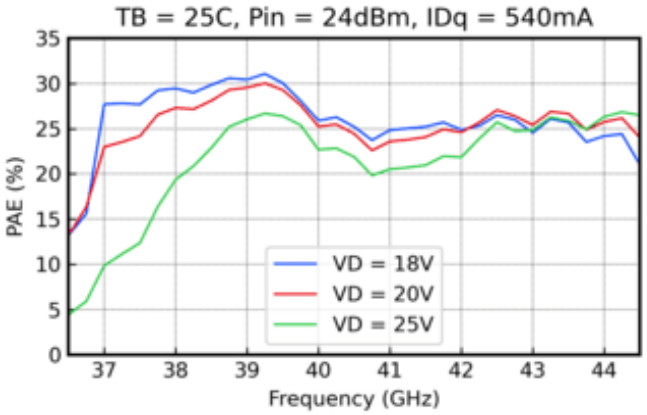
**Test conditions** : $I_{dq}$ = 540mA, TB = 25°C / 85°C

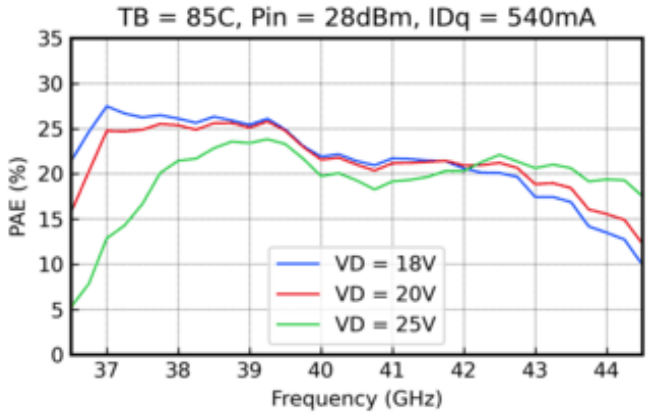
### Output Power versus Frequency and Drain Voltage, Pin at Psat



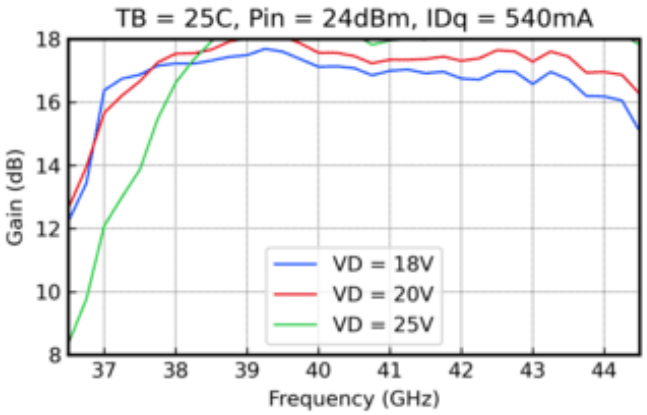



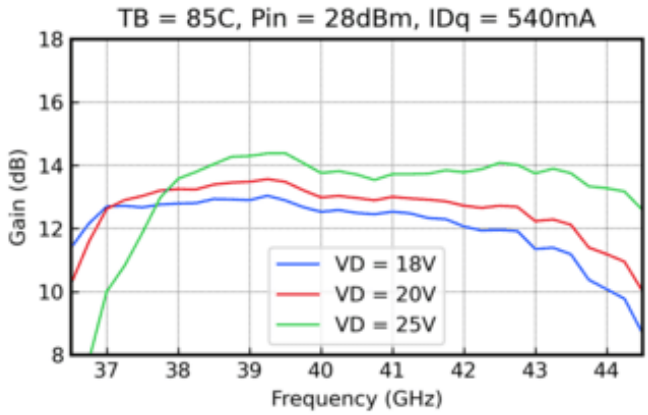

### Power Added Efficiency versus Frequency and Drain Voltage, Pin at max PAE




### Gain versus Frequency and Drain Voltage, Pin at max PAE



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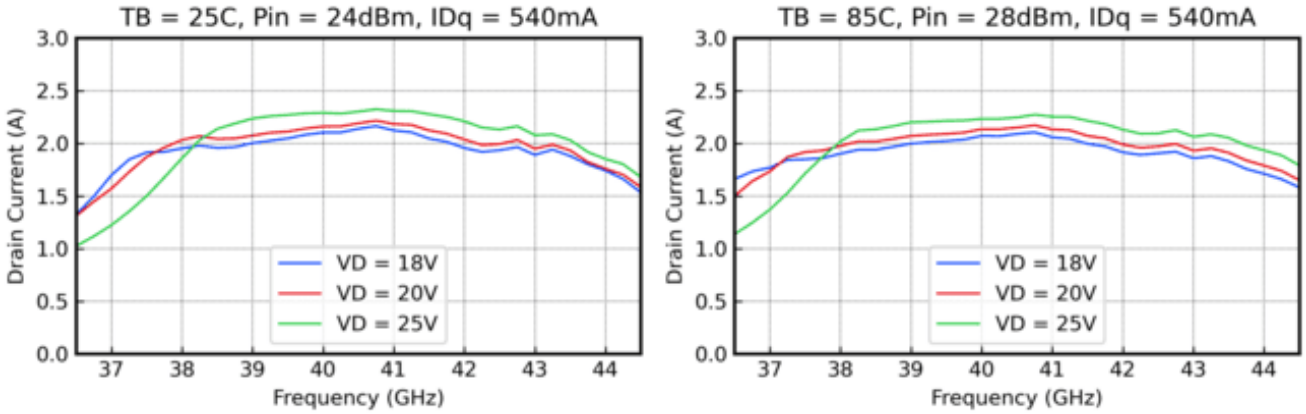
## Typical Board Measurements : Large Signal Performance

Measurements reference plane is de-embedded at the wire-bondings planes of the RF lines.

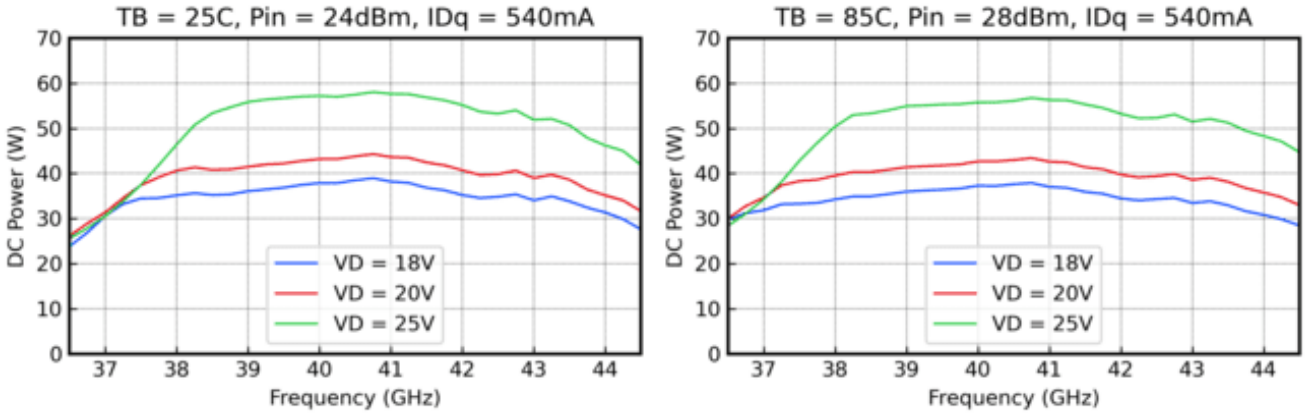
**Performance versus frequency and temperature**

**Test conditions** : $I_{dq}$ = 540mA, TB = 25°C / 85°C

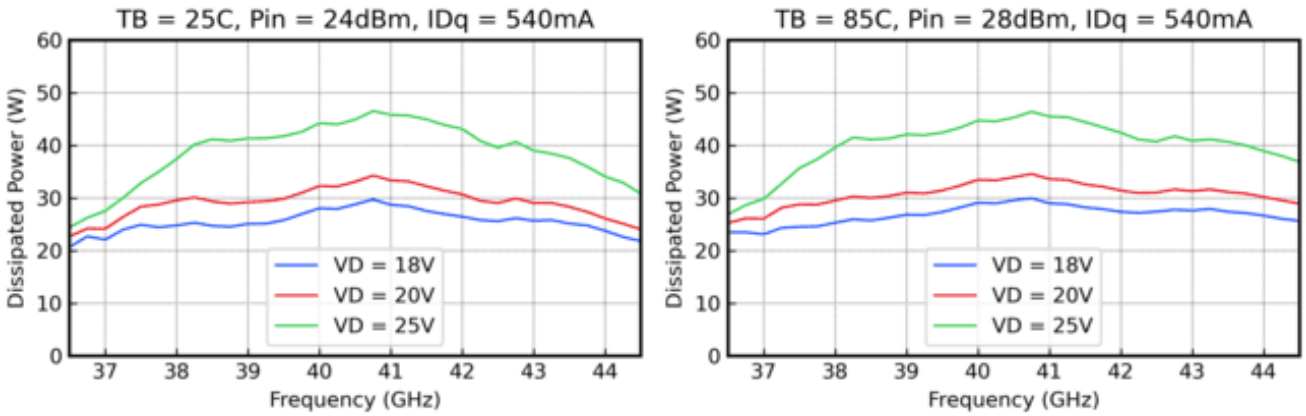
### Drain Current versus Frequency and Drain Voltage, Pin at max PAE




### DC Power Consumption versus Frequency and Drain Voltage, Pin at max PAE




### Dissipated Power versus Frequency and Drain Voltage, Pin at max PAE



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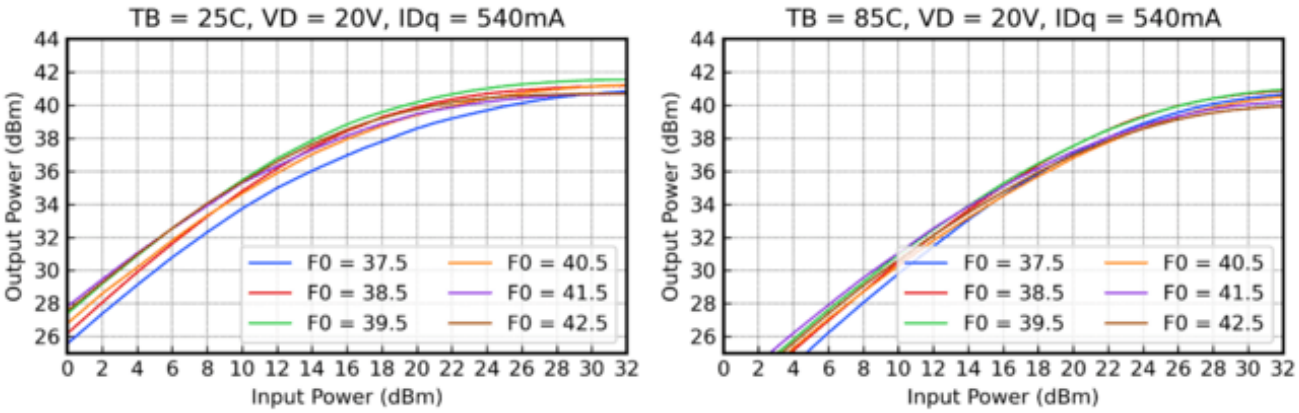
## Typical Board Measurements : Large Signal Performance

Measurements reference plane is de-embedded at the wire-bondings planes of the RF lines.

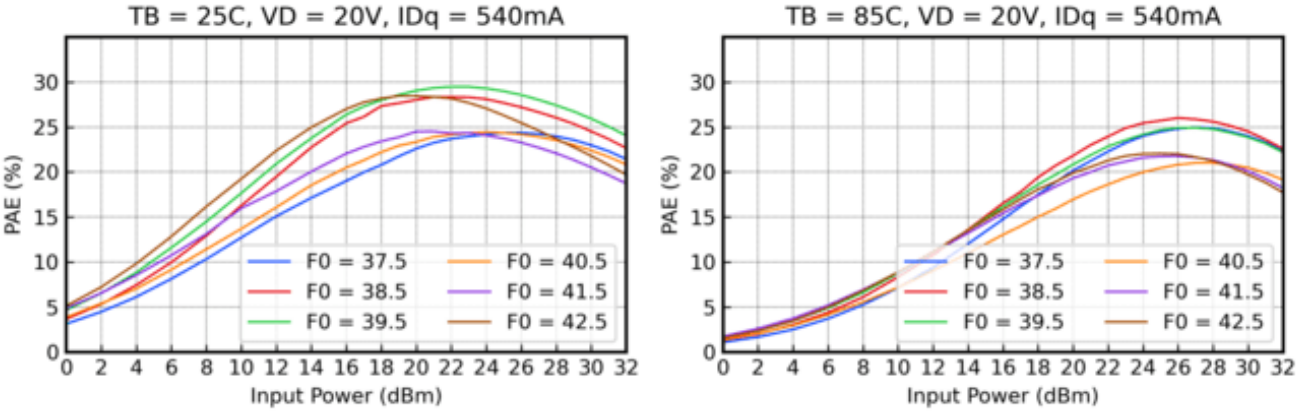
**Performance versus frequency and temperature**

**Test conditions** : $I_{dq}$ = 540mA, TB = 25°C / 85°C

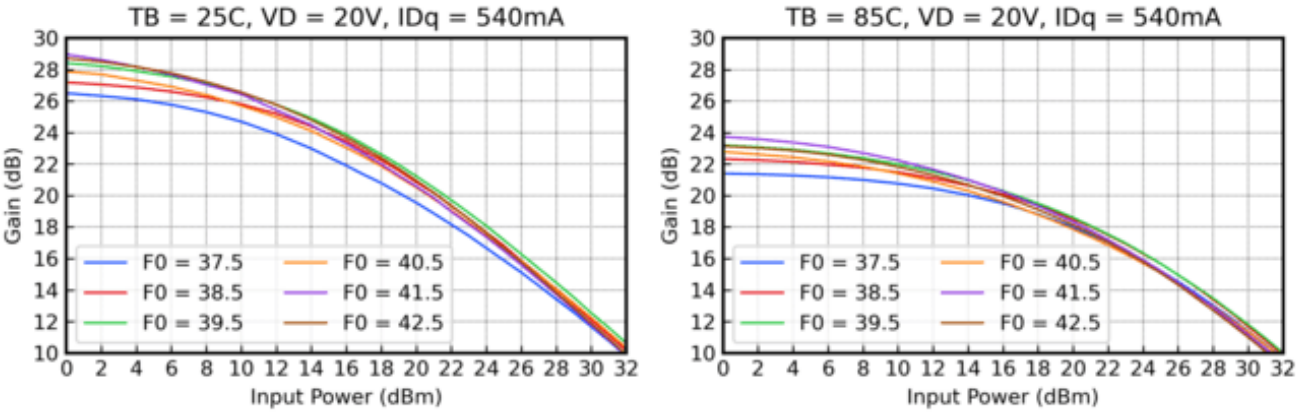
### Output Power versus Input Power and Frequency




### Power Added Efficiency versus Input Power and Frequency




### Gain versus Input Power and Frequency



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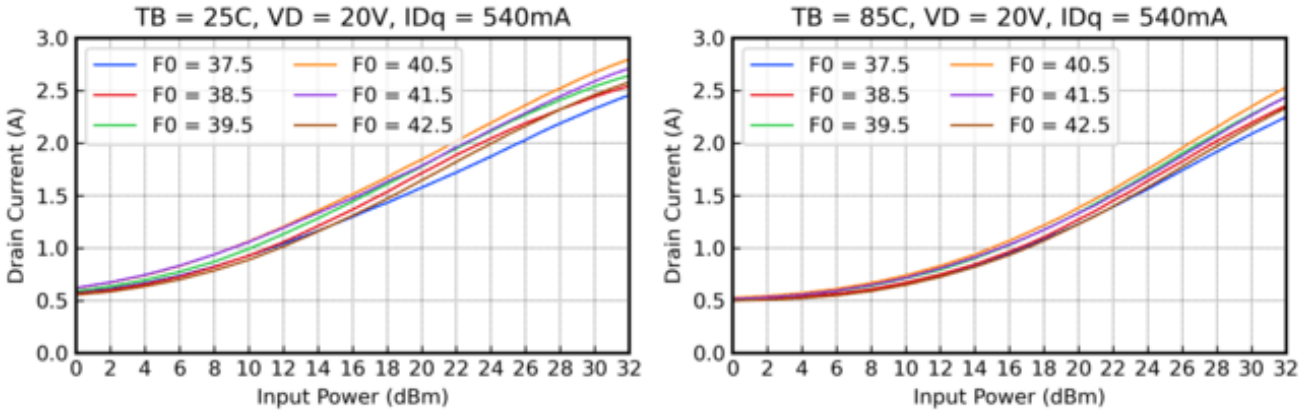
## Typical Board Measurements : Large Signal Performance

Measurements reference plane is de-embedded at the wire-bondings planes of the RF lines.

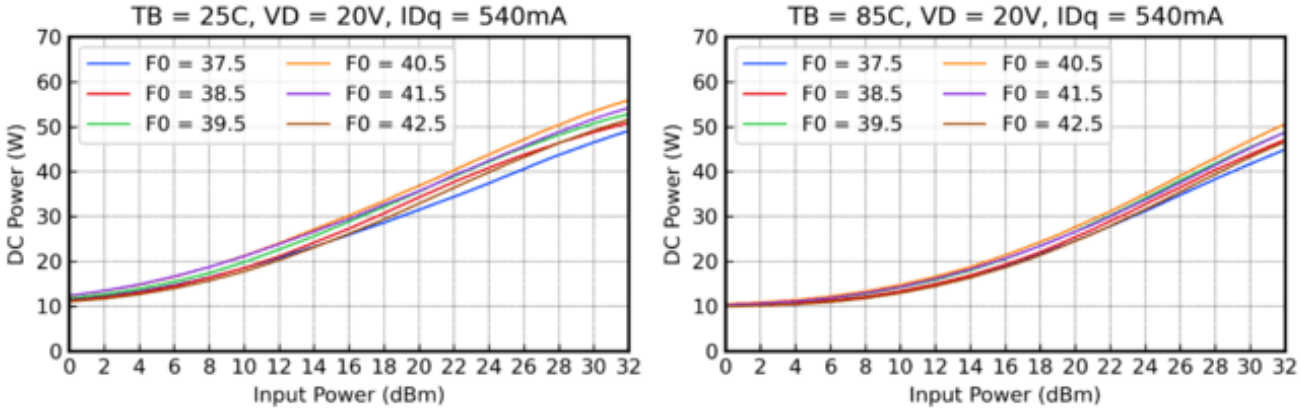
**Performance versus frequency and temperature**

**Test conditions** : $I_{dq}$ = 540mA, TB = 25°C / 85°C

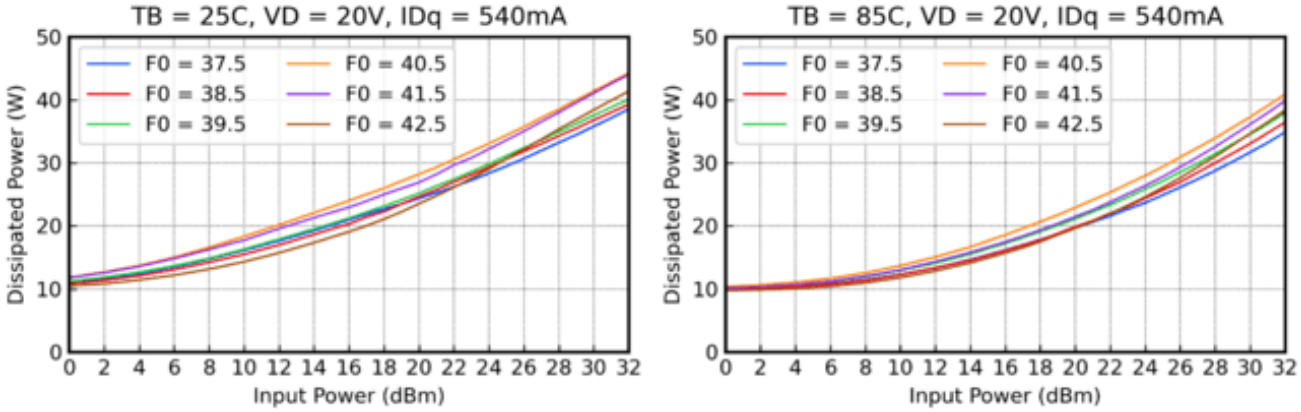
### Drain Current versus Input Power and Frequency




### DC Power Consumption versus Input Power and Frequency




### Dissipated Power versus Input Power and Frequency



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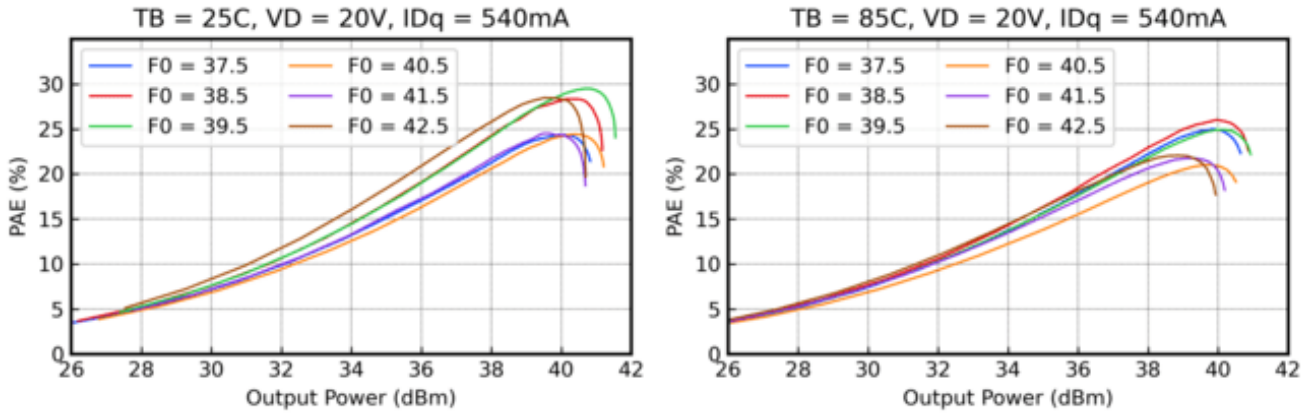
## Typical Board Measurements : Large Signal Performance

Measurements reference plane is de-embedded at the wire-bondings planes of the RF lines.

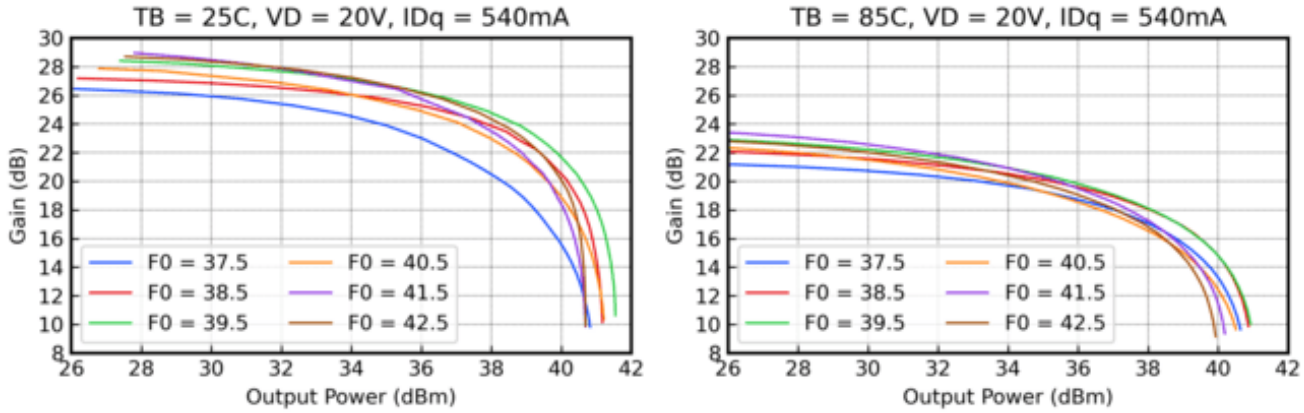
**Performance versus frequency and temperature**

**Test conditions** : $I_{dq}$ = 540mA, TB = 25°C / 85°C

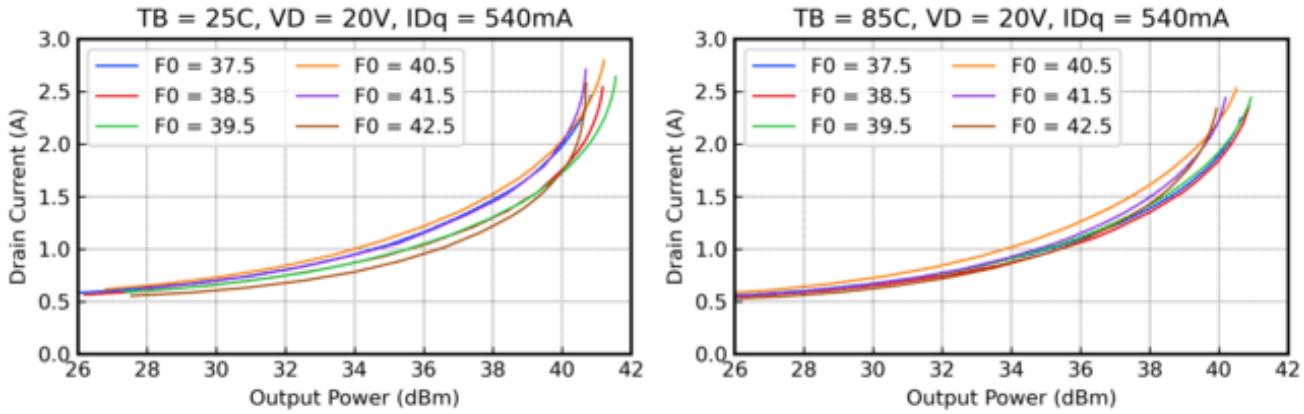
### Power Added Efficiency versus Output Power and Frequency




### Gain versus Output Power and Frequency




### Drain Current versus Output Power and Frequency



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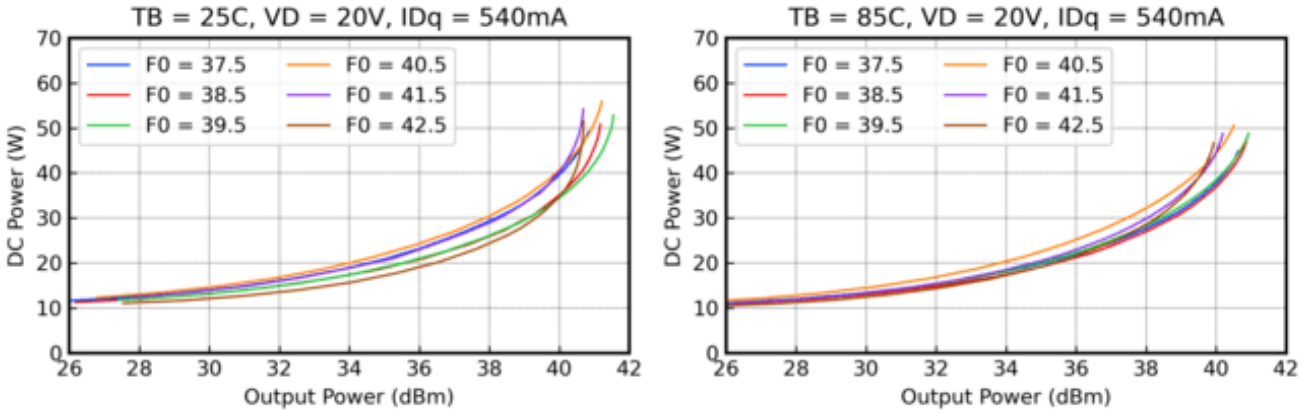
## Typical Board Measurements : Large Signal Performance

Measurements reference plane is de-embedded at the wire-bondings planes of the RF lines.

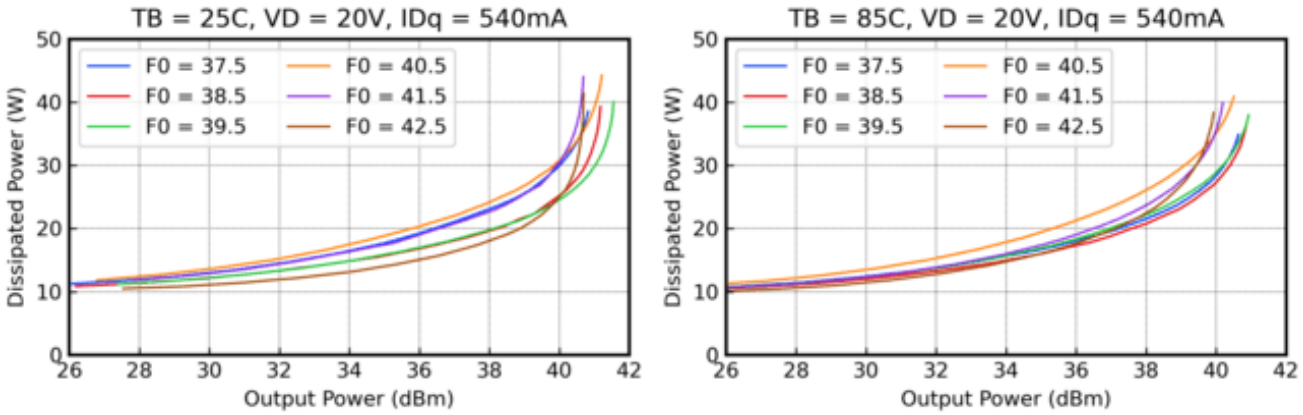
**Performance versus frequency and temperature**

**Test conditions** : VD = 20V, $I_{dq}$ = 540mA, TB = 25°C / 85°C

### DC Power Consumption versus Output Power and Frequency




### Dissipated Power versus Output Power and Frequency



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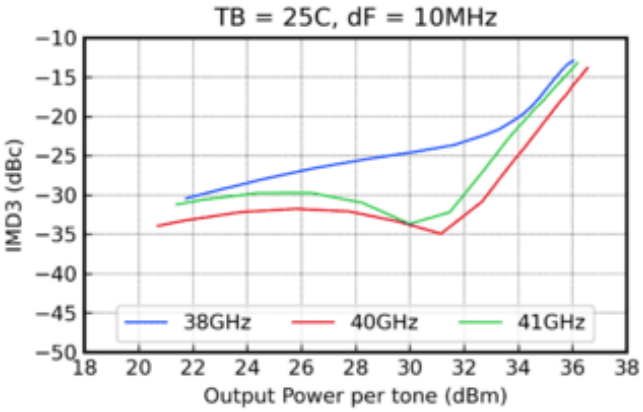
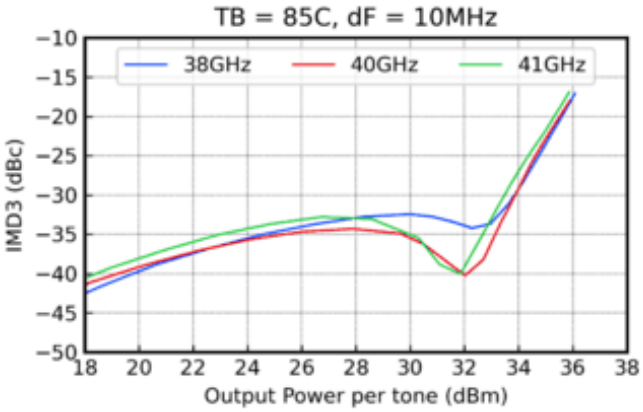
## Typical Board Measurements : Two Tone Large Signal Performance

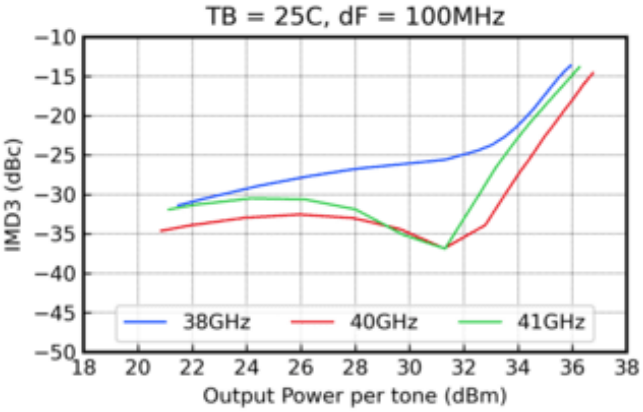
Measurements reference plane is de-embedded at the wire-bondings planes of the RF lines.

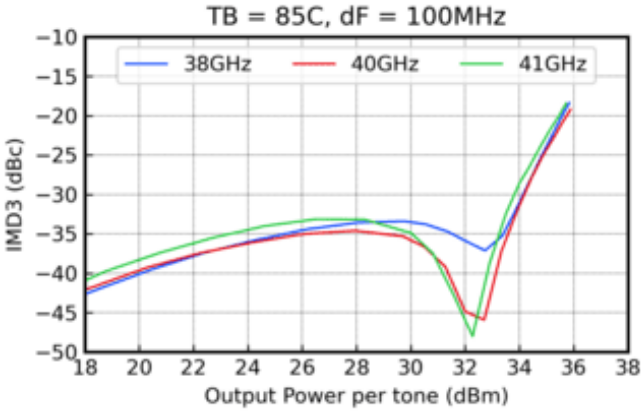
**IMD3 versus Output Power and Central Frequency**

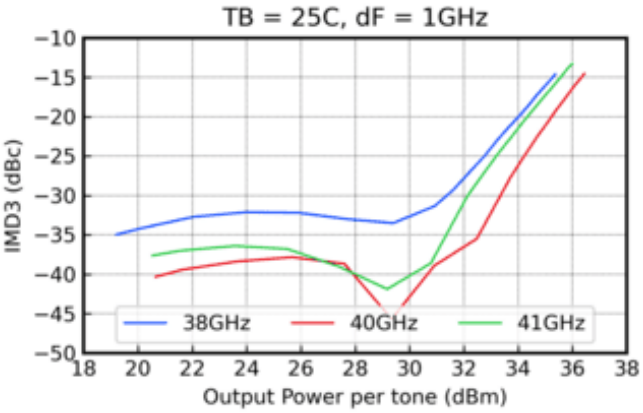
**Test conditions** : VD = 20V, TB = 25°C & IDq = 230mA, TB = 85°C & IDq = 310mA

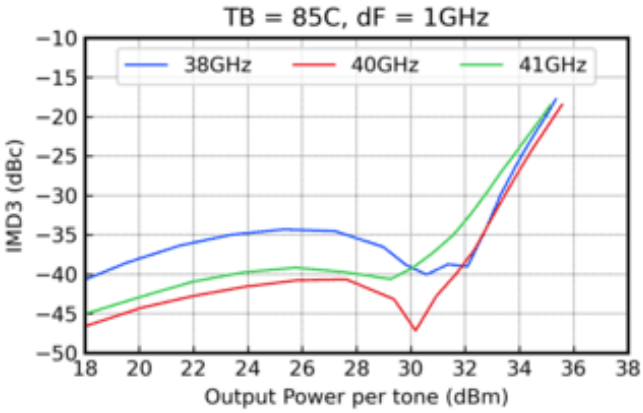


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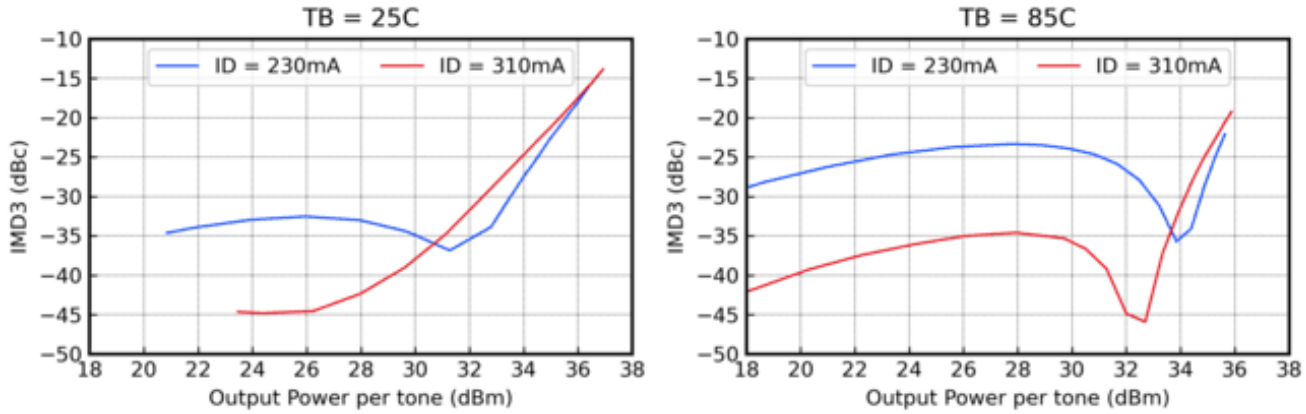
## Typical Board Measurements : Two Tone Large Signal Performance

Measurements reference plane is de-embedded at the wire-bondings planes of the RF lines.

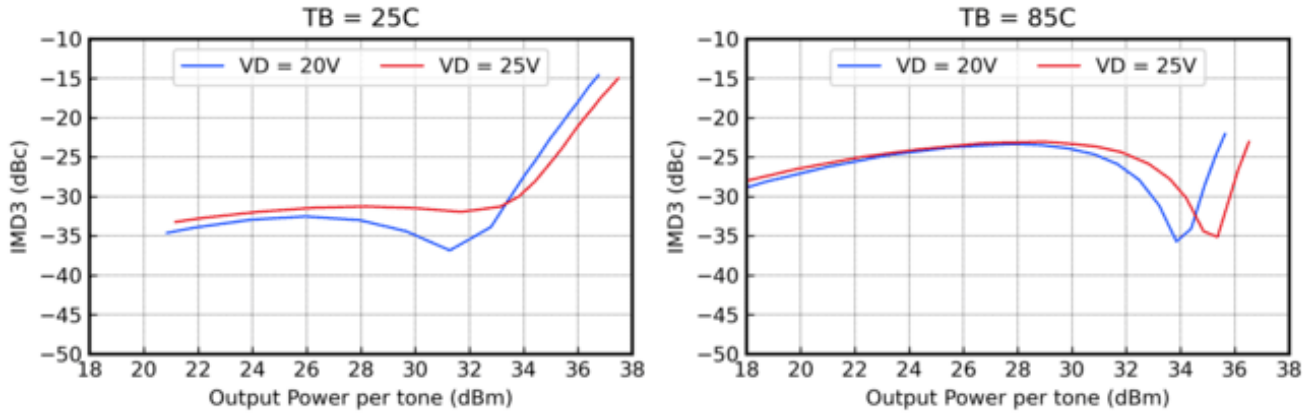
**IMD3 versus Output Power and Quiescent Current**

**Test conditions** : F0 = 40GHz, VD = 20V, TB = 25°/85°C, Tone spacing : 100MHz



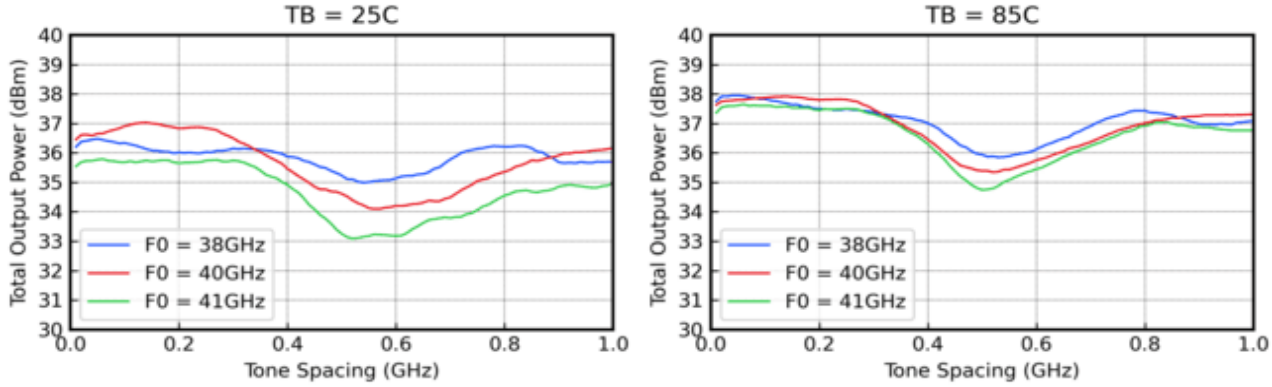

**IMD3 versus Output Power and Drain Voltage**

**Test conditions** : F0 = 40GHz, IDq = 230mA, TB = 25°/85°C , Tone spacing : 100MHz




**Total Output Power at -23dBc IMD3 versus Tone Spacing and Central Frequency**

**Test conditions** : VD = 20V, IDq = 230mA, TB = 25°/85°C, IMD3 = -23dBc



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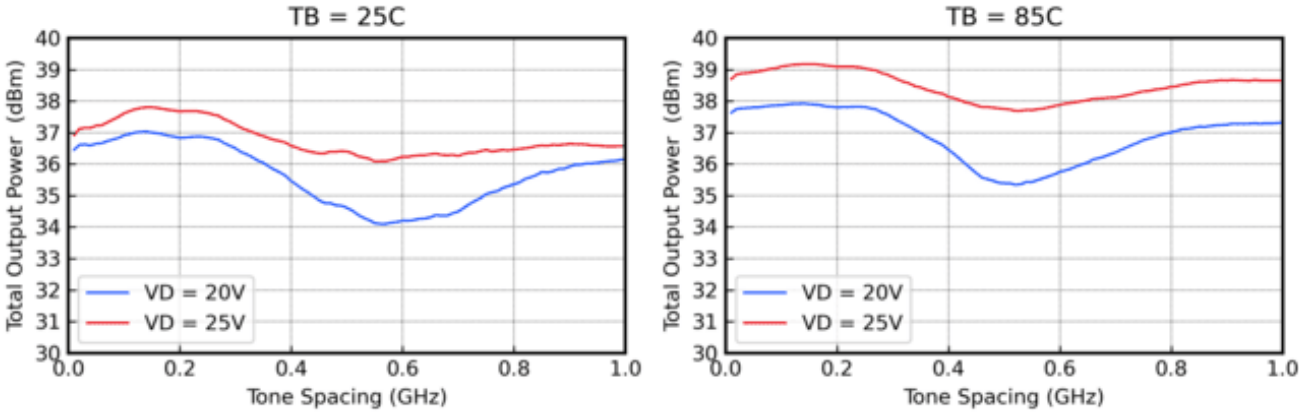
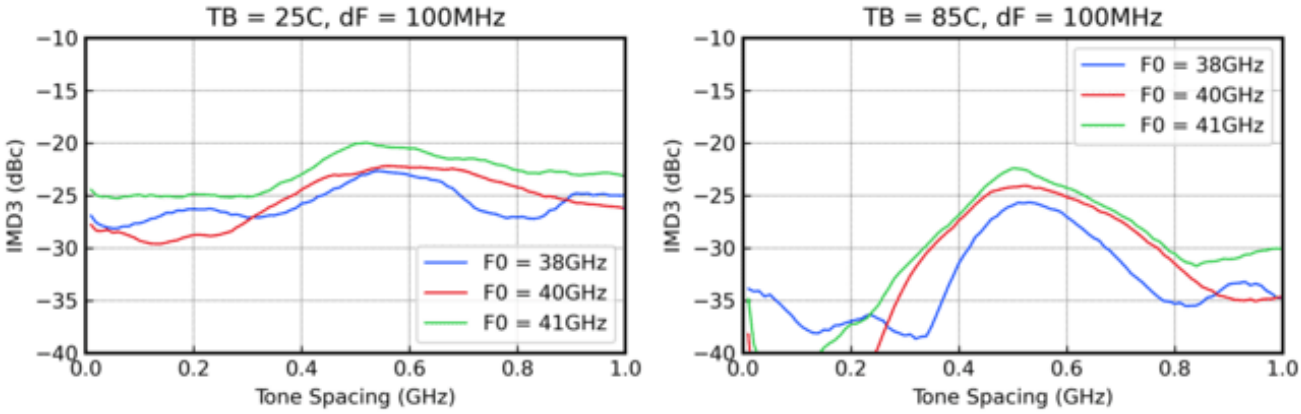
## Typical Board Measurements : Two Tone Large Signal Performance

Measurements reference plane is de-embedded at the wire-bondings planes of the RF lines.

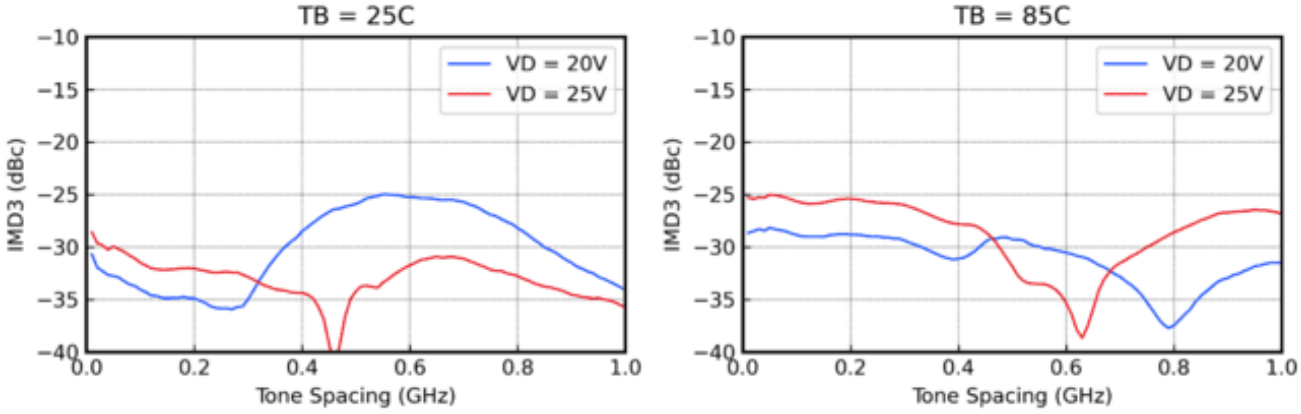
**Total Output Power at -23dBc IMD3 versus Tone Spacing and Drain Voltage**
**Test conditions** : F0 = 40GHz, $I_{dq}$ = 230mA, TB = 25°/85°C, IMD3 = -23dBc




**IMD3 at 36dBm Total Output Power, versus Tone Spacing and Central Frequency**
**Test conditions** : $I_{dq}$ = 230mA, VD = 20V, TB = 25°/85°C




**IMD3 at 36dBm Total Output Power, versus Tone Spacing and Drain Voltage**
**Test conditions** : F0 = 40GHz, $I_{dq}$ = 230mA, TB = 25°/85°C



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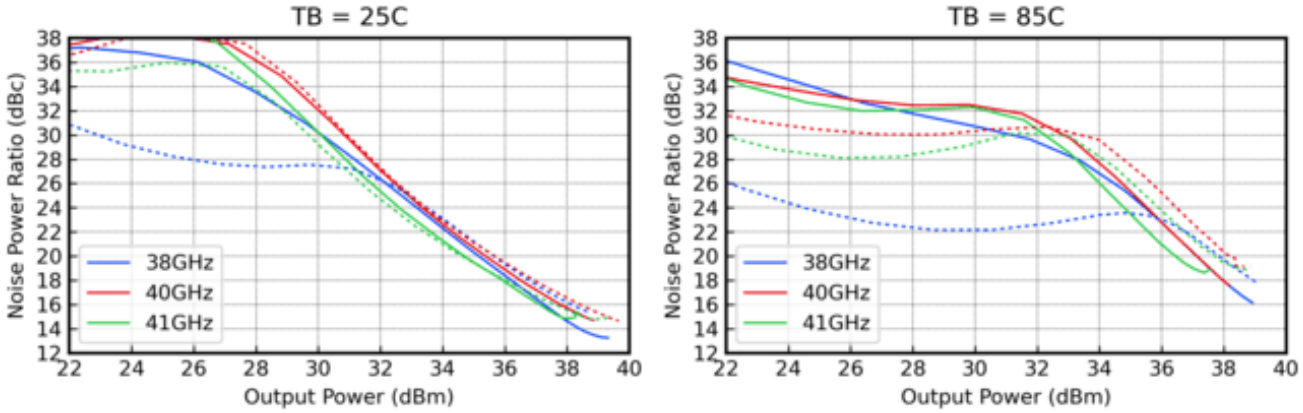
## Typical Board Measurements : Noise Power Ratio

### NPR Signal : 40MHz Signal Banwidth, 10% Notch

Measurements reference plane is de-embedded at the wire-bondings planes of the RF lines.

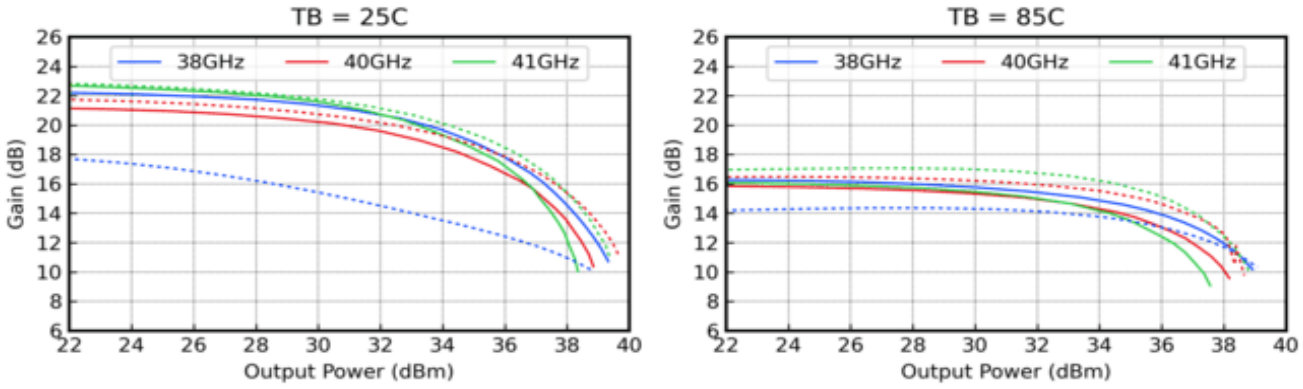
**NPR versus Output Power and Central Frequency**

**Test conditions** : $I_{dq}$ = 310mA, TB = 25°/85°C, solid line VD = 20V, dashed line VD = 25V



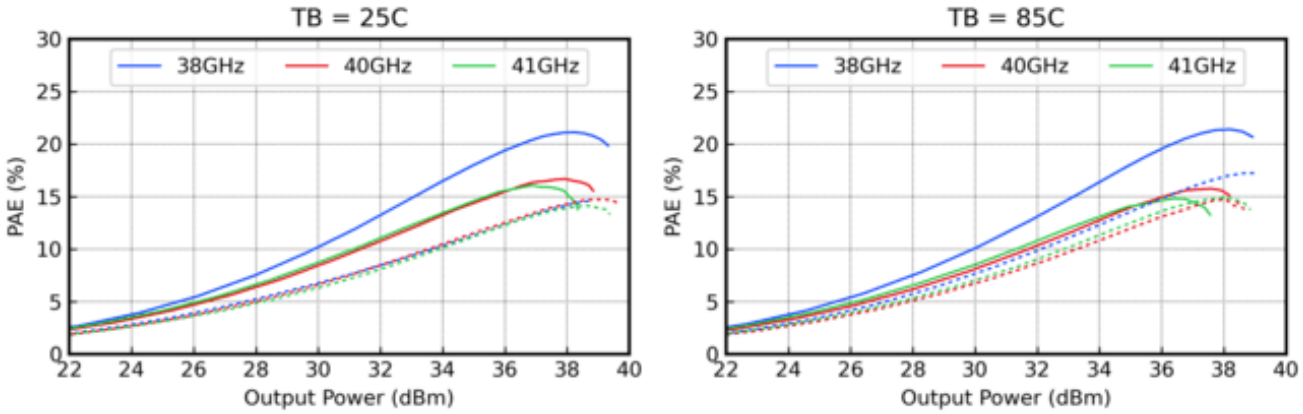

**Gain versus Output Power and Central Frequency**

**Test conditions** : $I_{dq}$ = 310mA, TB = 25°/85°C, solid line VD = 20V, dashed line VD = 25V




**PAE versus Output Power and Central Frequency**

**Test conditions** : $I_{dq}$ = 310mA, TB = 25°/85°C, solid line VD = 20V, dashed line VD = 25V



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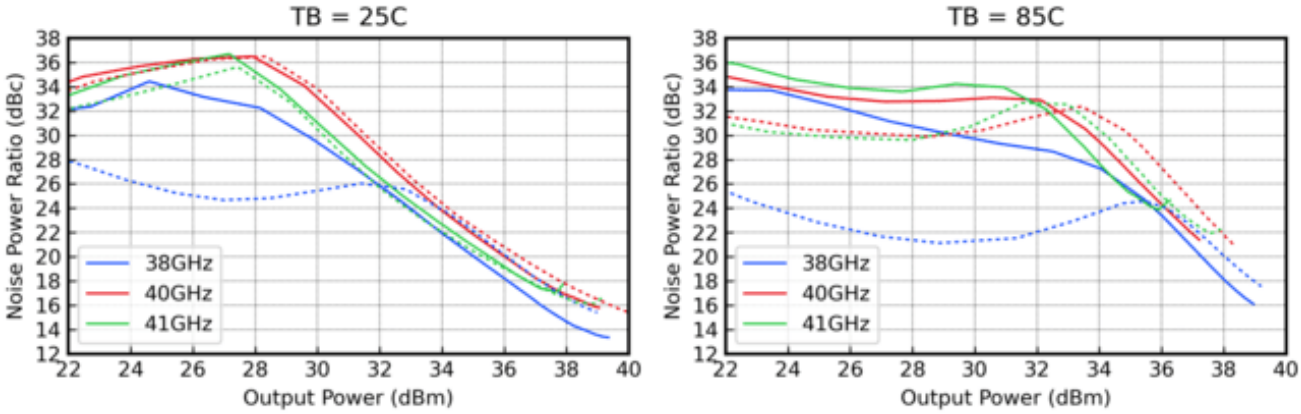
## Typical Board Measurements : Noise Power Ratio

### NPR Signal : 1GHz Signal Banwidth, 10% Notch

Measurements reference plane is de-embedded at the wire-bondings planes of the RF lines.

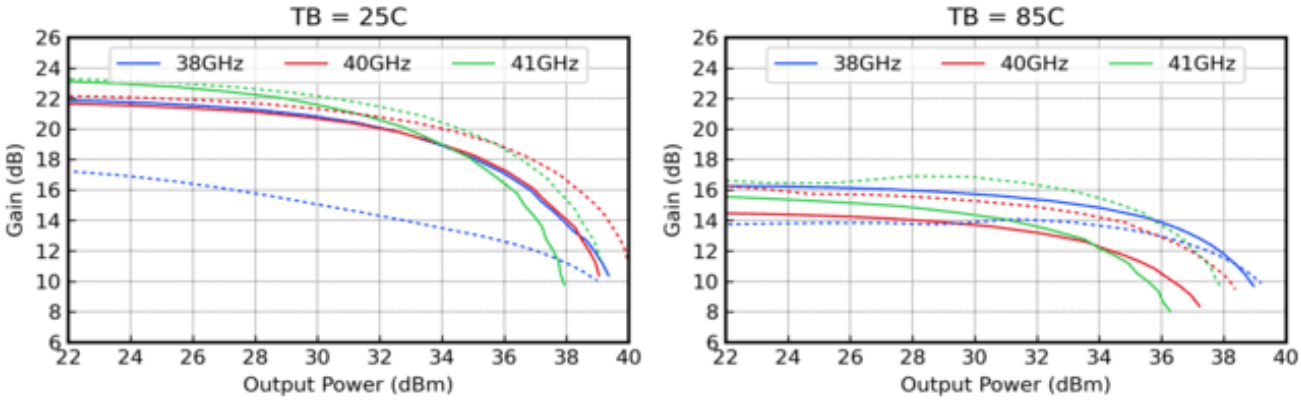
**NPR versus Output Power and Central Frequency**

**Test conditions** : $I_{dq}$ = 310mA, TB = 25°/85°C, solid line VD = 20V, dashed line VD = 25V



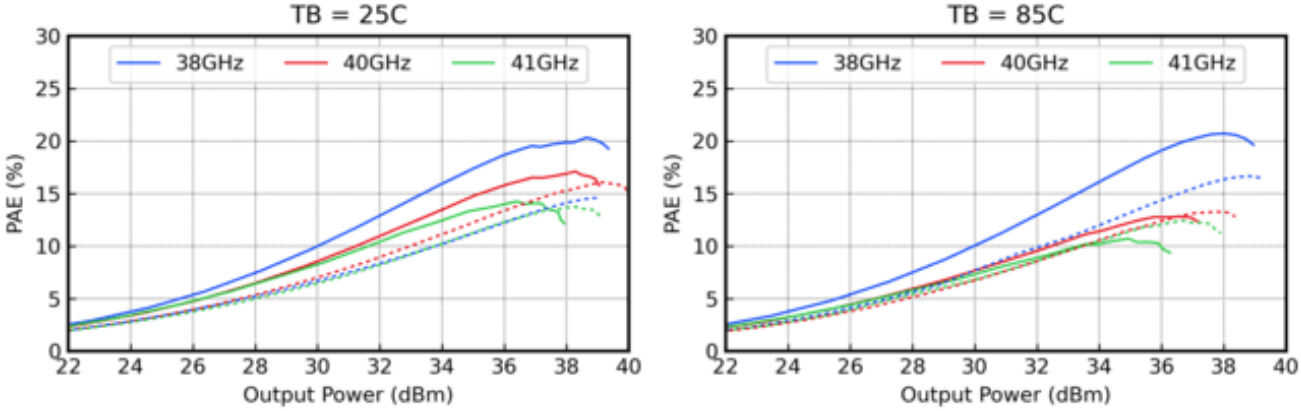

**Gain versus Output Power and Central Frequency**

**Test conditions** : $I_{dq}$ = 310mA, TB = 25°/85°C, solid line VD = 20V, dashed line VD = 25V




**PAE versus Output Power and Central Frequency**

**Test conditions** : $I_{dq}$ = 310mA, TB = 25°/85°C, solid line VD = 20V, dashed line VD = 25V



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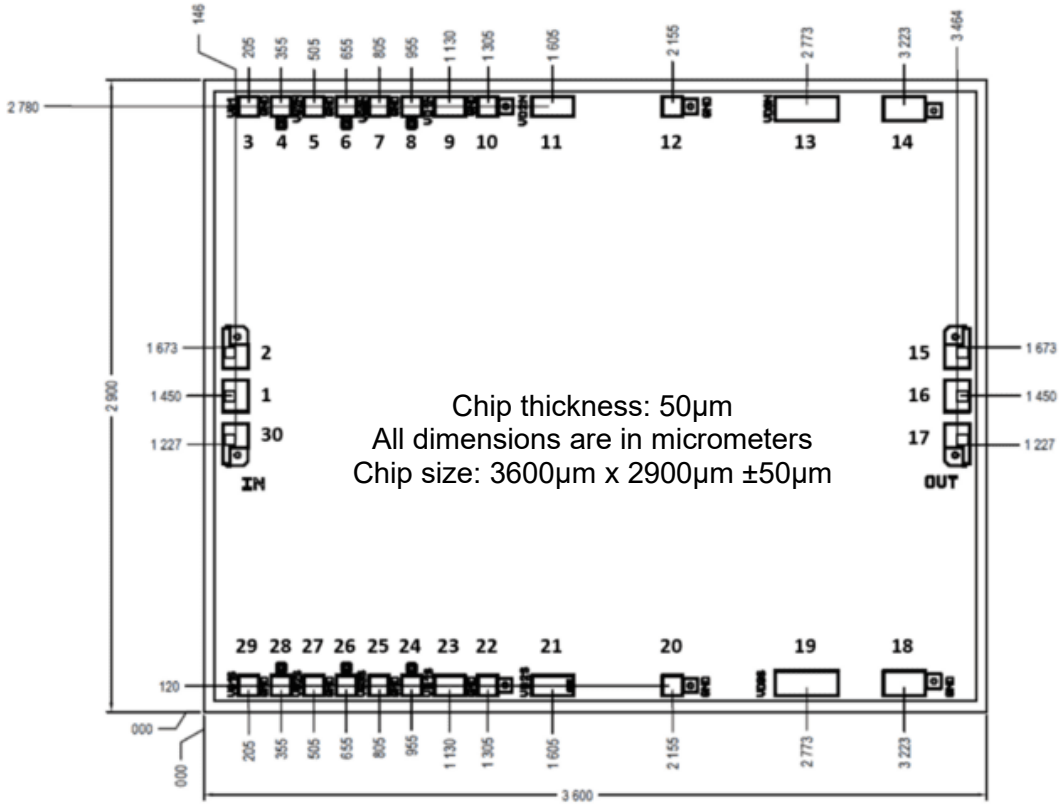
## Mechanical Data




| PAD Number | Name | Description | Pad size |
|---|---|---|---|
| 1 | RF IN | Input RF port | 118µm x 210µm |
| 3 | G12 | DC Gaite voltage, 1st stage, North | 96µm x 96µm |
| 5 | G3 | DC Gate voltage 2d stage, North | 96µm x 96µm |
| 7 | G4 | DC Gate voltage 3d stage, North | 96µm x 96µm |
| 9 | D12 | DC Drain voltage, 1st stage, North | 196µm x 96µm |
| 11 | D3 | DC Drain voltage 2d stage, North | 196µm x 96µm |
| 13 | D4 | DC Drain voltage 3d stage, North | 296µm x 116µm |
| 16 | RF OUT | Output RF port | 118 µm x210 µm |
| 19 | D4 | DC Drain voltage 3d stage, South | 296µm x 116µm |
| 21 | D3 | DC Drain voltage 2d stage, South | 196µm x 96µm |
| 23 | D12 | DC Drain voltage, 1st stage, South | 196µm x 96µm |
| 25 | G4 | DC Gate voltage 3d stage, South | 96µm x 96µm |
| 27 | G3 | DC Gate voltage 2d stage, South | 96µm x 96µm |
| 29 | G12 | DC Gaite voltage, 1st stage, South | 96µm x 96µm |
| 2,4,6,8,10,12,14 ,15,17,18,20,22, 24,26,28,30 | GND | Ground | 96µm x 96µm |



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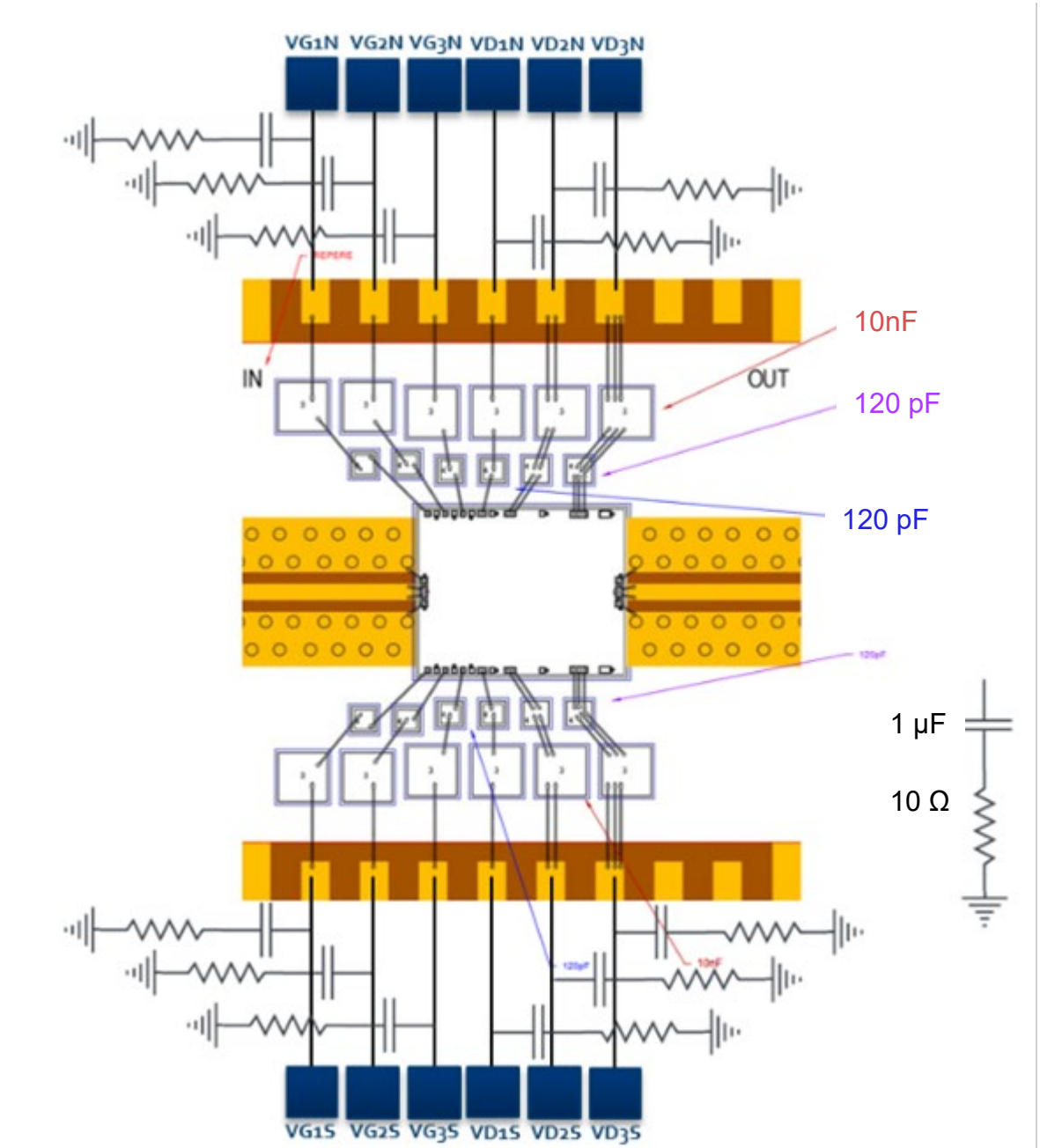
## Recommended Assembly Plan




3 levels of decoupling capacitor have been used, 2 on the tab and 1 on the board. The first level is composed of 120 pF chip capacitors, the second level is composed of 10nF chip capacitors, the third level is composed of 1µF SMD 1210 capacitors with 10Ω series resistance. The first two levels should be as close as possible to the die.



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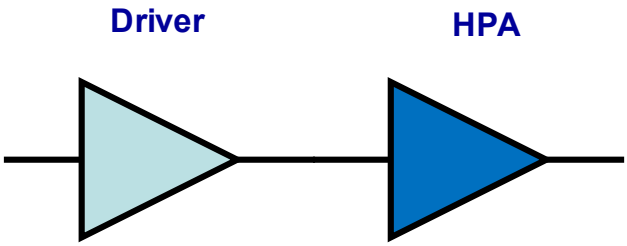
## Recommended UMS Power chain

The CHA8454-99F is recommended with the CHA5659-98F as driver, with a total small signal gain above 45dB. For more information about the CHA5659-98F, see our website www.ums-rf.com




| Reference | CHA5659-98F | CHA8454-99F |
|---|---|---|
| Frequency | 36-44GHz | 37.5-43.5GHz |
| Gain | 22dB | 24 |
| Psat | 30dBm(1) | 40dBm |
| Drain Voltage | 6V | 20V |
| Quiescent Current | 0.8A | 0.56A |

(1) Referring to the P1dB for the CHA5659-98F.



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## Notes



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## ESD Sensitivity

| Parameter | Classification | Standard |
|---|---|---|
| Human Body Model (HBM) | 1A | ANSI/ESDA/JEDEC - JS-001 |

## Recommended reflow process assembly

Refer to the application note AN0001 available at https://www.ums-rf.com for die attach.

## Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at https://www.ums-rf.com.

## Recommended ESD management

Refer to the application note AN0020 available at https://www.ums-rf.com for ESD sensitivity and handling recommendations for the UMS products.

## Ordering Information

Chip form : CHA8454-99F/00





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