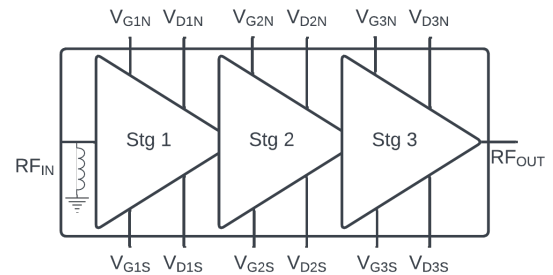


26.5-31GHz 25W High Power Amplifier

GaN Monolithic Microwave IC

Description

The CHA8362-99F is a three stage High Power Amplifier operating between 26.5 and 31GHz and providing typically 25W of saturated output power associated to 30% of Power Added Efficiency. This amplifier exhibits 40dBm linear power with -33dBc ACPR & 19dBc NPR with 25% PAE. It also provides more than 25dB small signal gain. This HPA is dedicated to SatCom and 5G applications and well suited for a wide range of microwave applications and systems. The circuit is manufactured on a robust GaN-on-SiC HEMT process and is available in bare die form. Input & output are 50Ω matched.

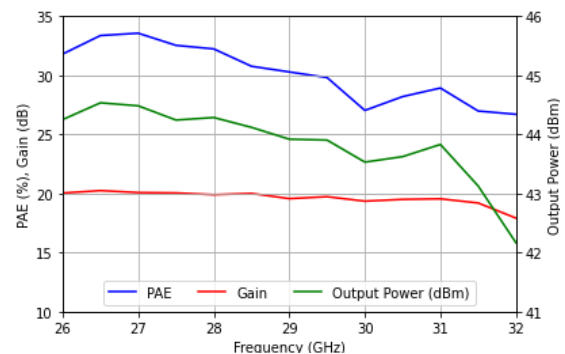


Main Features

- Frequency range: 26.5 – 31GHz
- High output power: 25W
- High PAE: 30%
- ACPR = -33dBc at 40dBm Average Pout⁽¹⁾
- Linear Gain: 25dB
- DC bias: VD = 25V & Idq = 440mA
- Chip size: 3.6 x 3.6mm²
- Available in bare die form

⁽¹⁾ 100MHz modulation bandwidth, 256QAM

VD = 25V, Idq = 440mA, TBS = 25°C, Pin = 25dBm



Main Electrical Characteristics

TBS = 25°C (TBS: chip backside temperature)

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	26.5		31	GHz
Gain	Linear Gain		25		dB
Pout	Output Power @ Pin=25dBm		44		dBm
ACPR	ACPR @ Pout = 40dBm with 256QAM modulation (BW=100MHz)		-33		dBc
NPR	Noise Power Ratio @ Pout = 40dBm (BW=45MHz)		19		dBc
PAE	Power Added Efficiency @ Pin = 25dBm		30		%

Specifications

$T_{BS} = +25^{\circ}\text{C}$, $V_d = +25\text{V}$, CW excitation

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	26.5		31	GHz
Gain	Linear Gain		25		dB
Pout	Output Power @ $P_{in} = 25\text{dBm}$ (P_{sat})		44		dBm
PAE	Power Added Efficiency		30		%
I_d	Drain current at saturation		3.5		A
S11	Input Return Loss		-9		dB
S22	Output return loss		-12		dB
I_{dq}	Quiescent current		440		mA
V_d	Drain Voltage		25		V

These values are representative of on-board measurements as defined on the drawing in paragraph "Evaluation mother board".

Absolute Maximum Ratings ⁽¹⁾

$T_{BS} = +25^{\circ}\text{C}$

Symbol	Parameter	Values	Unit
V_d	Drain bias voltage	27	V
I_d	Quiescent Drain bias current	1000	mA
V_g	Gate bias voltage	-7 to -1	V
P_{in}	Maximum Input Power	30	dBm

⁽¹⁾ Operation of this device above any one of these parameters may cause permanent damage

Recommended Operating Range ^{(2), (3)}

Symbol	Parameter	Values	Unit
V_d	Drain bias voltage	18 to 25	V
I_d	Drain bias current	300 to 700	mA
V_g	Gate bias voltage	-3.5 to -2.5	V
P_{in}	Maximum Input Power	25	dBm
T_j	Maximum Junction temperature ⁽⁴⁾	200	$^{\circ}\text{C}$

⁽²⁾ Electrical performances are defined for specified test conditions

⁽³⁾ Electrical performances are not guaranteed over all recommended operating conditions

⁽⁴⁾ See Device thermal performances section.

Temperature Range

T_{BS}	Operating temperature range	-40 to +95	$^{\circ}\text{C}$
T_{stg}	Storage temperature range	-55 to +150	$^{\circ}\text{C}$

Typical Bias Conditions $T_{BS} = 25^{\circ}\text{C}$

Symbol	Pad N°	Parameter	Values	Unit
V_G	4, 8, 11, 23, 26, 30	Gate voltage tuned for $I_{dq} = 440\text{mA}$	-3	V
V_D	6, 10, 14, 20, 24, 28	Drain voltage	25	V

“Power ON” sequence

1. Bias HPA gate voltage at V_g close to $V_{\text{pinch-off}}$ (Typically: $V_G \approx -5$)
2. Apply V_D bias voltage (Typically: $V_D = 25\text{V}$)
3. Increase gate voltage V_g up to quiescent bias drain current I_{dq}
4. Apply RF signal

“Power OFF” sequence

1. Turn off RF signal
2. Bias HPA gate voltage at V_g close to $V_{\text{pinch-off}}$ (Typically: $V_G \approx -5\text{V}$)
3. Check that quiescent bias drain current I_{dq} is close to 0mA
4. Turn V_D bias voltage to 0V
5. Check that quiescent bias drain current I_{dq} is close to 0mA
6. Turn V_G bias voltage to 0V

Device thermal performances

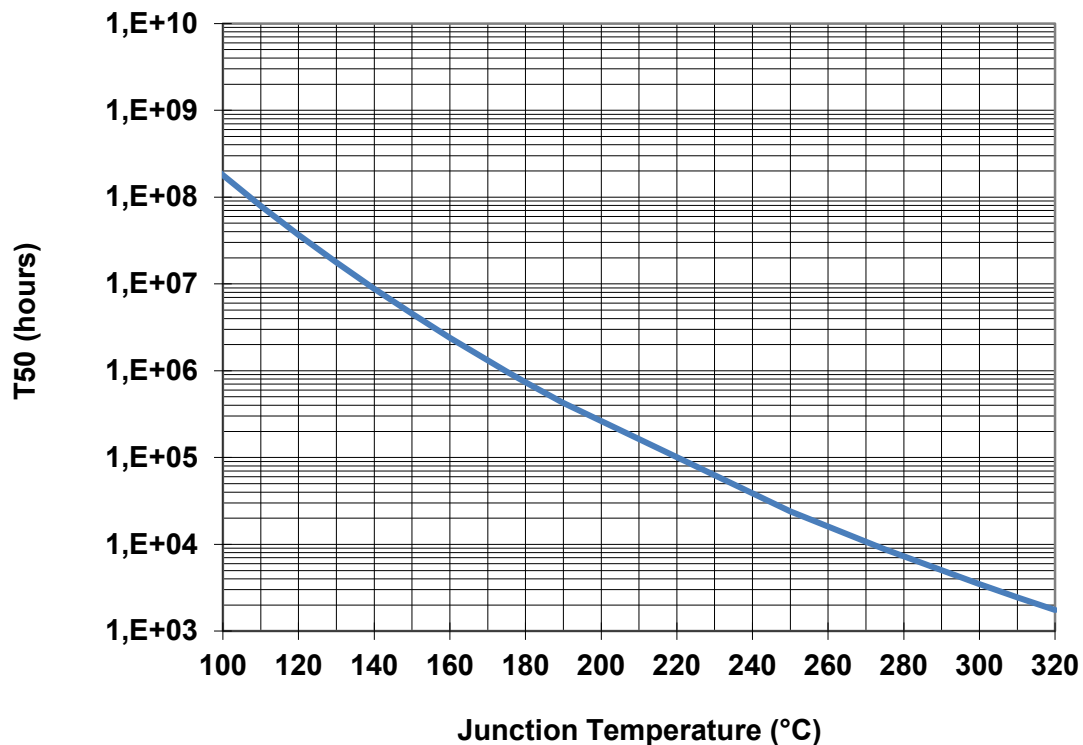
The device thermal performances below are based on UMS rules to evaluate the junction temperature.

This same procedure is the basis for junction temperature evaluation of the samples used to derive the Median lifetime and activation energy for the particular technology on which the CHA8362-99F is manufactured (GaN HEMT 0.15 μ m).

The temperature T_{BS} is defined as the chip backside temperature. The thermal resistance (R_{th_eq}), given in the following table, is for the full circuit in CW mode.

Thermal Resistance ⁽¹⁾	R_{th_eq}	$T_{BS} = 25^{\circ}\text{C}$, $V_d = 25\text{V}$, $I_{dq} = 440\text{ mA}$, $P_{in} = 26\text{ dBm}$, $Freq = 29\text{GHz}$, $P_{diss} = 56\text{ W}$	1.27	$^{\circ}\text{C/W}$
Junction Temperature	T_j		95	$^{\circ}\text{C}$
Median Life	T50		>2E8	Hrs
Thermal Resistance ⁽¹⁾	R_{th_eq}	$T_{BS} = 85^{\circ}\text{C}$, $V_d = 25\text{V}$, $I_{dq} = 440\text{ mA}$, $P_{in} = 26\text{ dBm}$, $Freq = 29\text{GHz}$, $P_{diss} = 54\text{ W}$	1.71	$^{\circ}\text{C/W}$
Junction Temperature	T_j		184	$^{\circ}\text{C}$
Median Life	T50		5.9E5	Hrs

⁽¹⁾ Thermal resistance measured at the backside of the chip

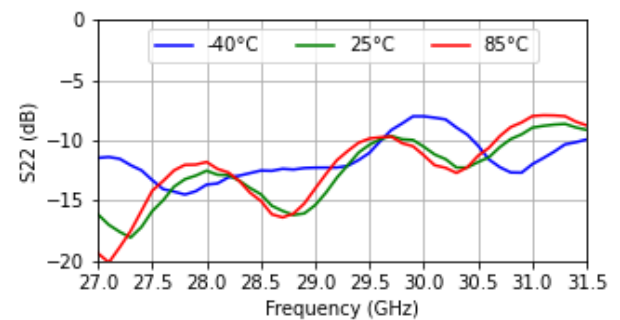
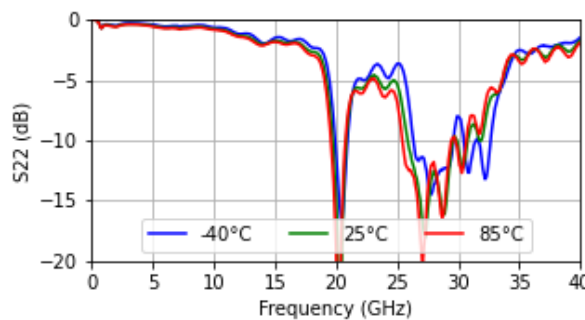
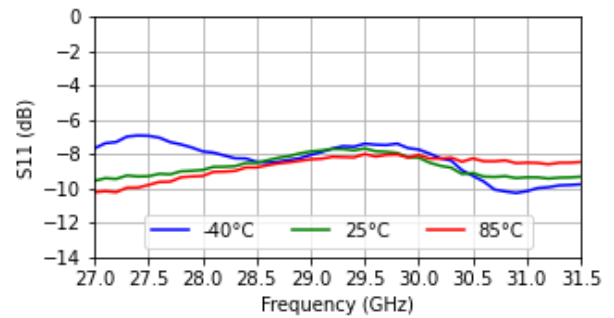
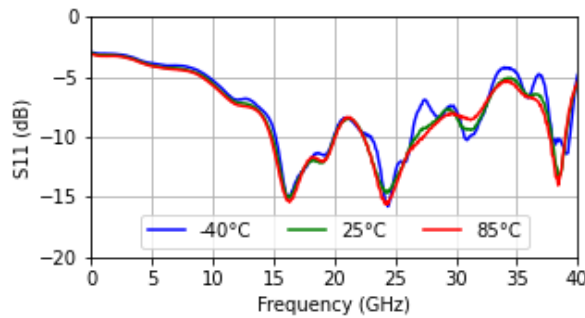
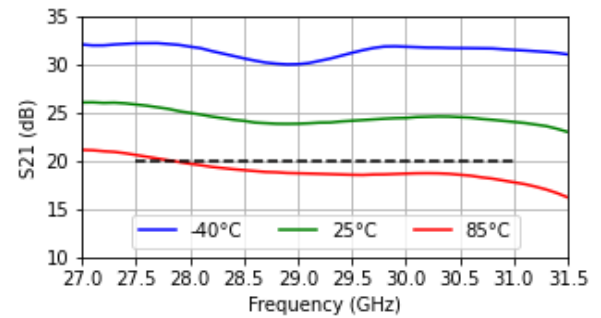
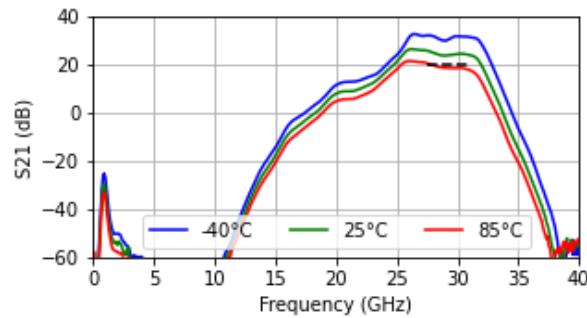


Typical Board Measurements: Small Signal Performances

Performance versus temperature

Test conditions : CW, $V_D = 25V$, $I_{DQ} = 440mA$, $T_{BS} = -40^{\circ}C / 25^{\circ}C / 85^{\circ}C$

Measurements reference planes are de-embedded at the wire bondings plane on the RF feed line.

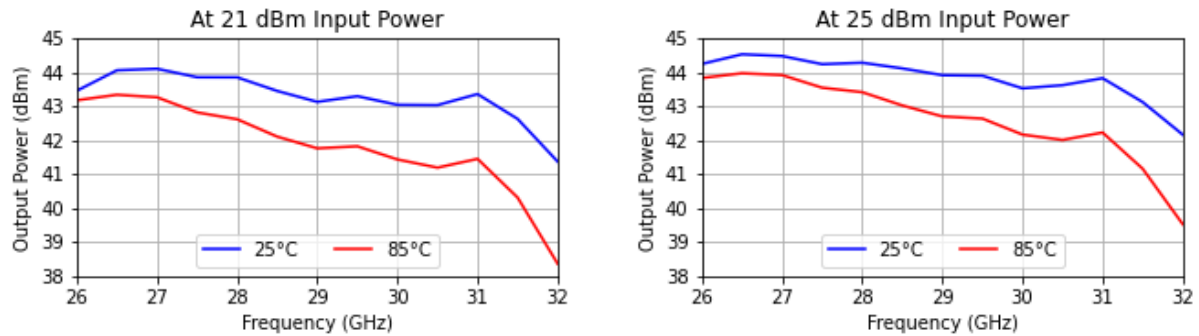


Typical Board Measurements: Large Signal Performances

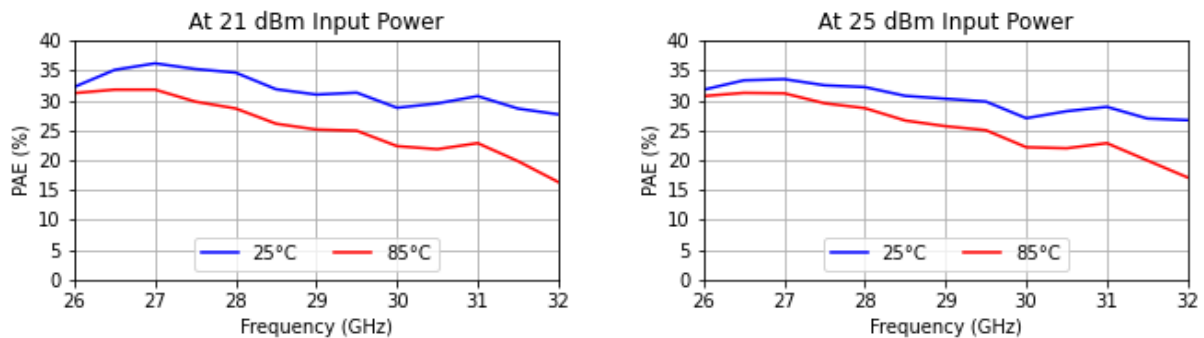
Performance versus frequency and temperature

Test conditions : CW, $V_D = 25V$, $I_{DQ} = 440mA$, $T_{BS} = 25^\circ C / 85^\circ C$

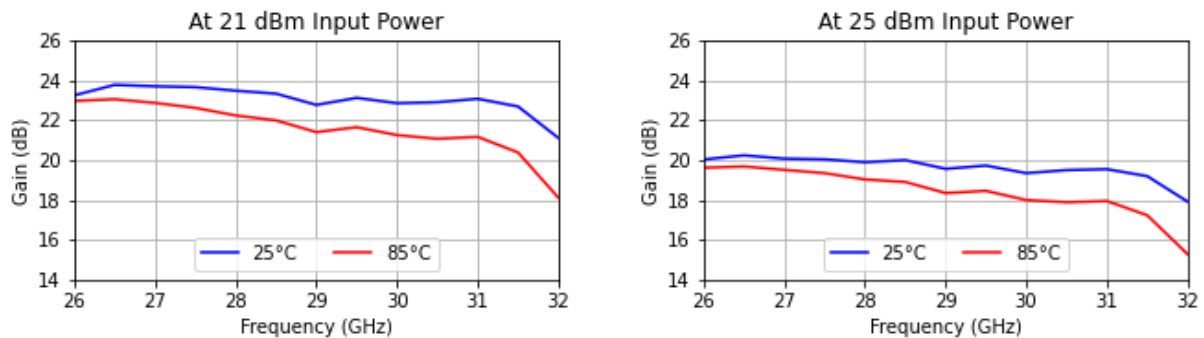
Output Power vs. Frequency & Chip Backside Temperature



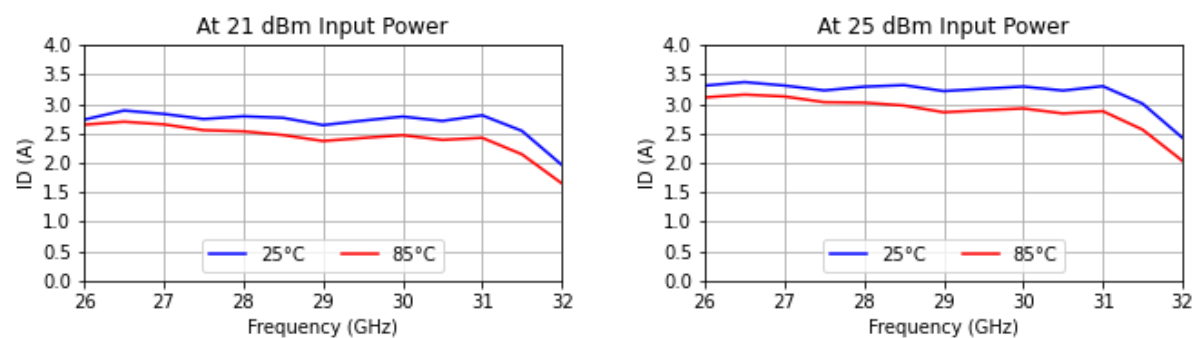
Power Added Efficiency vs. Frequency & Chip Backside Temperature

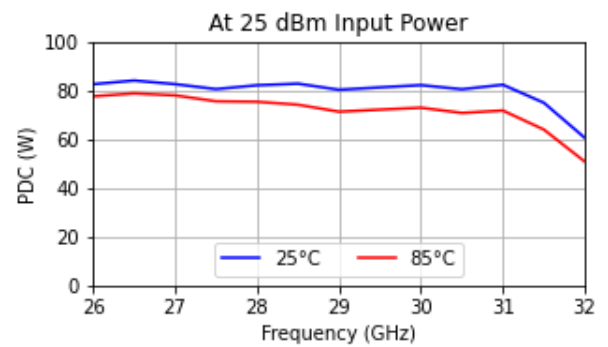
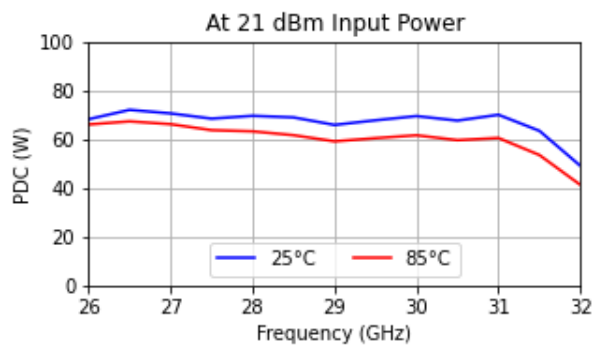
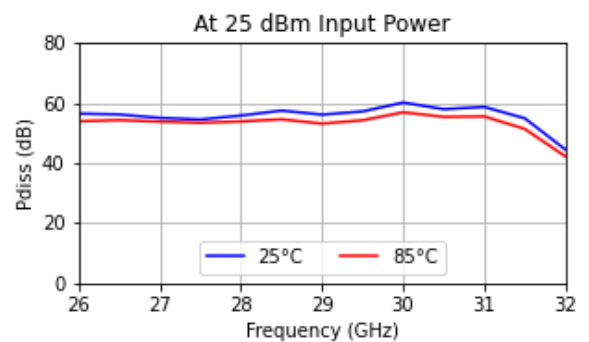
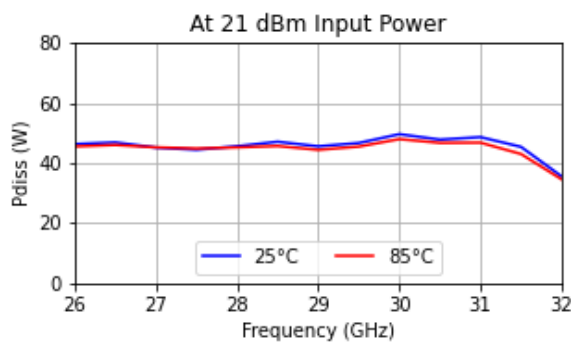


Gain vs. Frequency & Chip Backside Temperature



DC Drain current vs. Frequency & Chip Backside Temperature



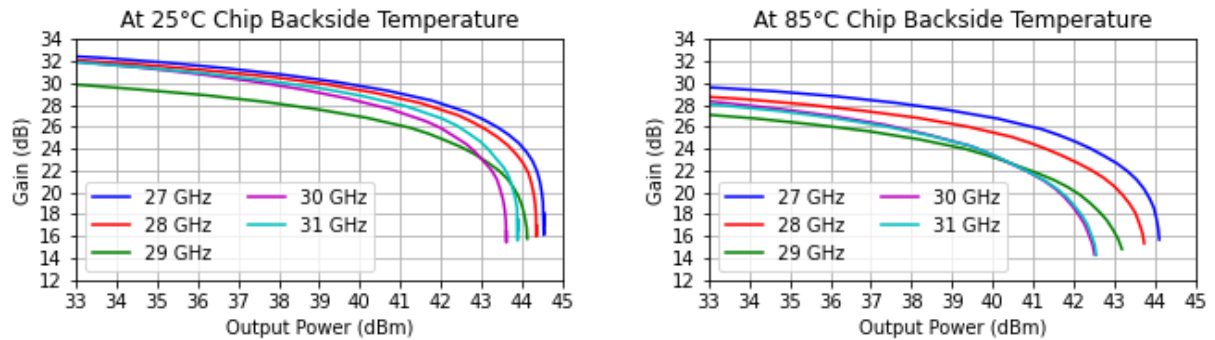
DC Power Consumption vs. Frequency & Chip Backside Temperature**Dissipated Power vs. Frequency & Chip Backside Temperature**

Typical Board Measurements: Large Signal Performances

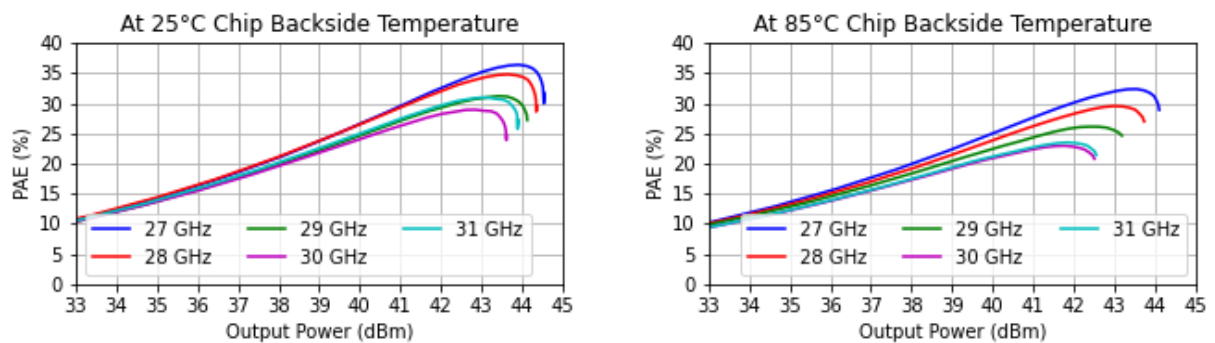
Performance versus output power and frequency

Test conditions : CW, $V_D = 25V$, $I_{DQ} = 440mA$, $T_{BS} = 25^\circ C / 85^\circ C$

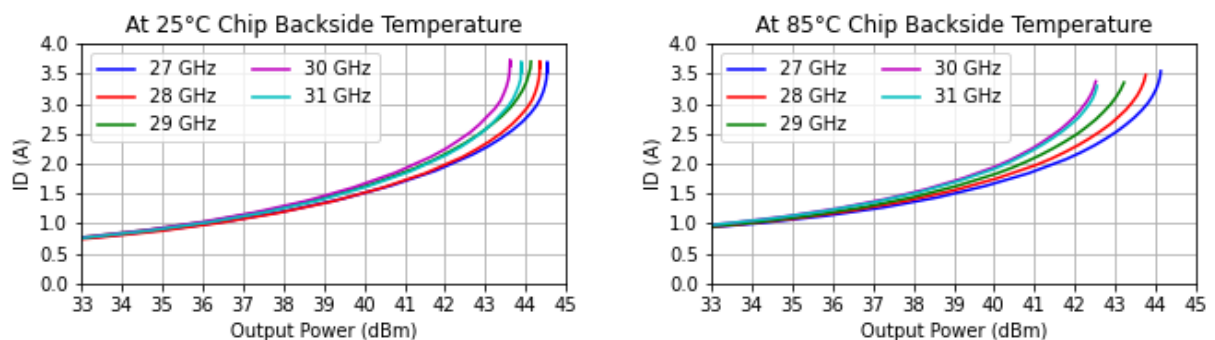
Gain vs. Output Power & Frequency



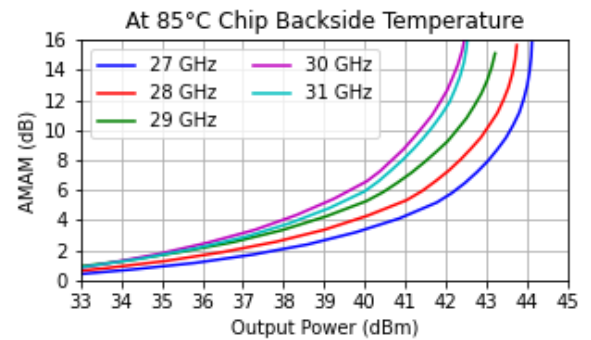
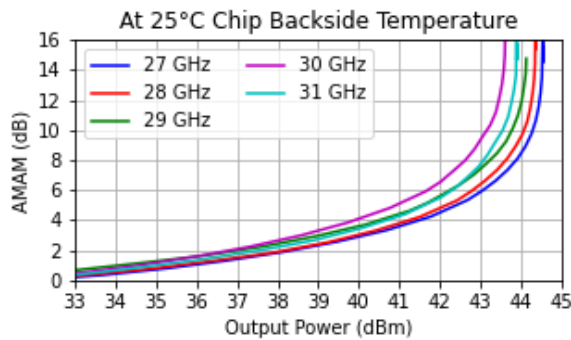
Power Added Efficiency vs. Output Power & Frequency



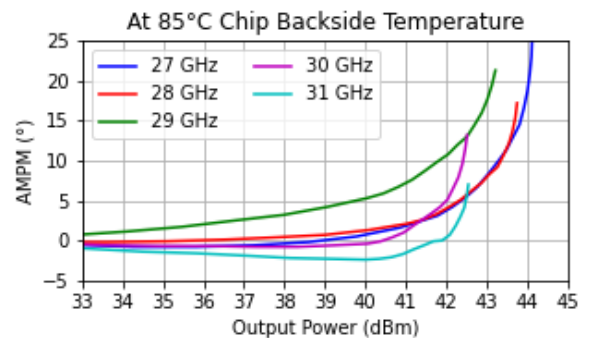
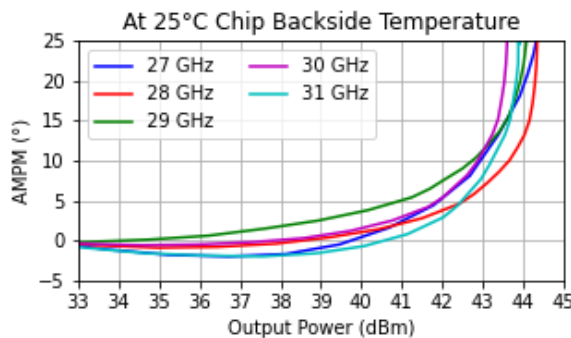
DC Drain Current vs. Output Power & Frequency



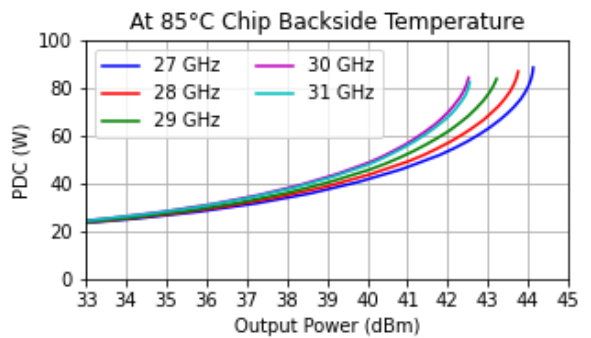
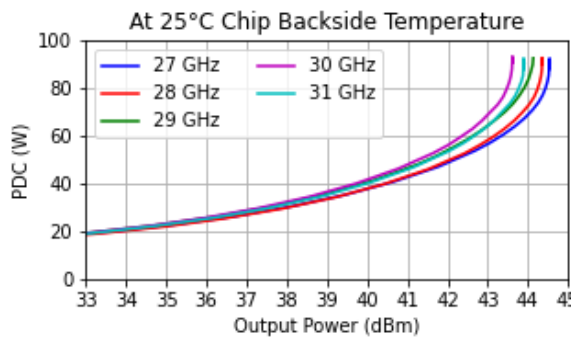
AMAM vs. Output Power & Frequency



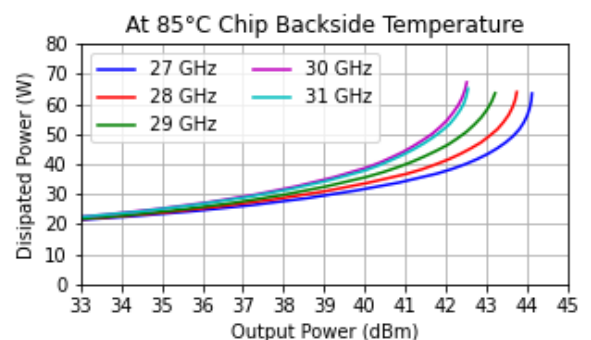
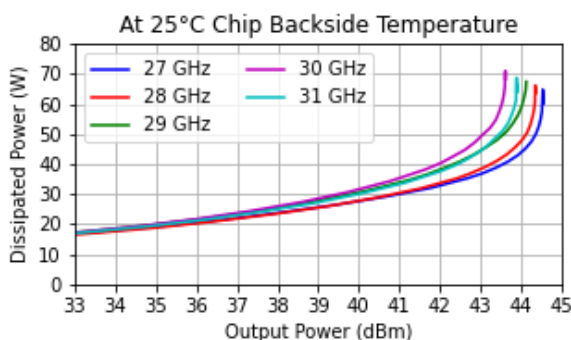
AMPM vs. Output Power & Frequency



DC Power Consumption vs. Output Power & Frequency



Dissipated Power vs. Output Power & Frequency

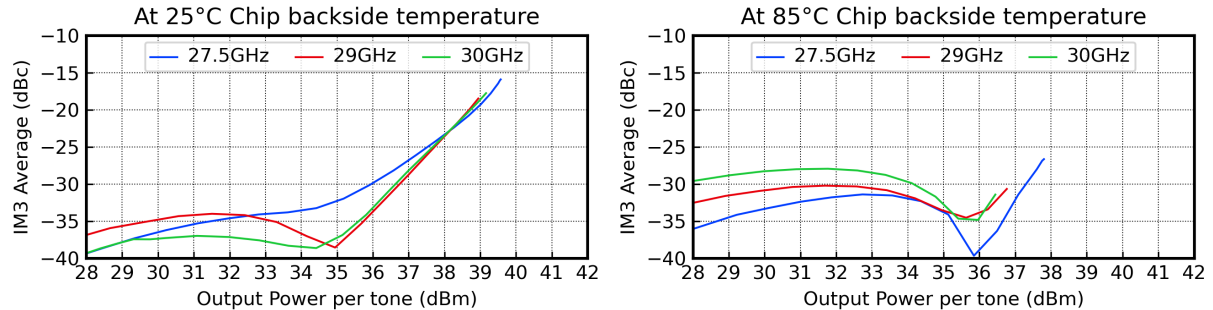


Typical Board Measurements: Intermodulation Distortion

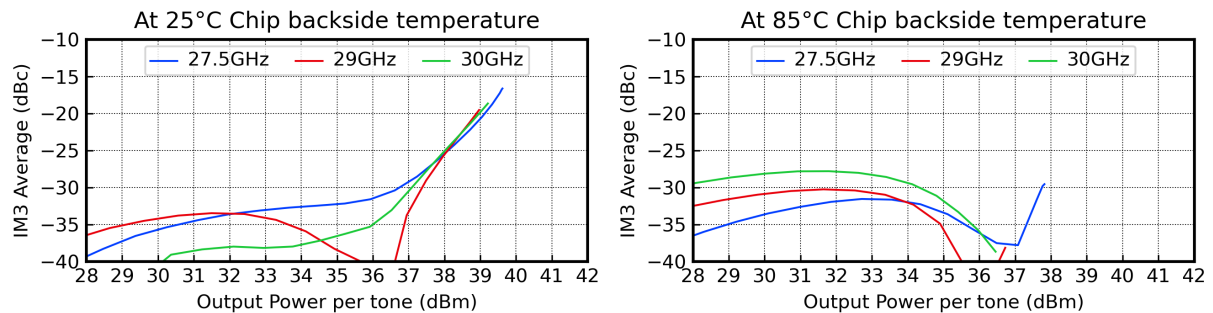
Performance versus output power and frequency

Test conditions : CW, $V_D = 25V$, $I_{dq} = 330mA$

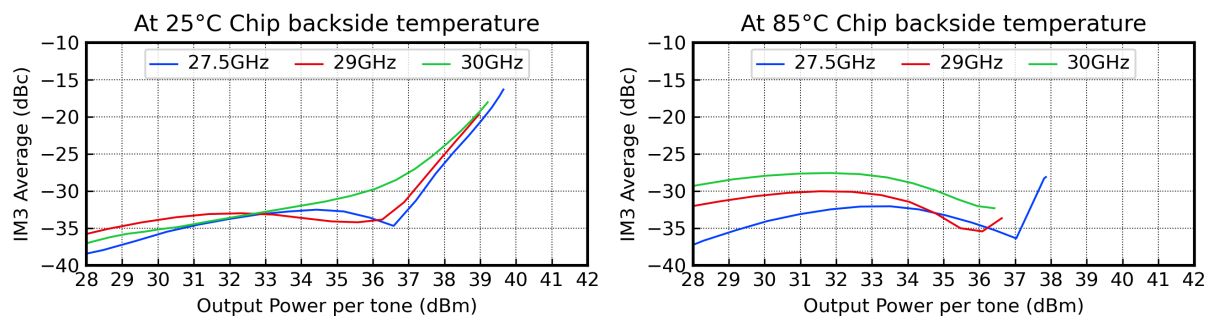
IMD3 vs. Output Power per Tone & Central Frequency, $\Delta F = 10MHz$



IMD3 vs. Output Power per Tone & Central Frequency, $\Delta F = 50MHz$



IMD3 vs. Output Power per Tone & Central Frequency, $\Delta F = 100MHz$

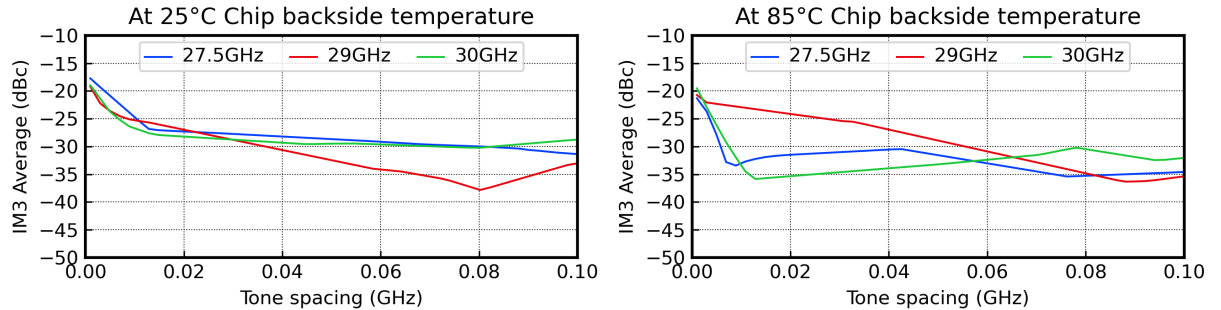


Typical Board Measurements: Intermodulation Distortion

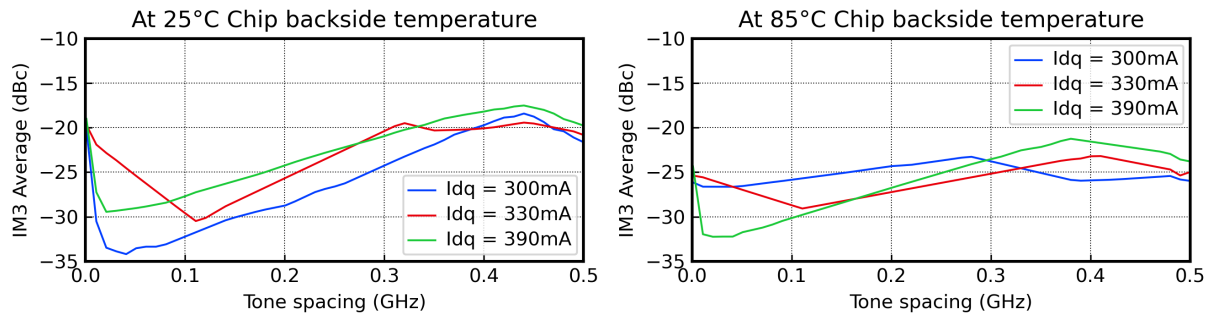
Performance versus output power and frequency

Test conditions : CW, $V_D = 25V$, $I_{dq} = 330mA$, $P_{out}/Tone = 37dBm$ at $T_{BS} = 25^\circ C$, $P_{out}/Tone = 36.5dBm$ at $T_{BS} = 85^\circ C$

IMD3 vs. Tone spacing & Central Frequency



IMD3 vs. Tone spacing & Quiescent Current @30GHz

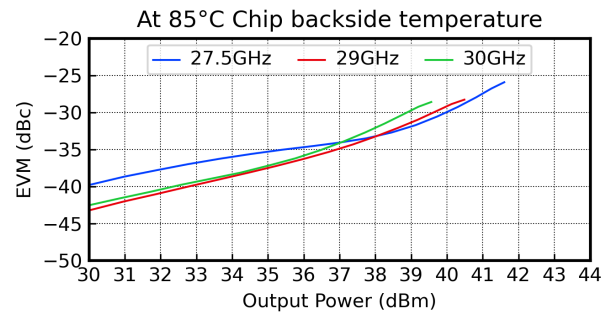
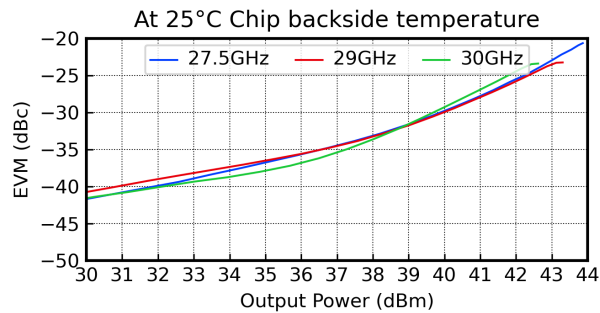


Typical Board Measurements: Modulation Measurements

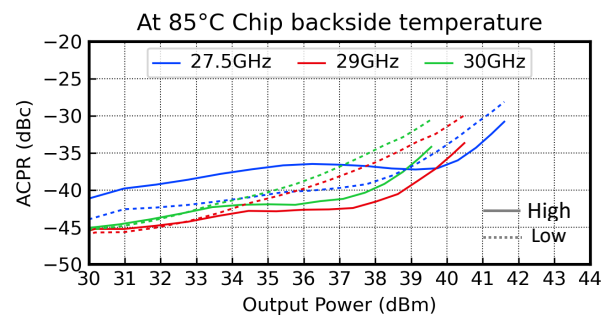
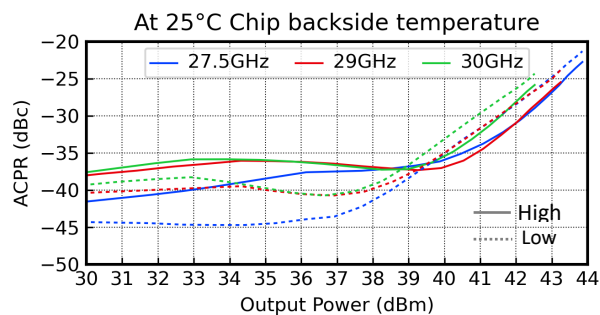
Performance versus output power and frequency

Test conditions : $V_D = 25V$, $I_{dq} = 330mA$, 8PSK, BW = 15 MHz, Roll-off = 0.2, PAPR = 5.1dB

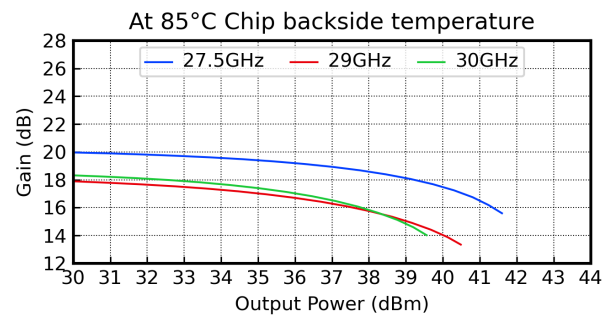
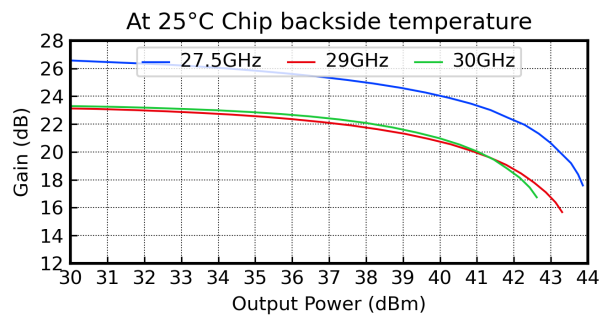
EVM vs. Output Power & Central Frequency



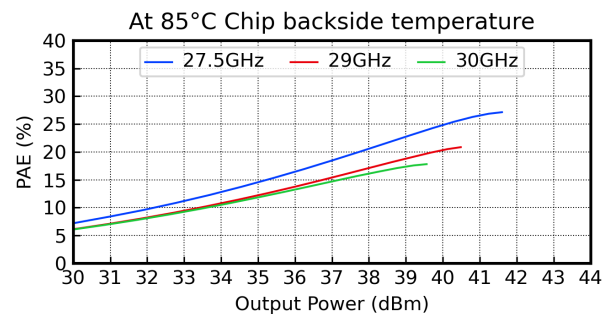
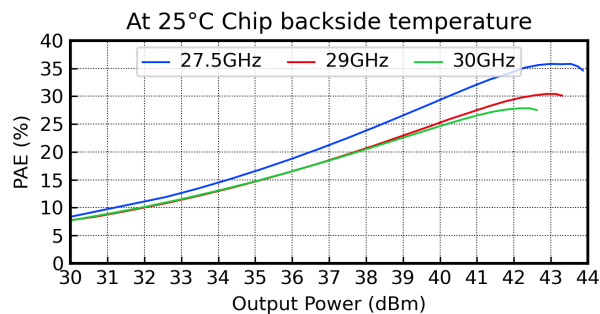
ACPR vs. Output Power & Central Frequency



Gain vs. Output Power & Central Frequency



PAE vs. Output Power & Central Frequency

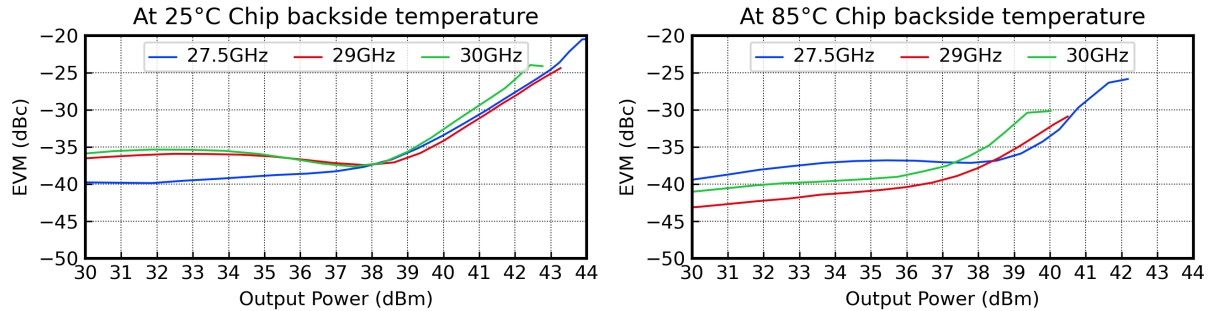


Typical Board Measurements: Modulation Measurements

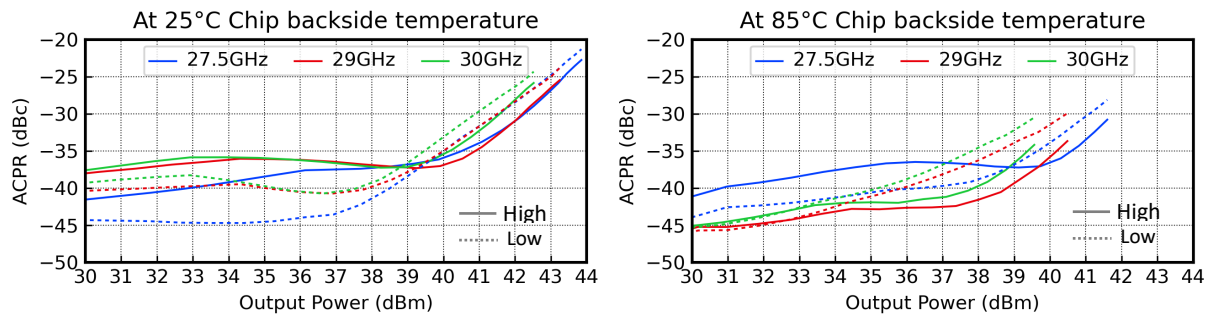
Performance versus output power and frequency

Test conditions : $V_D = 25V$, $I_{dq} = 330mA$, 8PSK, BW = 30 MHz, Roll-off = 0.2, PAPR = 5.1dB

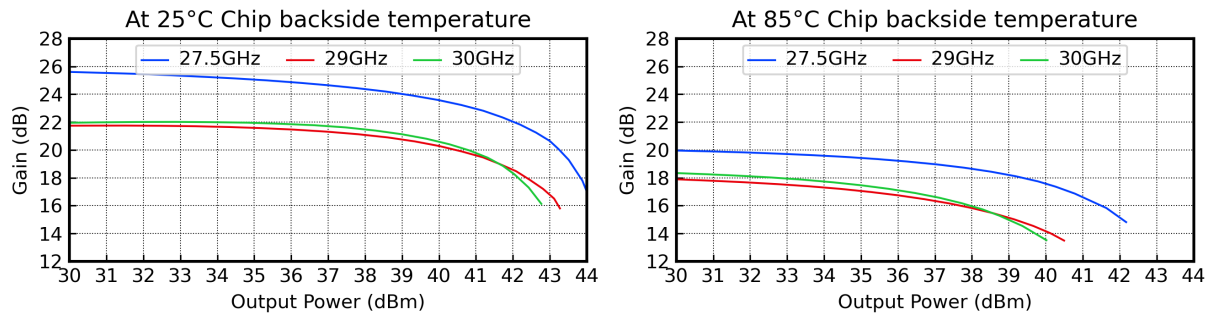
EVM vs. Output Power and Central Frequency



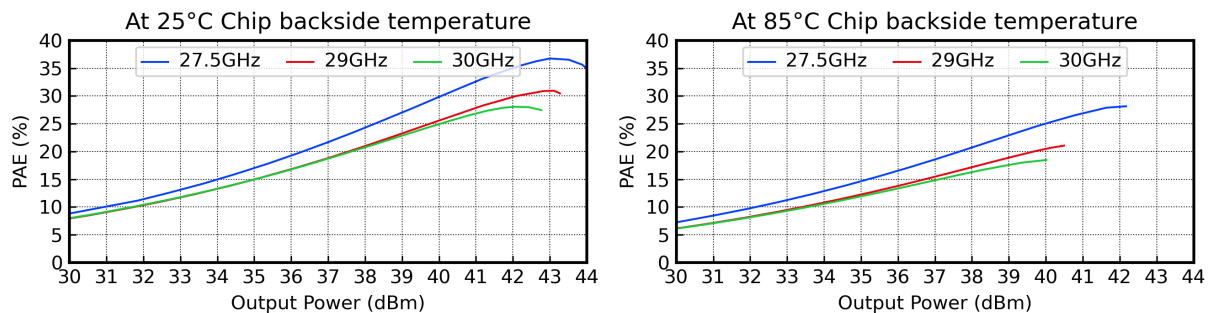
ACPR vs. Output Power & Central Frequency



Gain vs. Output Power & Central Frequency



PAE vs. Output Power & Central Frequency

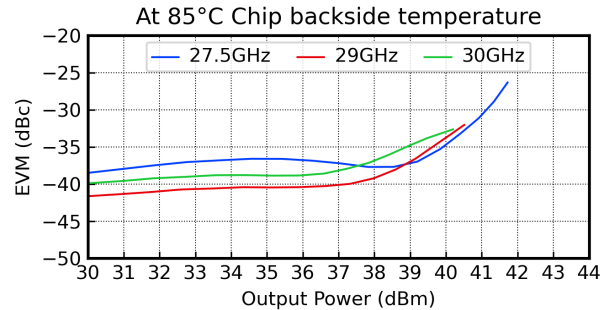
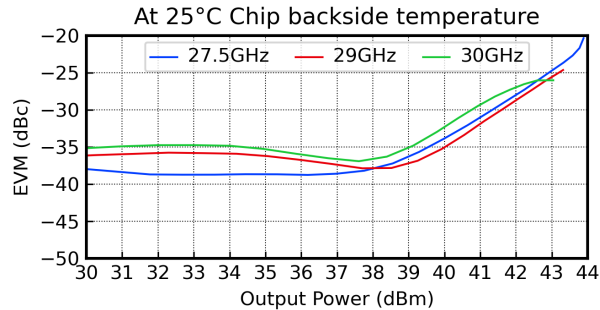


Typical Board Measurements : Modulation Measurements

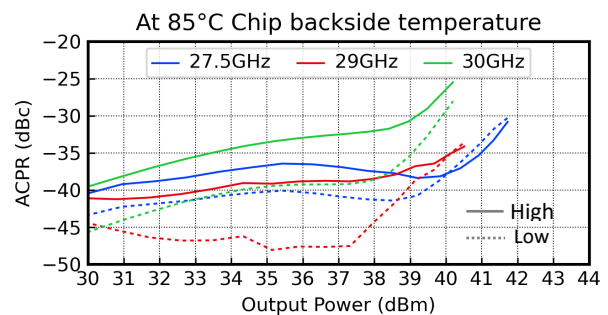
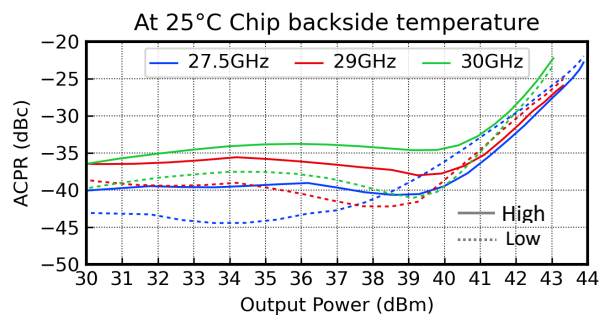
Performance versus output power versus frequency

Test conditions : $V_D = 25V$, $I_{dq} = 330mA$, 8PSK, BW = 100 MHz, Roll-off = 0.2, PAPR = 5.1dB

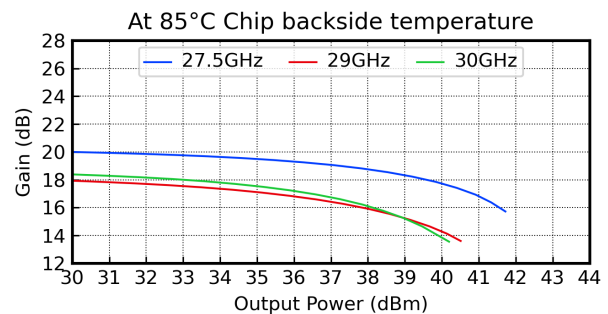
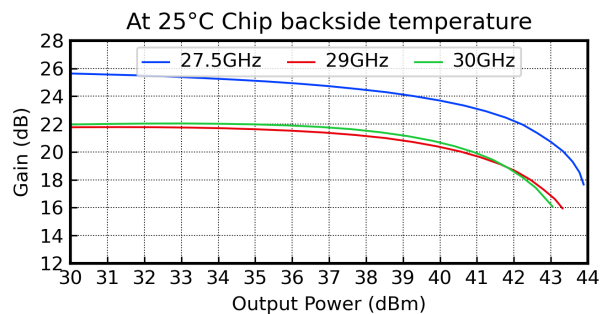
EVM vs. Output Power & Central Frequency



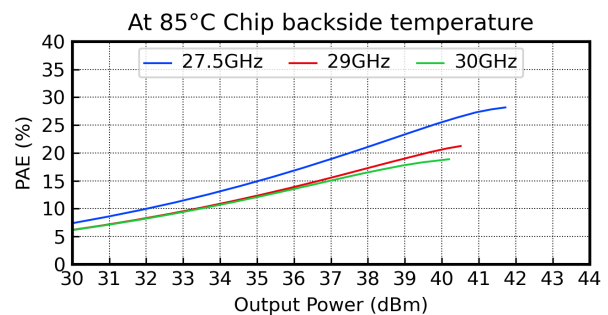
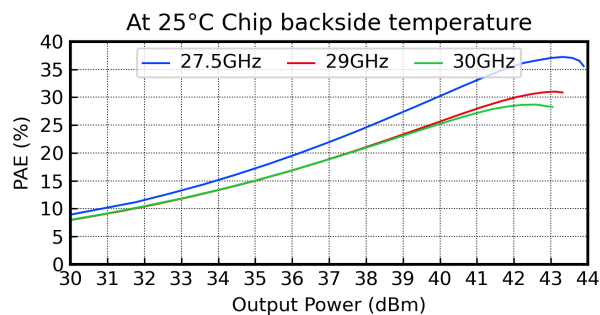
ACPR vs. Output Power & Central Frequency



Gain vs. Output Power & Central Frequency



PAE vs. Output Power & Central Frequency

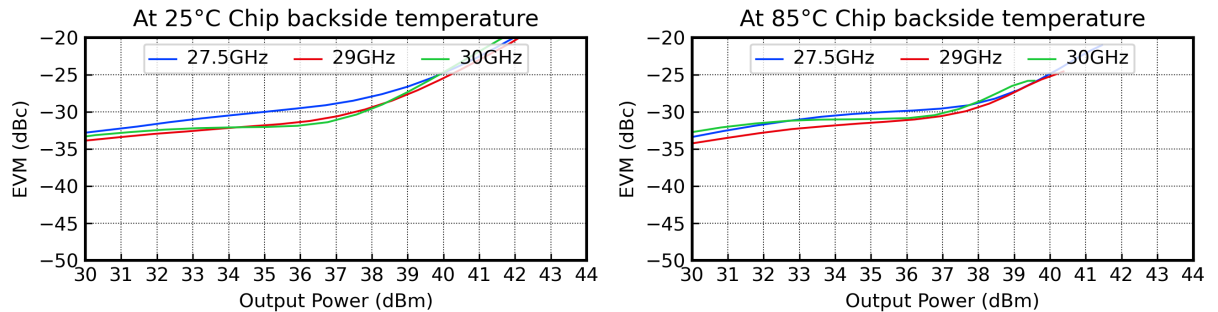


Typical Board Measurements: Modulation Measurements

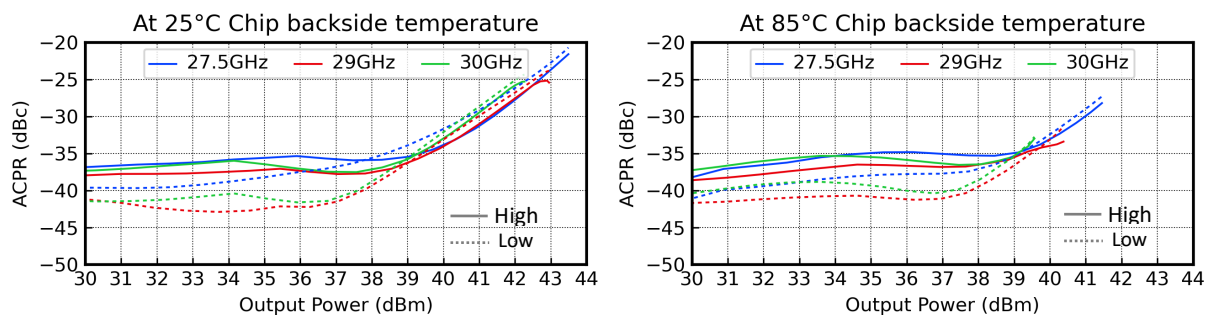
Performance versus output power and frequency

Test conditions : $V_D = 25V$, $I_{dq} = 330mA$, 256QAM, BW=100MHz, Roll-off=0.2, PAPR = 7.2dB

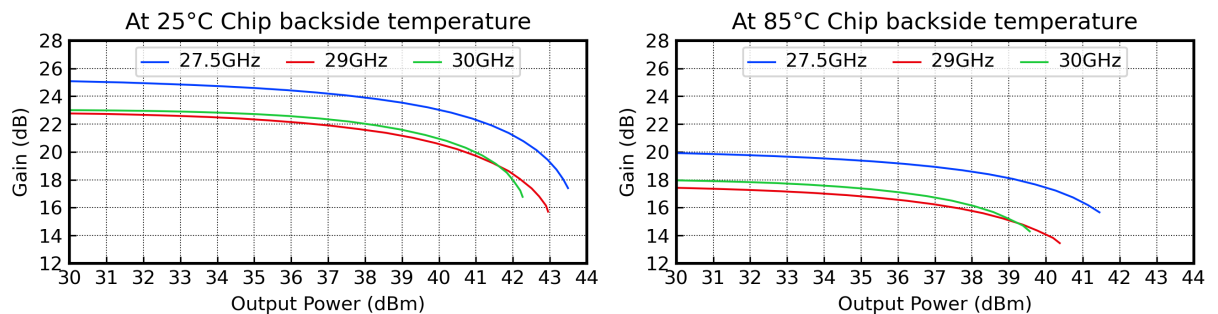
EVM vs. Output Power & Central Frequency



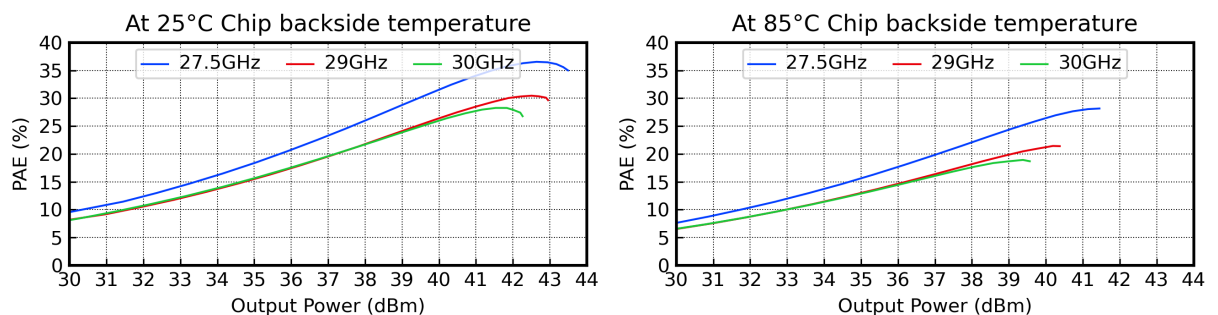
ACPR vs. Output Power & Central Frequency



Gain vs. Output Power & Central Frequency



PAE vs. Output Power & Central Frequency

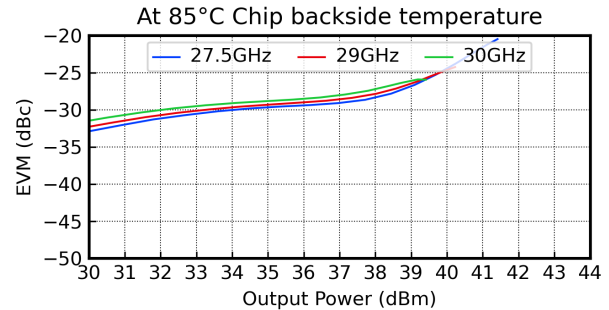
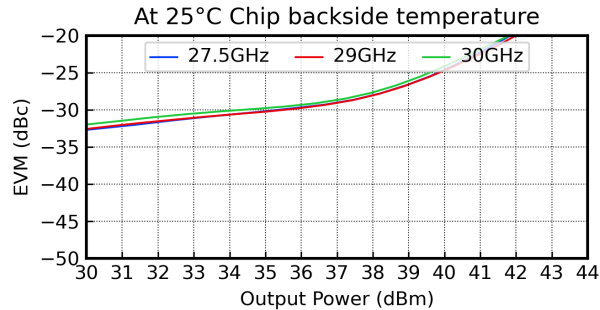


Typical Board Measurements: Modulation Measurements

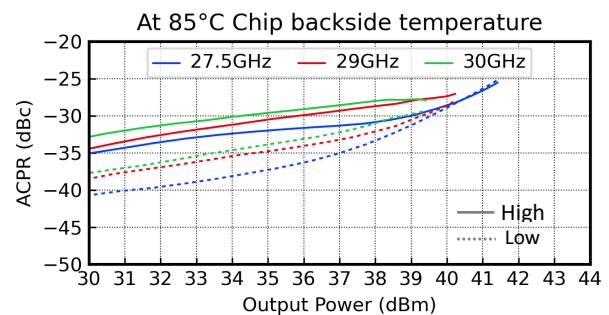
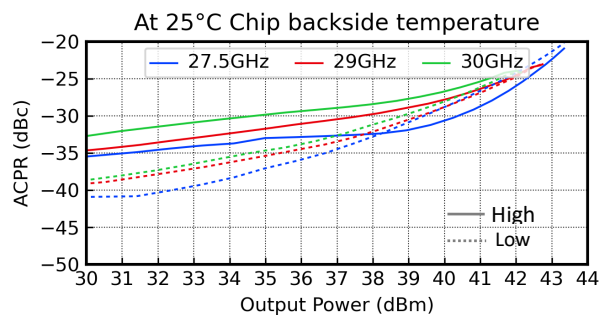
Performance versus output power and frequency

Test conditions : $V_D = 25V$, $I_{dq} = 330mA$, 256QAM, BW=400MHz, Roll-off=0.2, PAPR = 7.2dB

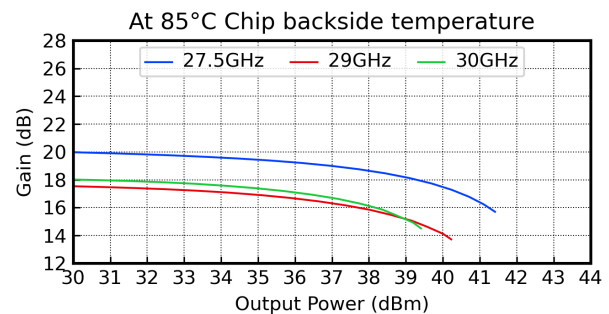
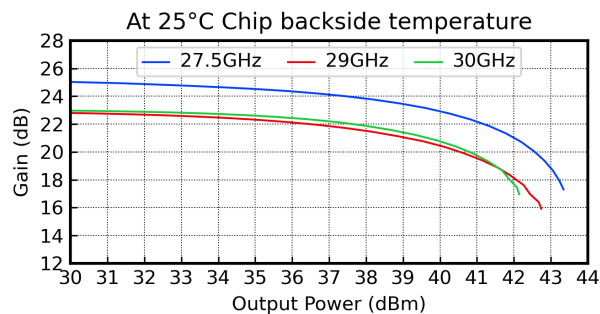
EVM vs. Output Power & Central Frequency



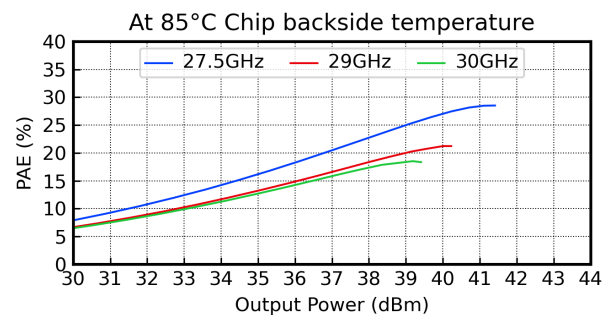
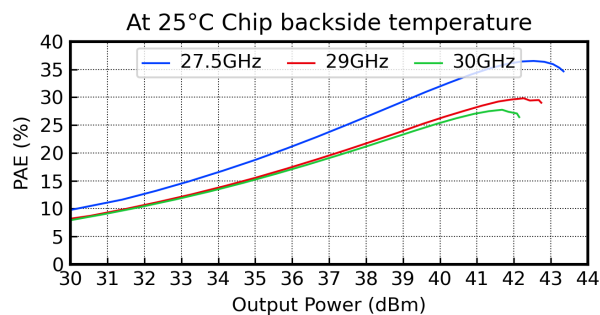
ACPR vs. Output Power & Central Frequency



Gain vs. Output Power & Central Frequency



PAE vs. Output Power & Central Frequency

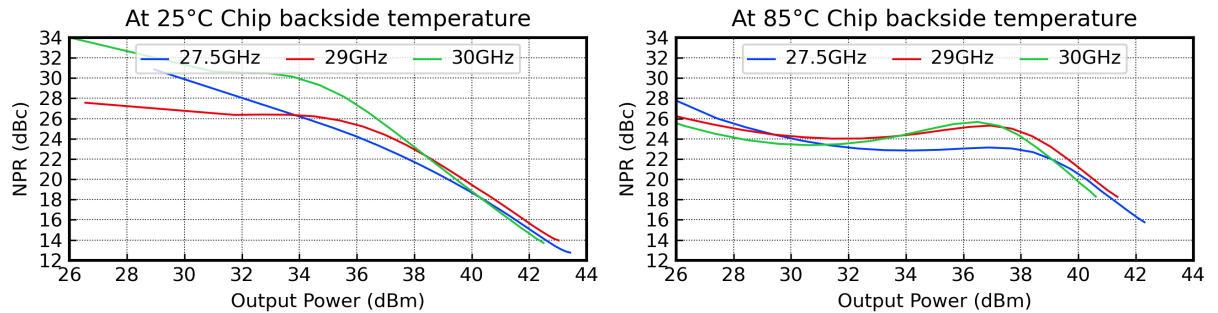


Typical Board Measurements: Noise Power Ratio

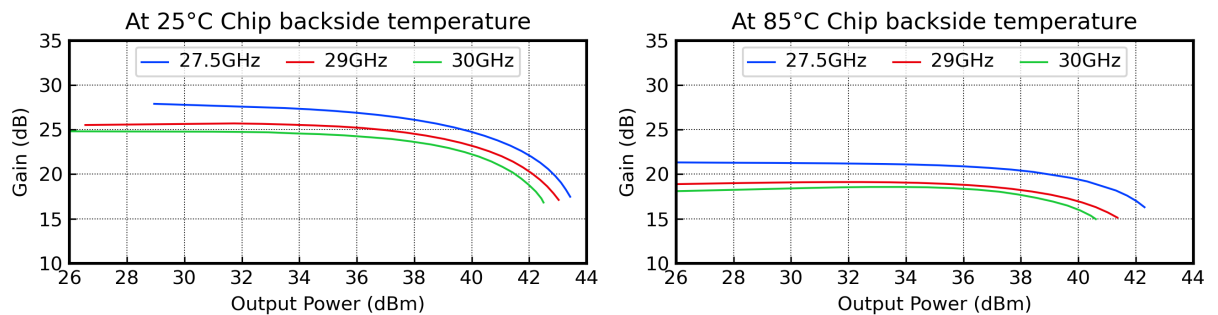
Performance versus output power and frequency

Test conditions : $V_D = 25V$, $I_{dq} = 330mA$, $BW = 45MHz$, Notch: 10%, Number of tones: 4501

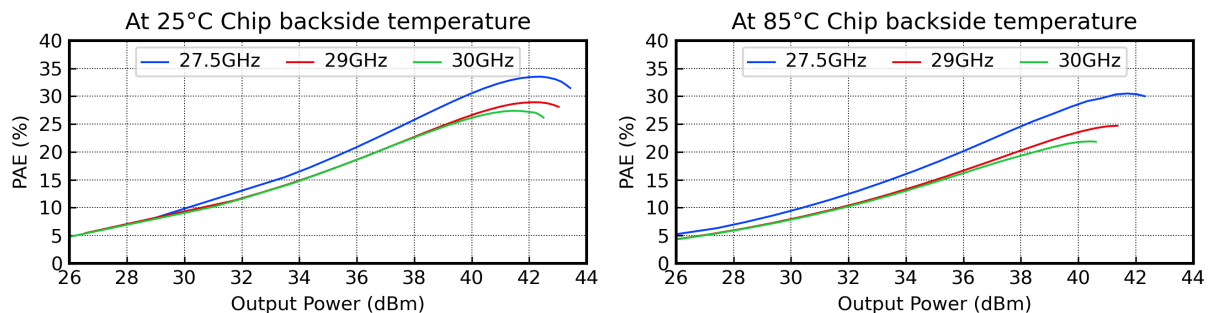
NPR vs. Output Power & Central Frequency



ACPR vs. Output Power & Central Frequency



Gain vs. Output Power & Central Frequency

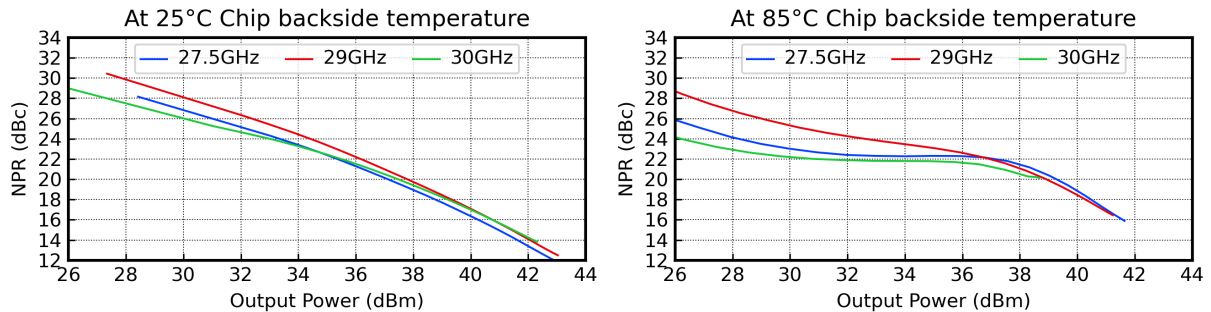


Typical Board Measurements: Noise Power Ratio

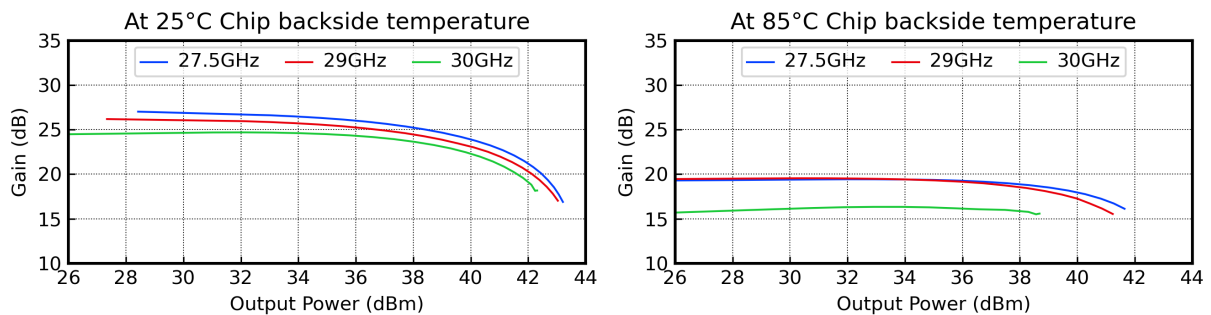
Performance versus output power and frequency

Test conditions : $V_D = 25V$, $I_{dq} = 330mA$, $BW = 1GHz$, Notch: 10%, Number of tones: 10 001

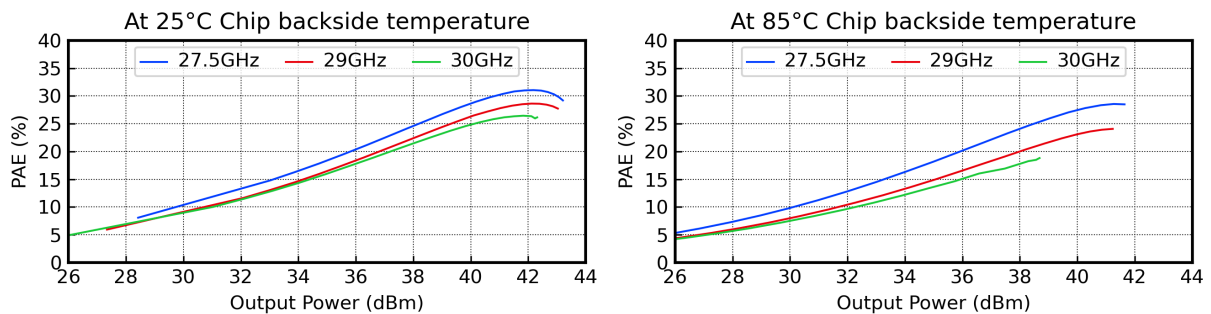
NPR vs. Output Power & Central Frequency



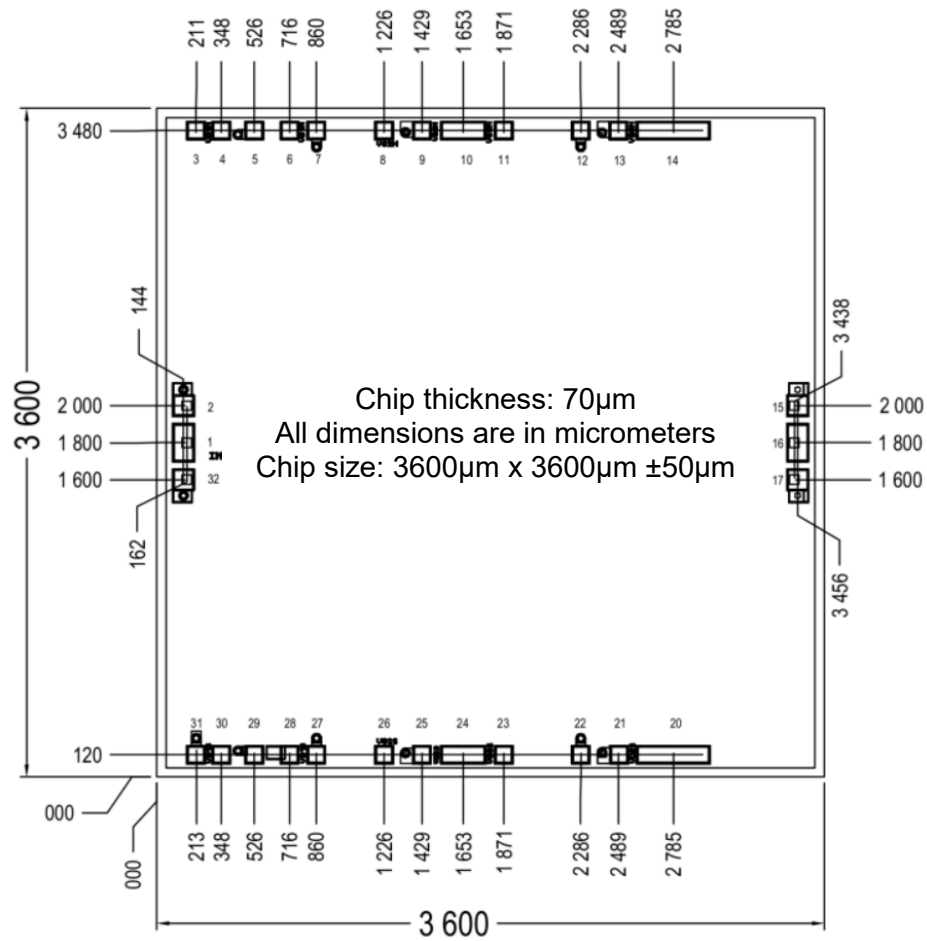
Gain vs. Output Power & Central Frequency



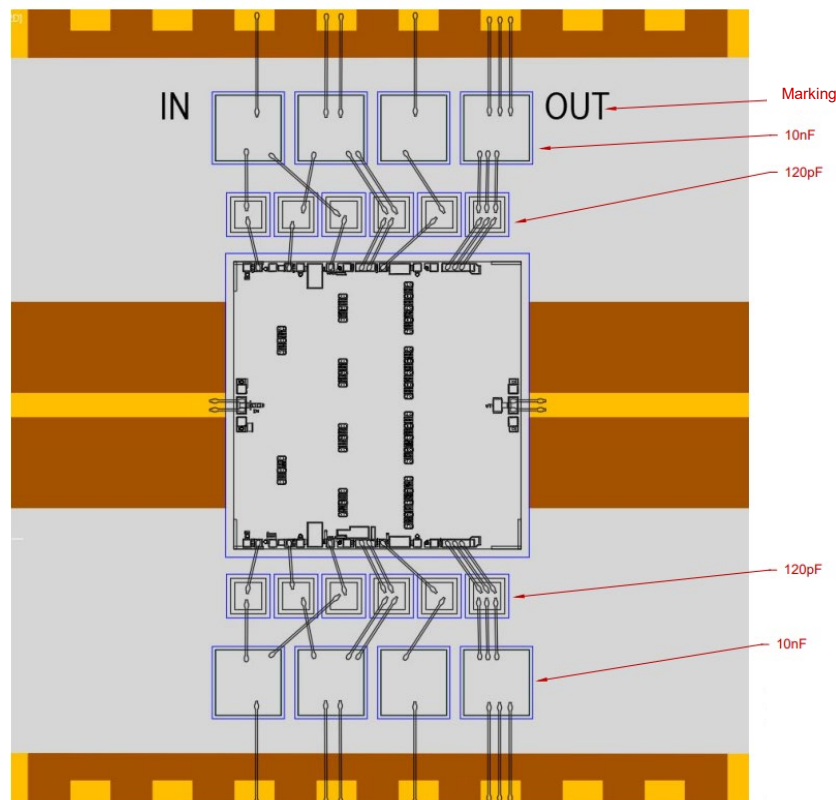
PAE vs. Output Power & Central Frequency



Mechanical Drawing



PAD Number	Name	Description	Pad size
1	RF IN	Input RF port	185μm x 200μm
4	G1	DC Gate voltage, 1 st Stage, North	100μm x 100μm
6	D1	DC Drain voltage, 1 st Stage, North	100μm x 100μm
8	G2	DC Gate voltage, 2 ^d stage, North	100μm x 100μm
10	D2	DC Drain voltage, 2 ^d stage, North	245μm x 100μm
11	G3	DC Gate voltage 3 ^d stage, North	100μm x 100μm
14	D3	DC Drain voltage, 3 ^d stage, North	400μm x 96μm
16	RF OUT	Output RF port	185μm x 200μm
20	D3	DC Drain voltage, 3 ^d stage, South	400μm x 96μm
23	G3	DC Gate voltage 3 ^d stage, South	100μm x 100μm
24	D2	DC Drain voltage, 2 ^d stage, South	245μm x 100μm
26	G2	DC Gate voltage, 2 ^d stage, South	100μm x 100μm
28	D1	DC Drain voltage, 1 st Stage, South	100μm x 100μm
30	G1	DC Gate voltage, 1 st Stage, South	100μm x 100μm
2,3,5,7,9,12, 13,15,17,21,22, 25,27,29,31,32	GND	Ground	100μm x 100μm



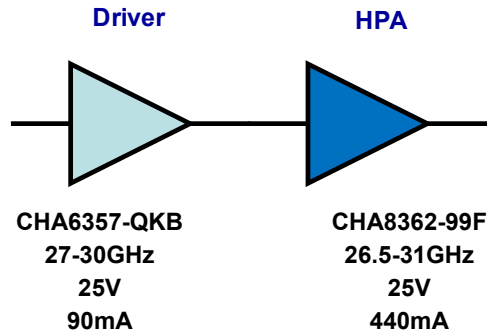
3 levels of decoupling capacitors have been used: 2 on the tab and 1 on the board. The first level is composed of 120 pF chip capacitors. The second level is composed of 10nF chip capacitors. The third level is made with 1μF SMD 1206 capacitors (and 10 ohms added in series). The first two levels should be as close as possible to the die.

Recommended UMS Power chain

The CHA8362-99F is recommended with the CHA6357-QKB as driver.

Total Gain: > 50dB

For more information about the CHA6357-QKB, see our web site www.ums-rf.com



Recommended reflow process assembly

Refer to the application note AN0001 available at <https://www.ums-rf.com> for die attach.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACH N°1907/2006. More environmental data are available in the application note AN0019 also available at <https://www.ums-rf.com>.

Recommended ESD management

Refer to the application note AN0020 available at <https://www.ums-rf.com> for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

Chip form :

CHA8362-99F/00

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