United Monolithic Semiconductors

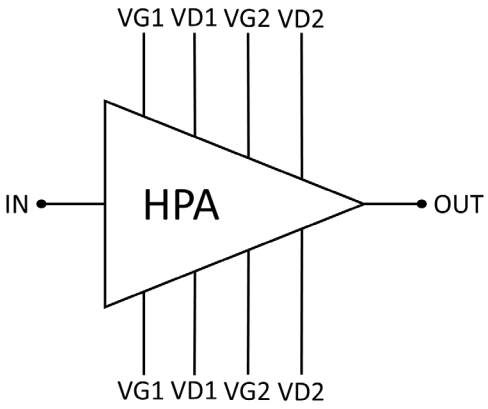
CHA8315-99F

15-18GHz High Power Amplifier

GaN Monolithic Microwave IC

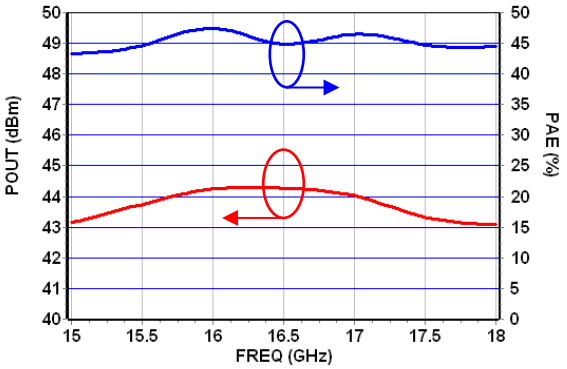
Description

The CHA8315-99F is a monolithic GaN High Power Amplifier operating in the frequency band 15 to 18 GHz and delivering an output power of 43.5dBm with an associated PAE of 45%. It exhibits 23dB small signal gain. The overall power supply is 20V/1.16A. The circuit is designed for defence applications but offers performance suited for a wide range of microwave applications. The part is manufactured on a robust GaN HEMT technology and is available as a die.



Main Features

- Broadband performance: 15-18GHz
- 43.5dBm Pout for +28dBm input power
- 45.5% PAE for +28dBm input power
- DC bias: Vd=20V & Idq = 1.16 A
- Chip size: 4.49 mm x 3.22 mm



Main Electrical Characteristics

Tbackside = +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	15		18	GHz
Gain	Linear Gain		23		dB
PAE	Maximum power added efficiency (Pin = 28dBm)		47		%
Psat	Output Power @saturation (Pin = 30dBm)		43.5		dBm

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Specifications

Tbackside = +25°C, Vd = +20V

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	15		18	GHz
Gain	Linear Gain		23		dB
Psat	Output Power @saturation (Pin = 30dBm)		43.5		dBm
Id	Drain current @saturation (Pin = 30dBm)		2.5		A
PAE	Maximum power added efficiency (Pin=28dBm)		45		%
Gass	Associated gain @max PAE (Pin = 28dBm)		15		dB
Pdiss	Dissipated power @max PAE (Pin = 28dBm)		27.5		W
S11	Input return loss		-14		dB
S22	Output return loss		-20		dB
Idq	Quiescent drain current		1.16		A

These values are representative of average de-embedded on board measurements.

Absolute Maximum Ratings (1)(2)

Tbackside = +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	27	V
Vg	Gate bias voltage	-5	V
Pin	Maximum peak input power overdrive	34	dBm
Tj	Maximum junction temperature	230	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.

(2) See Device thermal performances section

Recommended Operating Range (3), (4)

Symbol	Parameter	Values	Unit
Vd	Recommended drain bias voltage	20	V
Idq	Quiescent drain current	1 to 1.25	A
Pin	Recommended input power overdrive	25 to 30	dBm
Tj	Maximum junction temperature	200	°C

(3) Electrical performances are defined for specified test conditions

(4) Electrical performances are not guaranteed over all recommended operating conditions

Temperature Range

Tbackside	Operating backside temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +150	°C

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Typical Bias Conditions

Tbackside= +25°C

Symbol	Pad N°	Parameter	Values	Unit
VG1	5 & 25	1st stage gate voltage tuned for Idq = 1.16A	-2.8	V
VG2	10 & 20	2nd stage gate voltage tuned for Idq = 1.16A	-2.8	V
VD1	8 & 22	1st stage drain voltage	20	V
VD2	12 & 18	2nd stage drain voltage	20	V

"Power ON" sequence

1. Bias HPA gate voltage close to Vpinch-off (Typically: VG = VG1 = VG2 = ~ -5V)
2. Apply VD bias voltage (Typically: VD = VD1 = VD2 = 20V)
3. Increase VG up to quiescent bias drain current Idq
4. Apply RF signal

"Power OFF" sequence

1. Turn off RF signal
2. Bias HPA gate voltage close to Vpinch-off (Typically: VG = ~ -5V)
3. Turn VD bias voltage to 0V
4. Turn VG bias voltage to 0V

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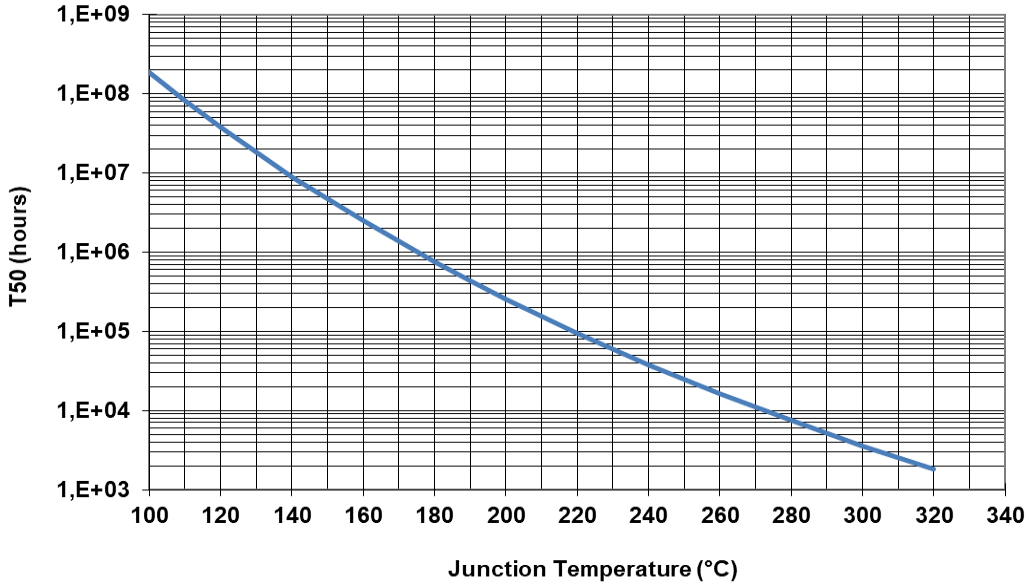
Device thermal performance

All the figures given in this section are obtained assuming that the die is only cooled down by conduction through the chip backside.
The temperature is monitored at the chip back-side interface (Tb).
For nominal operation, the system maximum temperature must be adjusted in order to guarantee that Tj remains below the maximum value specified in the Recommended Operating Ratings table.
PCB system must be designed to comply with this requirement.

Parameter	Biasing conditions	Tjunction (°C)	R_{TH} (°C/W)	T50 (hours)
R_{TH} (1) Thermal Resistance (Junction to Case)	Vd= 20V Pout = 43 dBm Pdiss = 31.6W Tb = 85°C	142	1.82	$8x10^6$

(1) Assuming 85°C Tb



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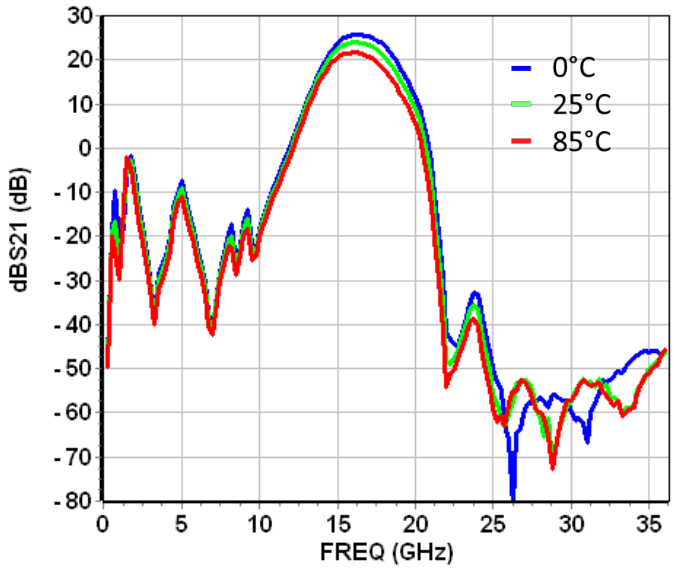
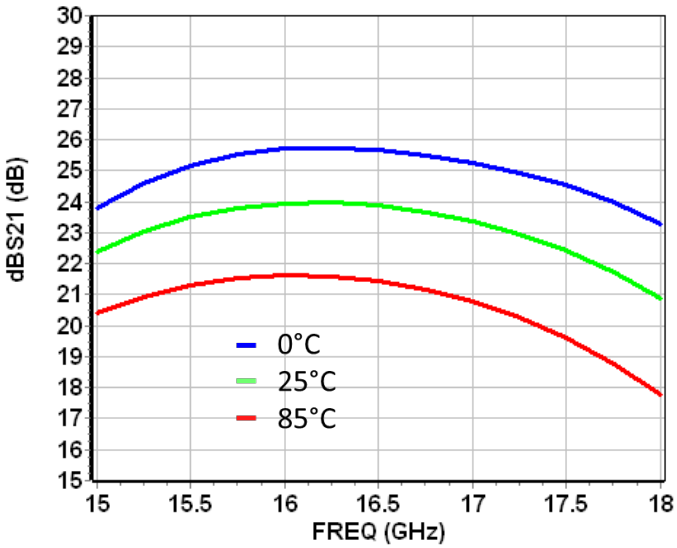
Typical Board Measurements (CW S parameters)

Tbackside= 0°C/+25°C/+85°C, Vd = 20V, Idq = 1.16A@25°C
Board losses are de-embedded. Measurements are given in die access plans.

Wide band linear gain S21 (dB) versus frequency (GHz) for Tb = 0, +25 and +85°C



Linear gain S21 (dB) versus frequency for Tb=0, +25 and +85°C



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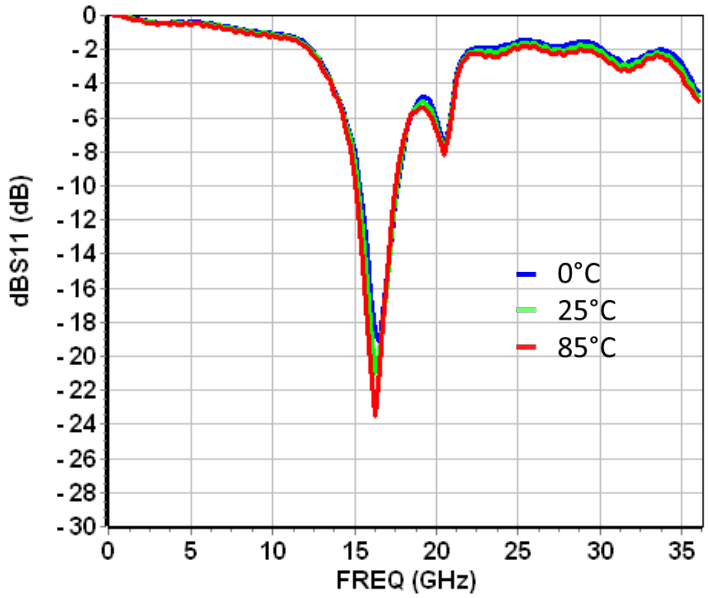
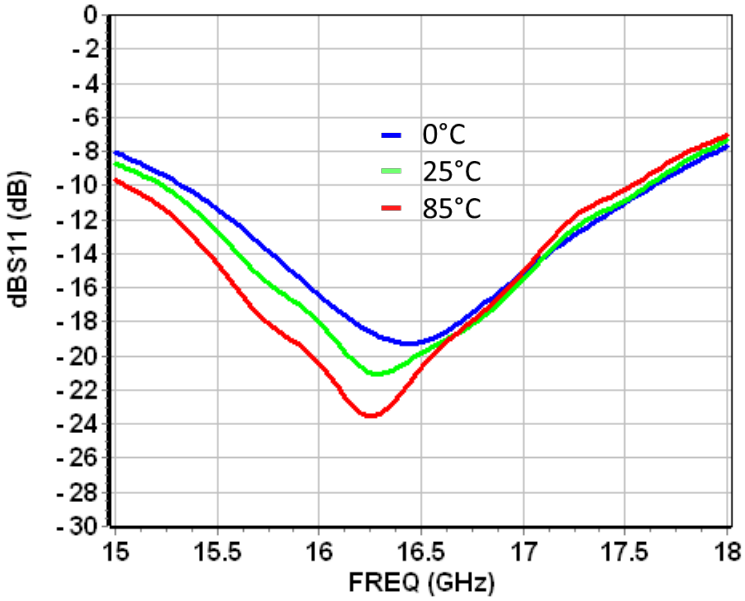
Typical Board Measurements (CW S parameters)

Tbackside = 0°C/+25°C/+85°C, Vd = 20V, Idq = 1.16A@25°C
Board losses are de-embedded. Measurements are given in die access plans.

Wide band input return loss S11 (dB) versus frequency (GHz) for Tb=0, +25 and +85°C



Input return loss S11 (dB) versus frequency (GHz) for Tb=0, +25 and +85°C



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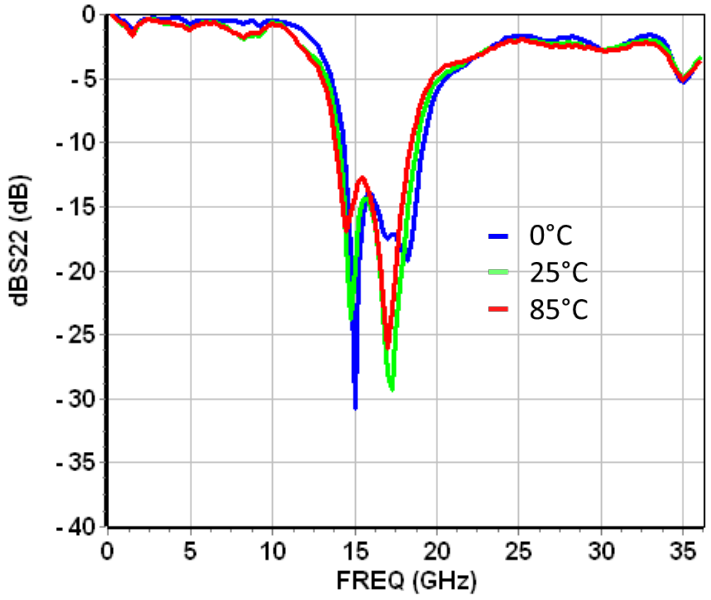
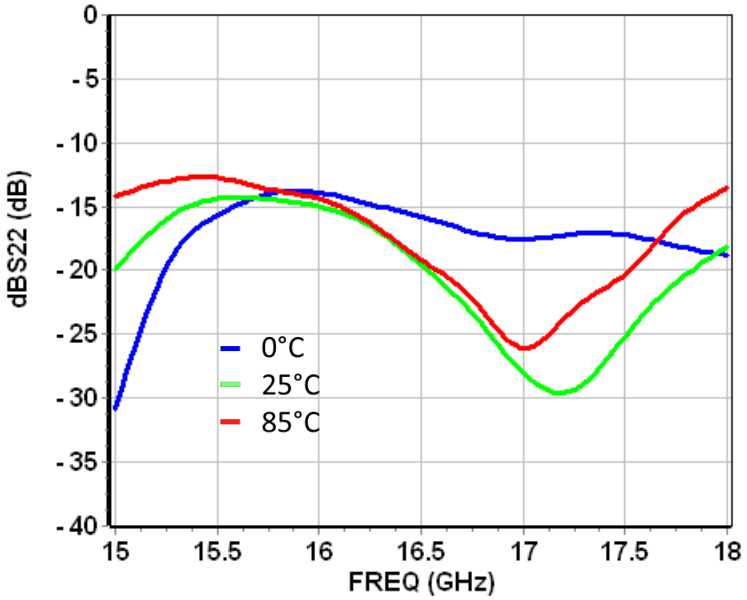
Typical Board Measurements (CW S parameters)

Tbackside = 0°C/+25°C/+85°C, Vd = 20V, Idq = 1.16A@25°C
Board losses are de-embedded. Measurements are given in die access plans.

Wide band output return loss S22 (dB) versus frequency (GHz) for Tb=0, +25 and +85°C



Output return loss S22 (dB) versus frequency (GHz) for Tb=0, +25 and +85°C



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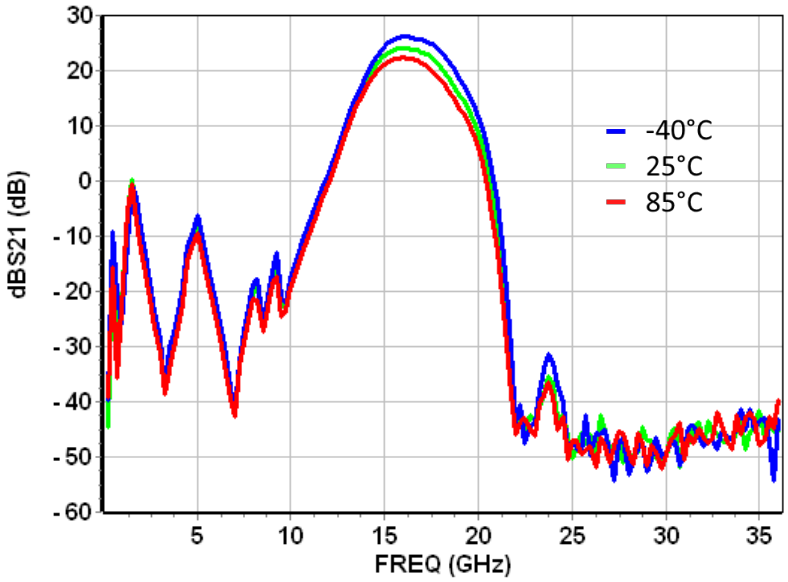
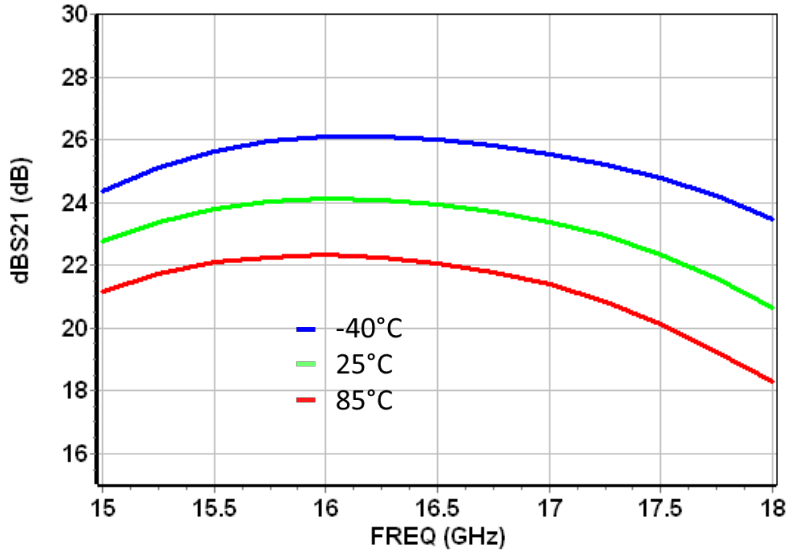
Typical Board Measurements (pulsed S parameters)

Tbackside = -40°C/+25°C/+85°C, Vd = 20V, Idq = 1.16A@25°C.
Pulse width=35µs & Duty cycle =10%.
Board losses are de-embedded. Measurements are given in die access plans.

Wide band linear gain S21 (dB) versus frequency (GHz) for Tb=-40, +25 and +85°C



Linear gain S21 (dB) versus frequency (GHz) for Tb=-40, +25 and +85°C



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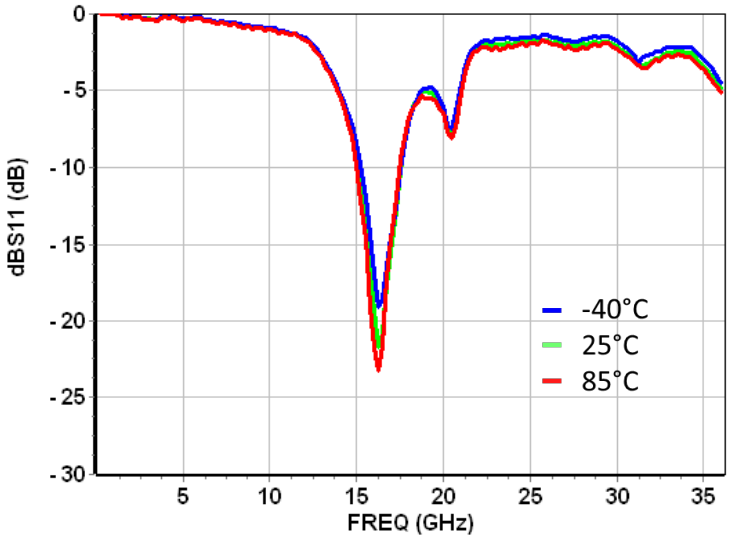
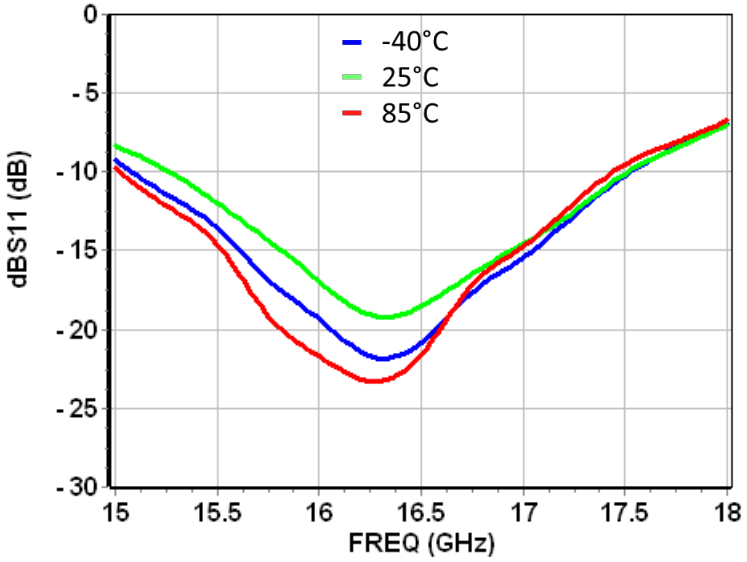
Typical Board Measurements (pulsed S parameters)

Tbackside = -40°C/+25°C/+85°C, Vd = 20V, Idq = 1.16A@25°C.
Pulse width=35µs & Duty cycle =10%.
Board losses are de-embedded. Measurements are given in die access plans.

Wide band input return loss S11 (dB) versus frequency (GHz) for Tb=-40, +25 and +85°C



Input return loss S11 (dB) versus frequency (GHz) for Tb=-40, +25 and +85°C



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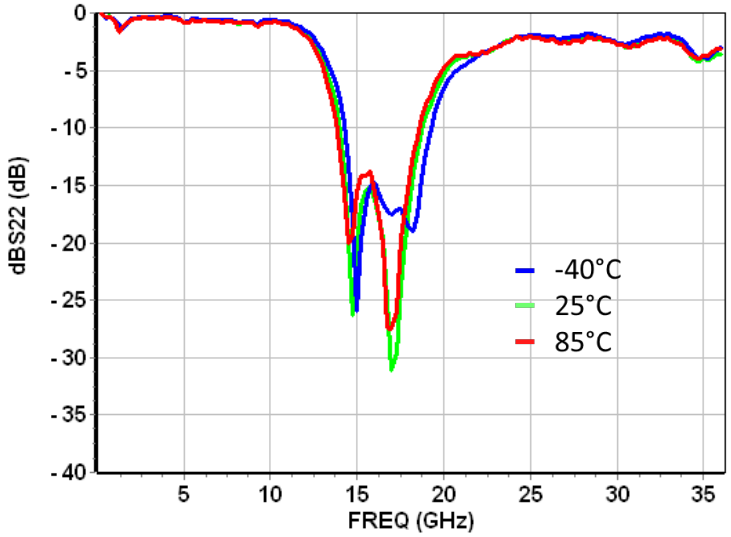
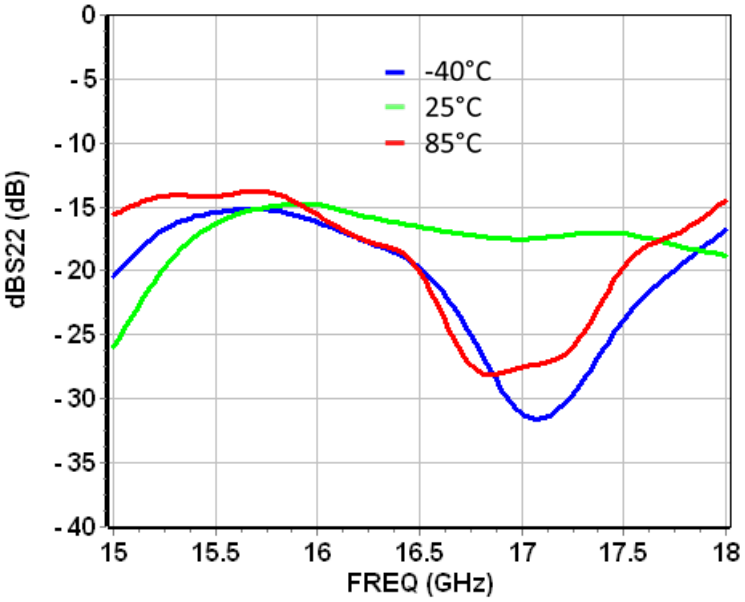
Typical Board Measurements (pulsed S parameters)

Tbackside = -40°C/+25°C/+85°C, Vd = 20V, Idq = 1.16A@25°C.
Pulse width=35µs & Duty cycle =10%.
Board losses are de-embedded. Measurements are given in die access plans.

Wide band output return loss S22 (dB) versus frequency (GHz) for Tb=-40, +25 and +85°C



Output return loss S22 (dB) versus frequency (GHz) for Tb=-40, +25 and +85°C



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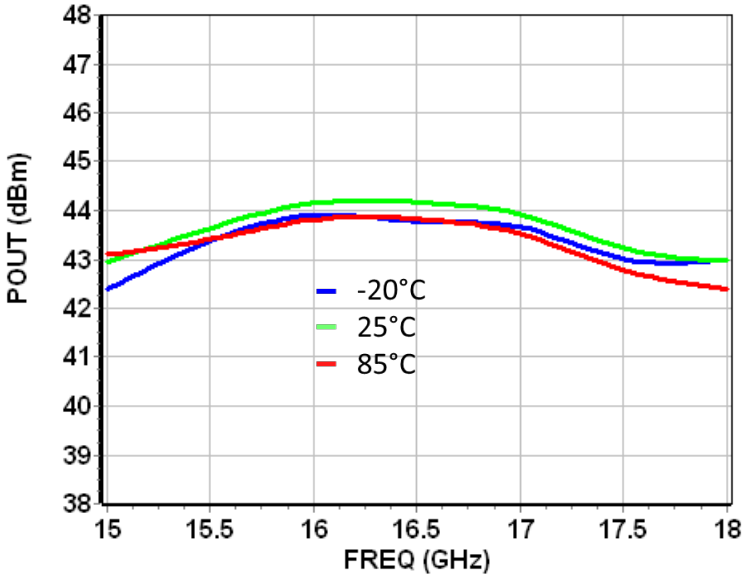
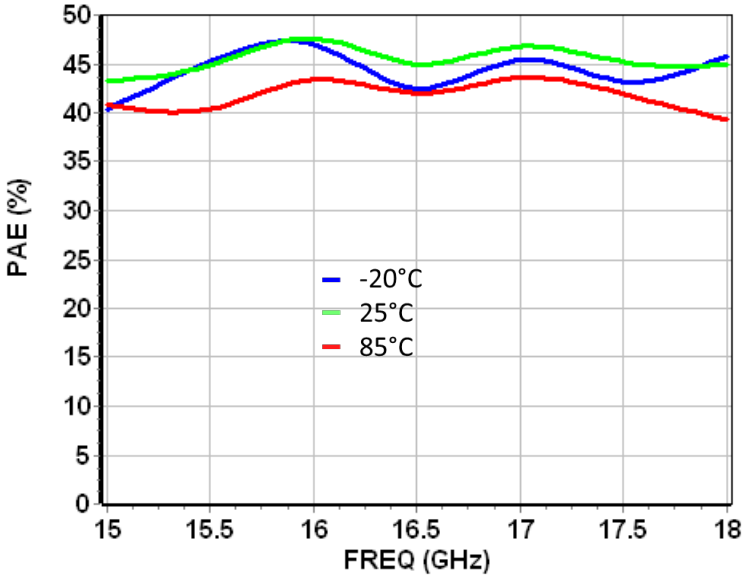
Typical Board Measurements (CW power measurements)

Tbackside = -20°C/+25°C/+85°C, Vd = 20V, Idq = 1.16A@25°C, 8 dB gain compression
Board losses are de-embedded. Measurements are given in die access plans.

Pout (dBm) versus frequency (GHz) for Tb=-20, +25 and +85°C



PAE (%) versus frequency (GHz) for Tb=-20, +25 and +85°C



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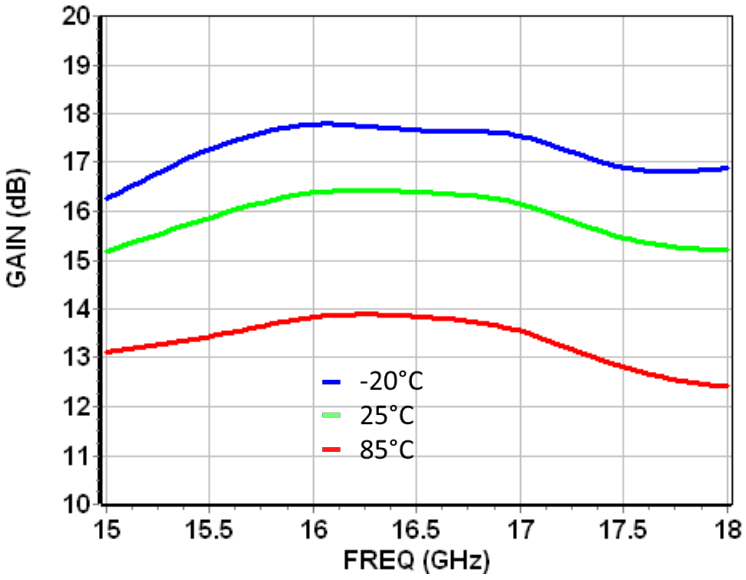
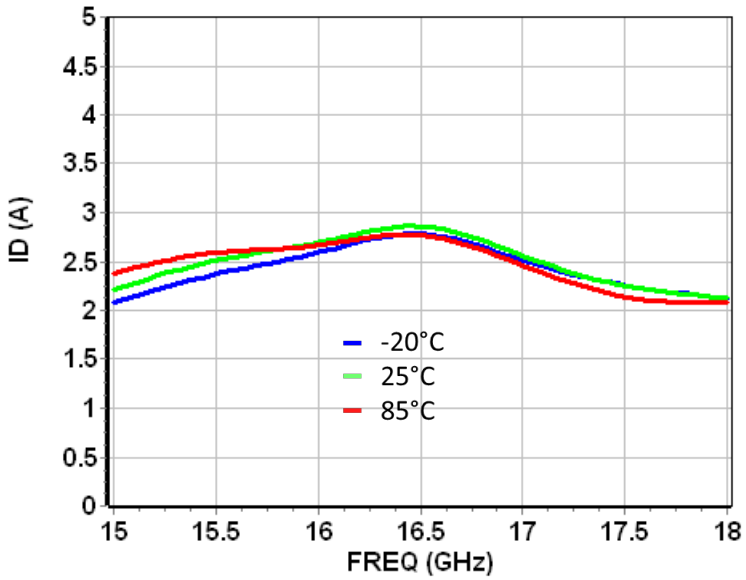
Typical Board Measurements (CW power measurements)

Tbackside = -20°C/+25°C/+85°C, Vd = 20V, Idq = 1.16A@25°C, 8 dB gain compression
Board losses are de-embedded. Measurements are given in die access plans.

Gain (dB) versus frequency (GHz) for Tb=-20, +25 and +85°C



Id (A) versus frequency (GHz) for Tb=-20,+25 and +85°C



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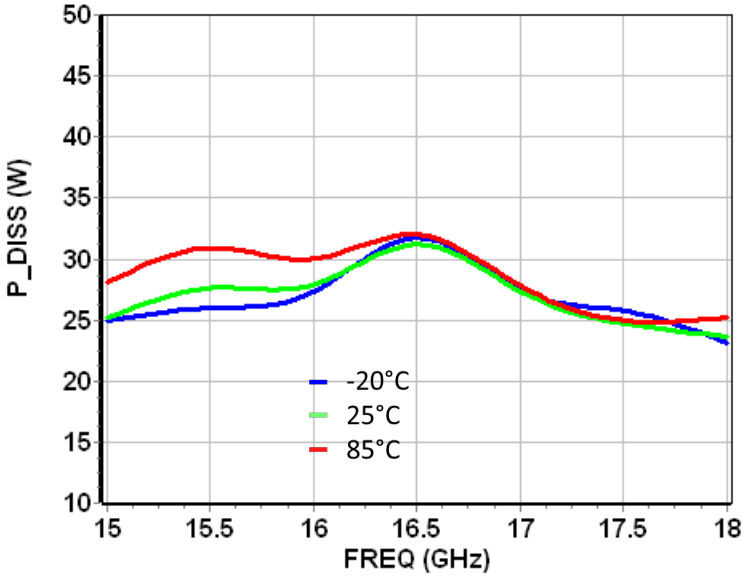
Typical Board Measurements (CW power measurements)

Tbackside = -20°C/25°C/85°C, Vd = 20V, Idq = 1.16A@25°C, 8 dB gain compression
Board losses are de-embedded. Measurements are given in die access plans.

Pdiss (W) versus frequency (GHz) for Tb=-20,+25 and +85°C



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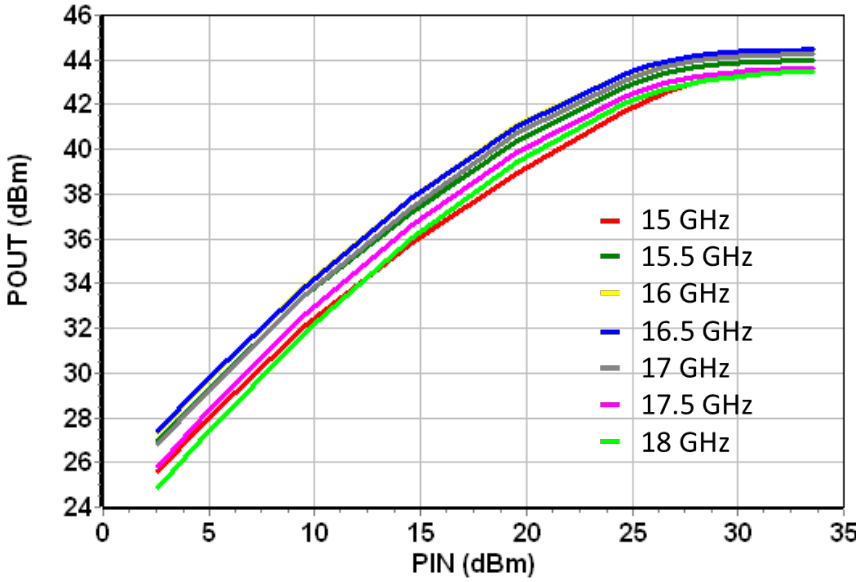
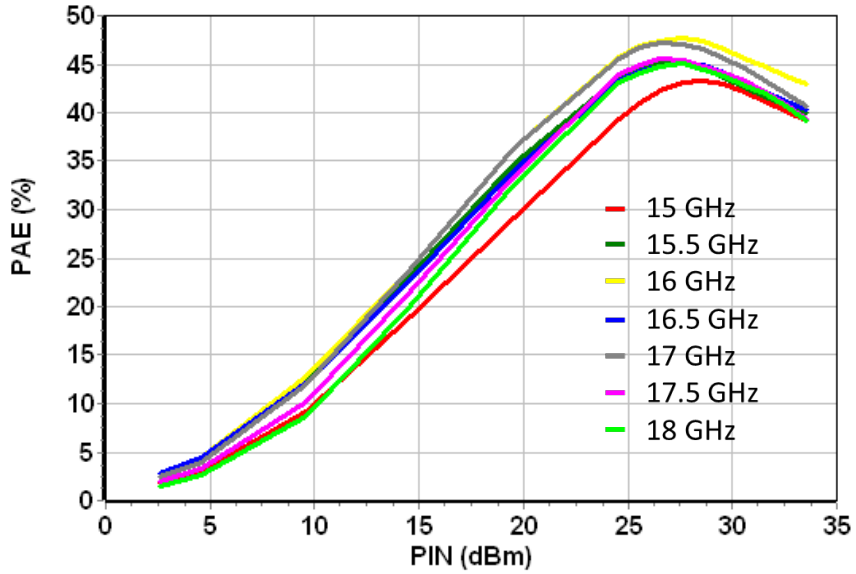
Typical Board Measurements (CW power measurements)

Tbackside = +25°C, Vd = 20V, Idq = 1.16A
Board losses are de-embedded. Measurements are given in die access plans.

Pout (dBm) versus Pin (dBm)



PAE (%) versus Pin (dBm)



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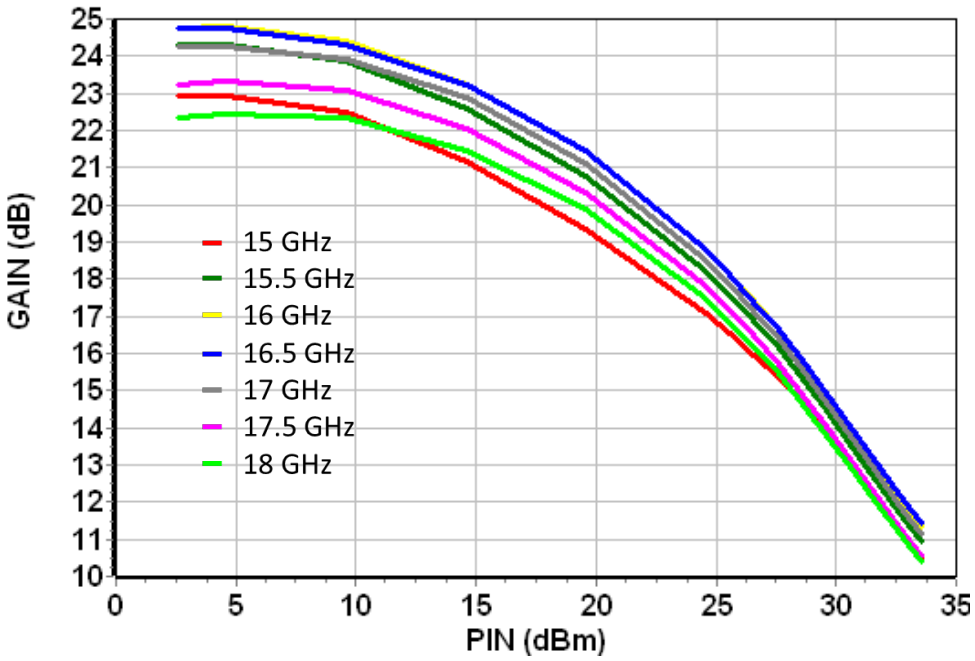
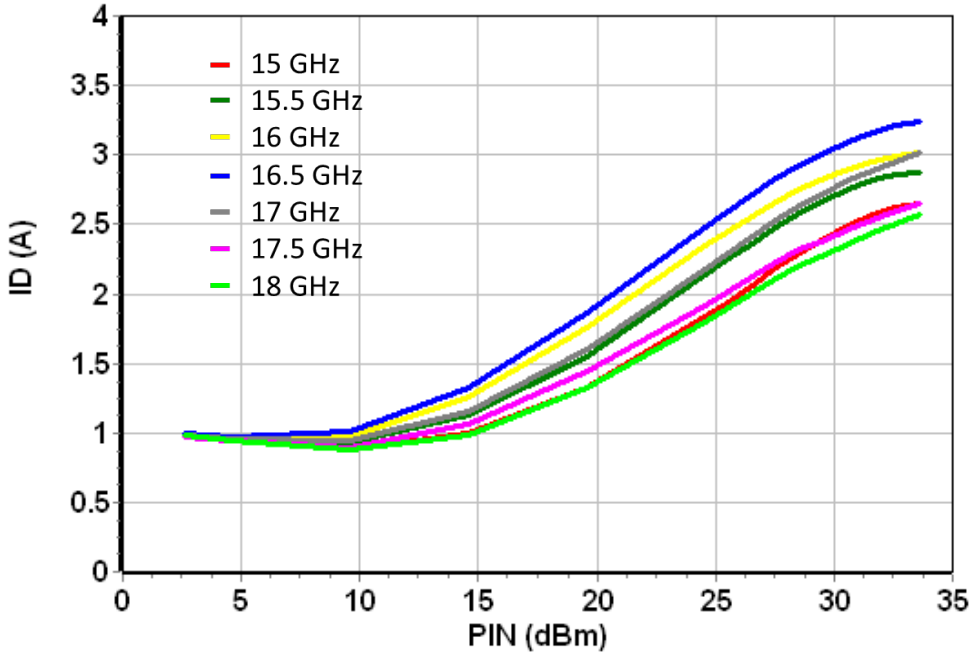
Typical Board Measurements (CW power measurements)

Tbackside = +25°C, Vd = 20V, Id = 1.16A@25°C
Board losses are de-embedded. Measurements are given in die access plans.

Gain (dB) versus Pin (dBm)



Id (A) versus Pin (dBm)



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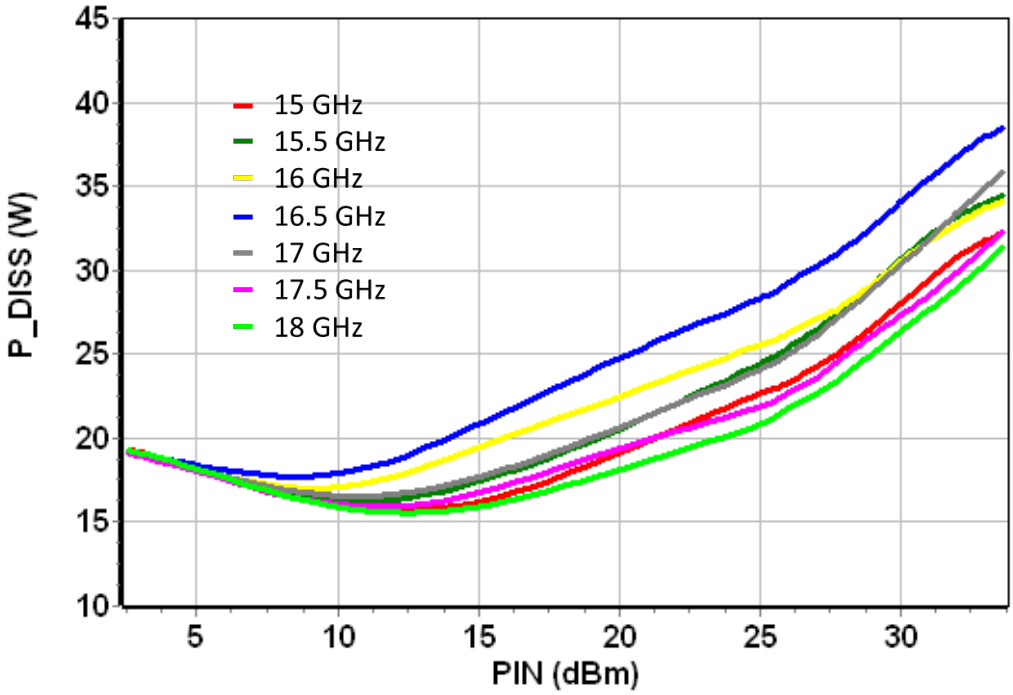
Typical Board Measurements (CW power measurements)

Tbackside = +25°C, Vd = 20V, Id = 1.16A@25°C
Board losses are de-embedded. Measurements are given in die access plans.

Pdiss (W) versus Pin (dBm)



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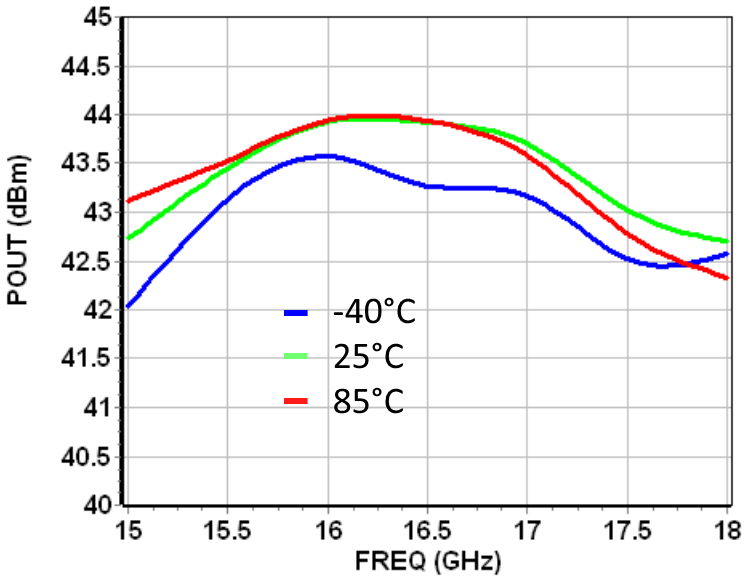
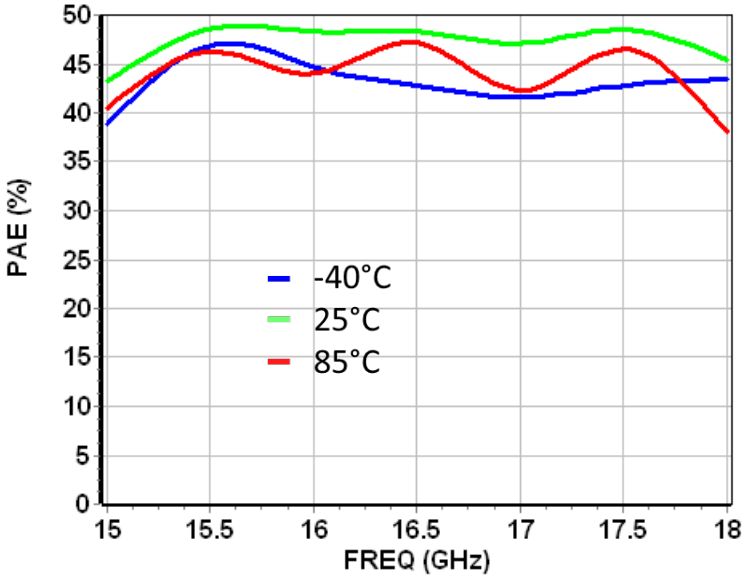
Typical Board Measurements (pulsed power measurements)

Tbackside = -40°C/+25°C/+85°C, Vd = 20V, Idq = 1.16A@25°C, 7 dB gain compression
Pulse width=25µs & Duty cycle =10%
Board losses are de-embedded. Measurements are given in die access plans.

Pout (dBm) versus frequency (GHz) for Tb=-40, +25 and +85°C



PAE (%) versus frequency (GHz) for Tb=-40, +25 and +85°C



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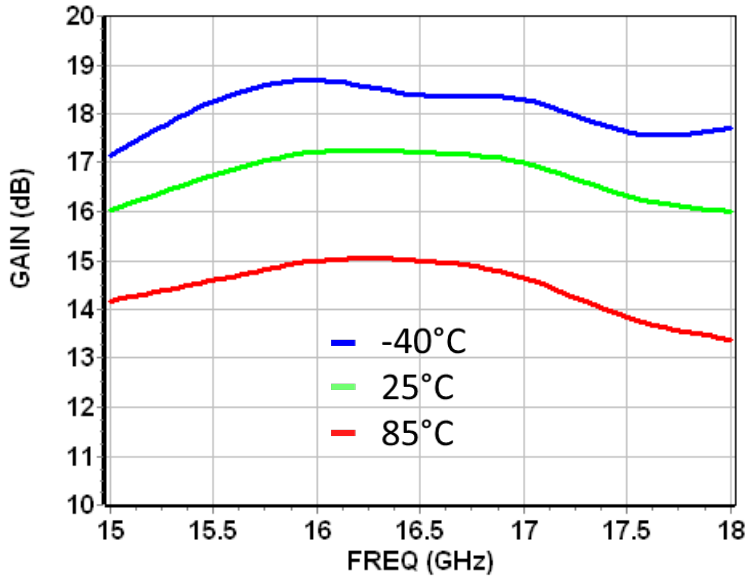
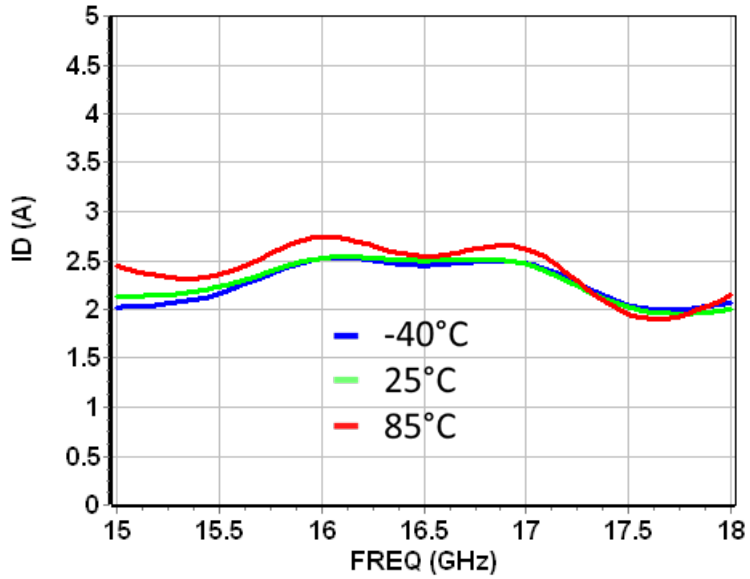
Typical Board Measurements (pulsed power measurements)

Tbackside = -40°C/+25°C/+85°C, Vd = 20V, Idq = 1.16A@25°C, 7 dB gain compression
Pulse width=25µs & Duty cycle =10%
Board losses are de-embedded. Measurements are given in die access plans.

Gain (dB) versus frequency (GHz) for Tb=-40, +25 and +85°C



Id (A) versus frequency (GHz) for Tb=-40, +25 and +85°C



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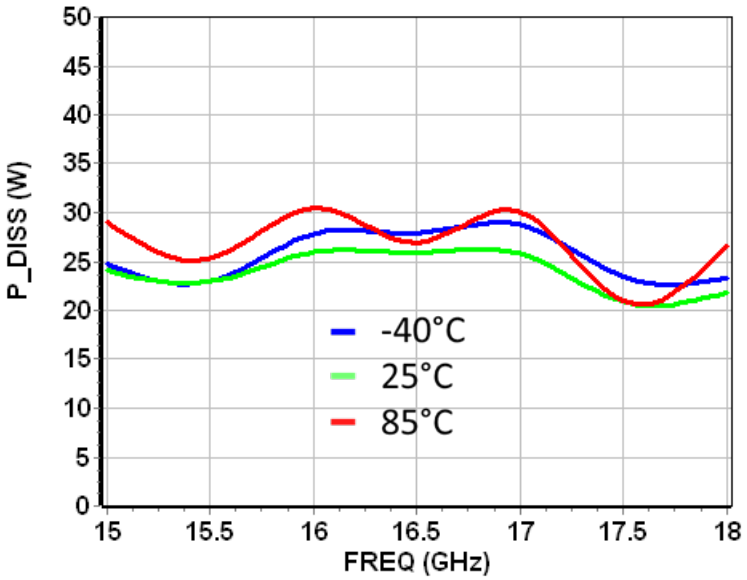
Typical Board Measurements (pulsed power measurements)

Tbackside = -40°C/+25°C/+85°C, Vd = 20V, Idq = 1.16A@25°C, Pin = 28dBm
Pulse width=25µs & Duty cycle =10%
Board losses are de-embedded. Measurements are given in die access plans.

Pdiss (W) versus frequency (GHz) for Tb=-40, +25 and +85°C



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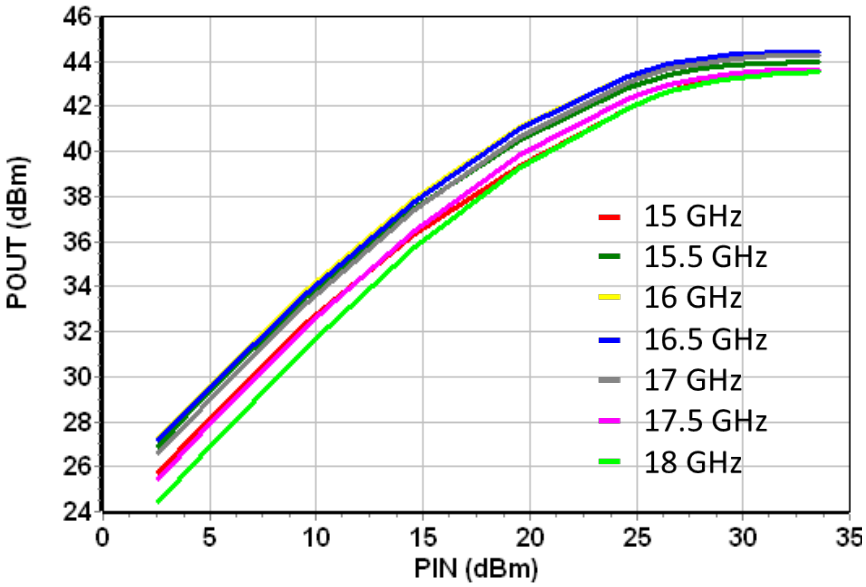
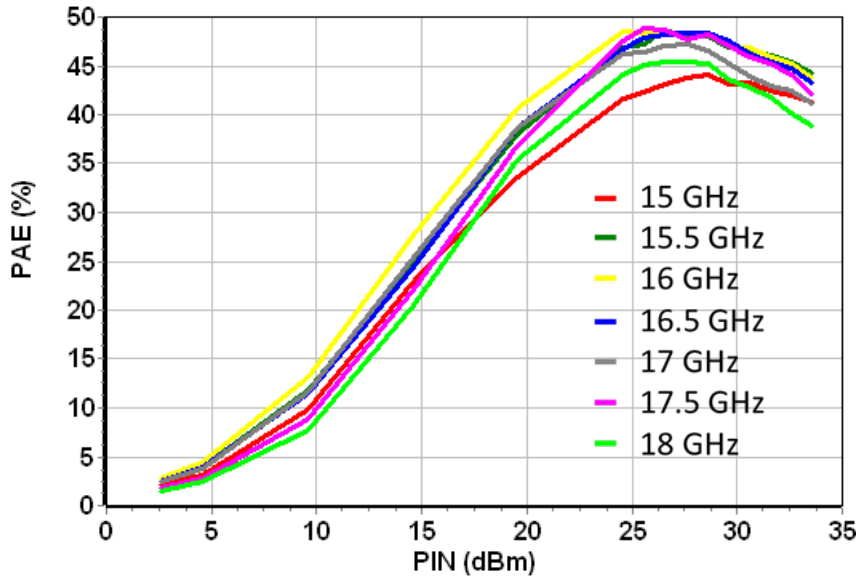
Typical Board Measurements (pulsed power measurements)

Tbackside = +25°C, Vd = 20V, Idq = 1.16A
Pulse width=25µs & Duty cycle =10%
Board losses are de-embedded. Measurements are given in die access plans.

Pout (dBm) versus Pin (dBm)



PAE (%) versus Pin (dBm)



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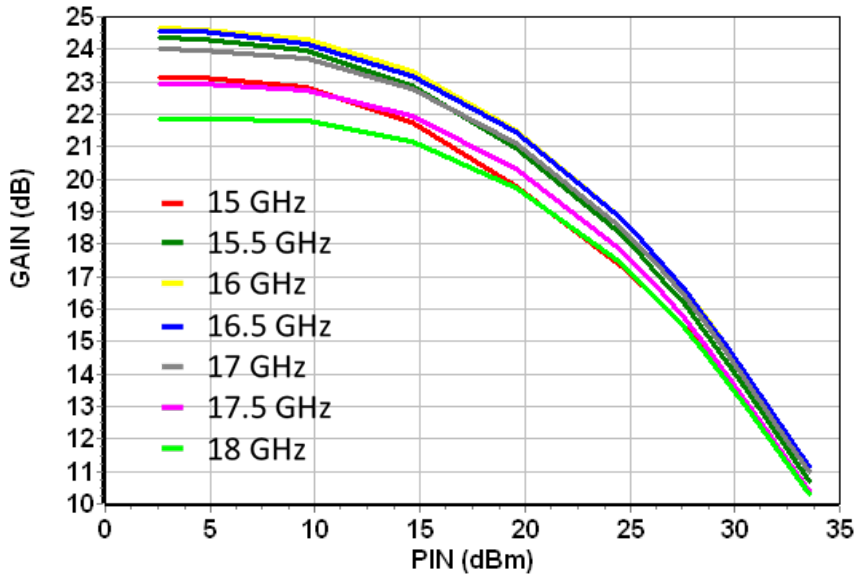
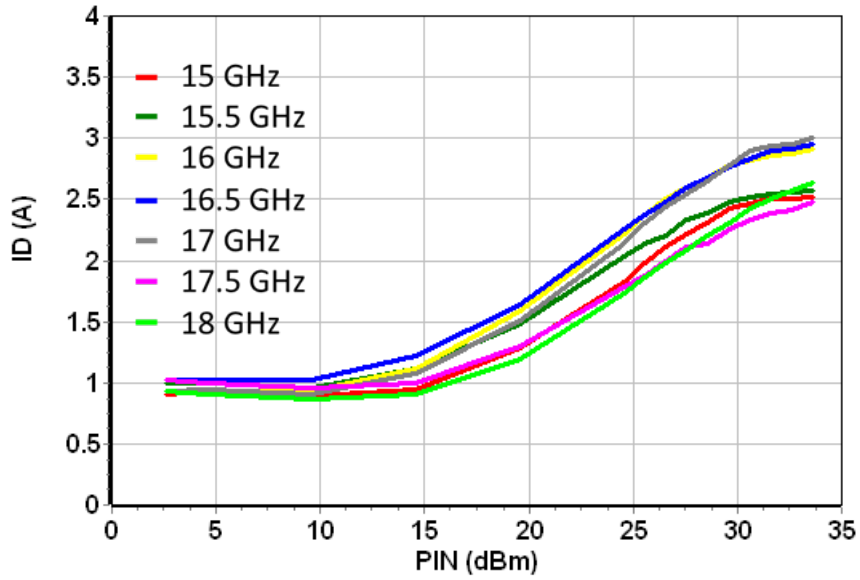
Typical Board Measurements (pulsed power measurements)

Tbackside = +25°C, Vd = 20V, Id = 1.16A @25°C
Pulse width=25µs & Duty cycle =10%
Board losses are de-embedded. Measurements are given in die access plans.

Gain (dB) versus Pin (dBm)



Id (A) versus Pin (dBm)



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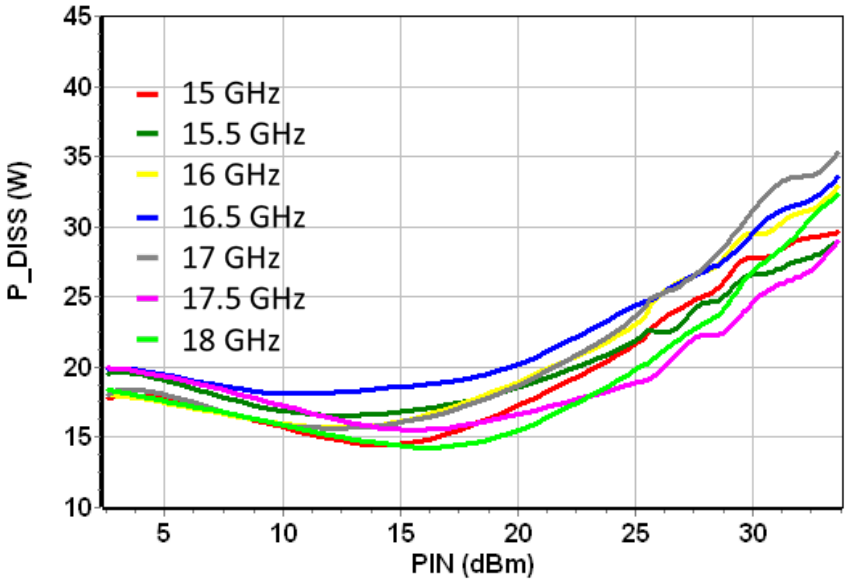
Typical Board Measurements (pulsed power measurements)

Tbackside = +25°C, Vd = 20V, Id = 1.16A@25°C
Pulse width=25µs & Duty cycle =10%
Board losses are de-embedded. Measurements are given in die access plans.

Pdiss (W) versus Pin (dBm)



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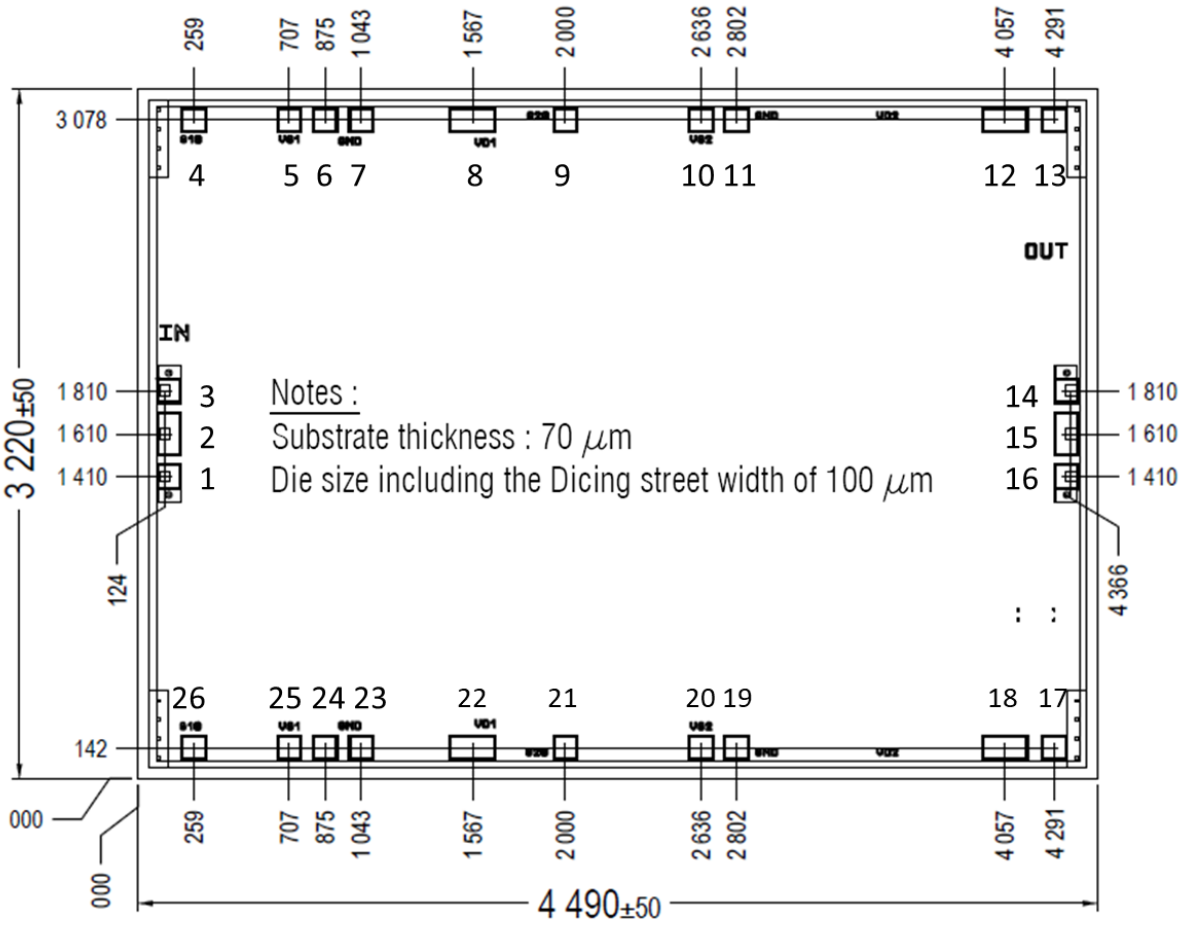
Chip mechanical data



Pad number	Pad name	Pad type	Description
4, 9, 21 & 26	NC	NC	Not connected
1, 3, 6, 7, 11, 13, 14, 16, 17, 19, 23, 24	GND	GND	Ground not connected
2	IN	RF IN	RF input signal
15	OUT	RF OUT	RF output signal
5 & 25	VG1	Supply	1st stage gate supply
10 & 20	VG2	Supply	2nd stage gate supply
8 & 22	VD1	Supply	1st stage drain supply
12 & 18	VD2	Supply	2nd stage drain supply

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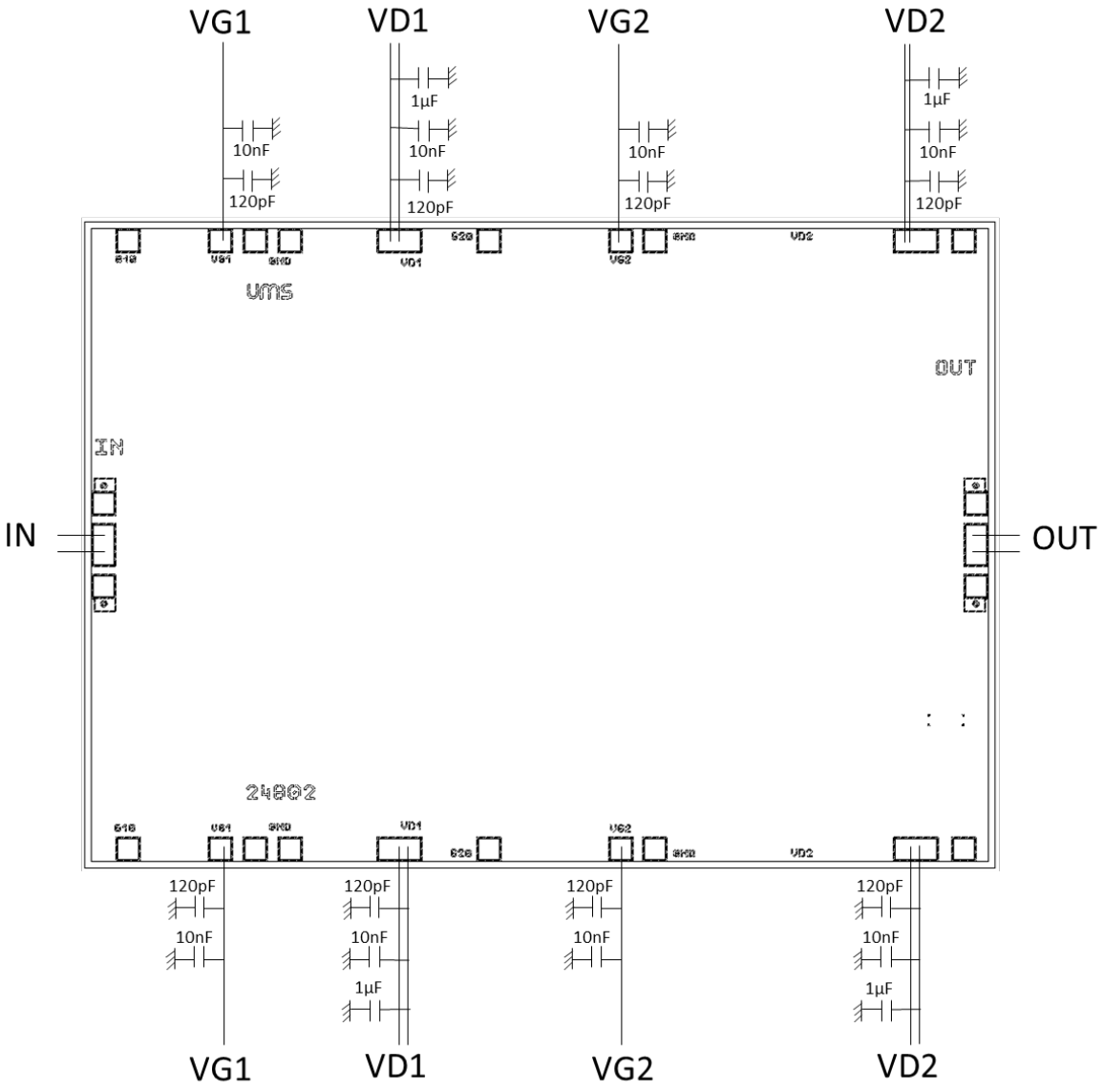
Recommended assembly plan

- Compatible with the proposed footprint.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 120pF, 10nF are recommended for gate accesses.
- For pulsed application, only decoupling capacitors of 120 pF are necessary on gate accesses.
- Decoupling capacitors of 120pF, 10nF and 1µF are recommended for drain accesses.
- See application note AN0030 for details.



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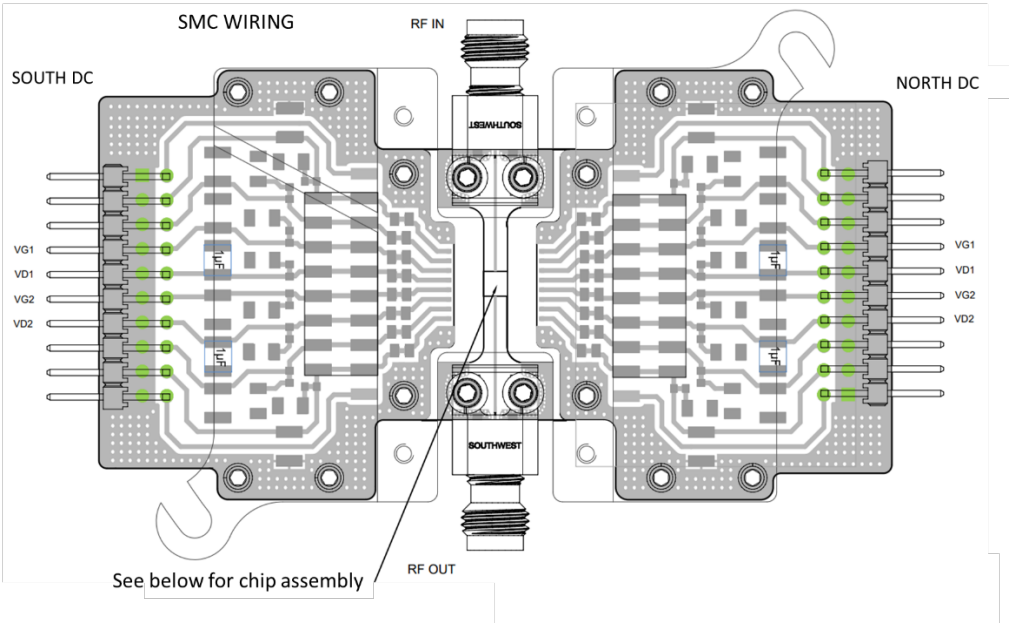
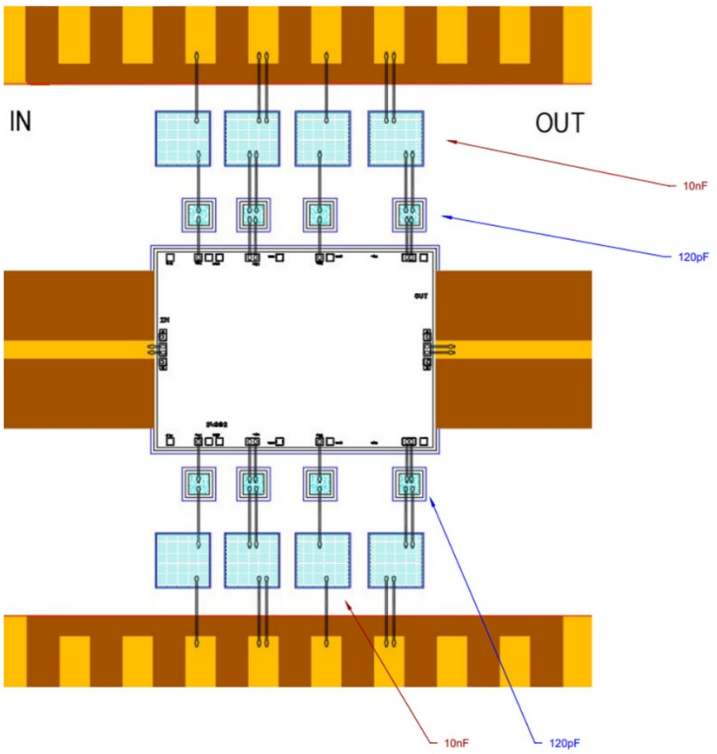
Evaluation board (EVB)

Three levels of decoupling capacitors have been used on the board.
The first level is composed of 120 pF chip capacitors. The second level is composed of 10nF chip capacitors. The third level on drain access is composed of 1µF capacitors. The first two levels should be as close as possible to the die. If bondwires are about 1 mm or longer for a 25µm diameter, use three bondwires on drain access.





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Recommended Evaluation board EVB assembly

Refer to the application note AN0030 available at https://www.ums-rf.com Evaluation board EVB.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at http://www.ums-rf.com.

Recommended ESD management

Refer to the application note AN0020 available at http://www.ums-rf.com for ESD sensitivity and handling recommendations.

Ordering Information

Chip form:	CHA8315-99F/00

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