9W 37-42GHz High Power Amplifier

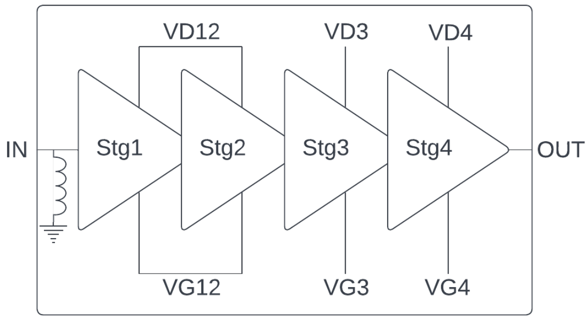
GaN Monolithic Microwave IC

Description

The CHA7453-99F is a four stages High Power Amplifier operating between 37 and 42GHz and providing typically 9W of saturated output power and 23% of Power Added Efficiency.The typical power supply is 20V/290mA (quiescent current). Thanks to a low drain voltage biasing, the CHA7453-99F provides a junction temperature below 160°C, even in saturation.

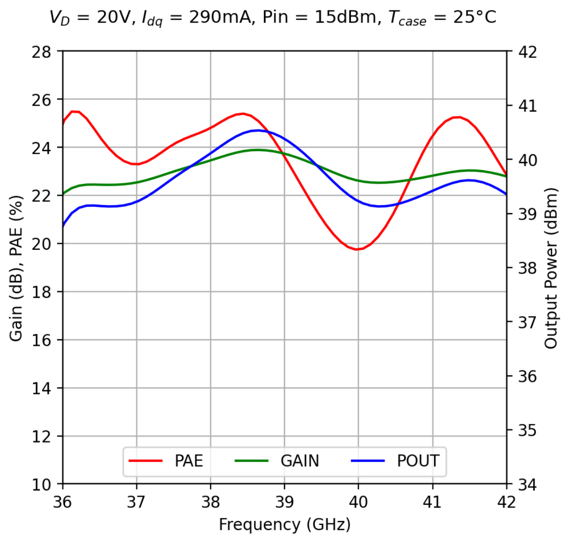
The circuit is manufactured on a space qualified GaN-on-SiC HEMT process and is available in bare die form.

It is firstly dedicated to space, military and telecom applications and well suited for a wide range of microwave applications and systems.



Main Features

- ■ Frequency range: 37 – 42GHz
- ■ High output power: 9W
- ■ High PAE: 23%
- ■ Linear Gain: above 24dB
- ■ DC bias: Vd=20V @Id=290mA
- ■ Chip size: 3.6x2.9mm²
- ■ Available in bare die



Main Electrical Characteristics

$T_{Backside}$ = +25°C (T_{case} : Chip backside temperature)

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	37.5		41.5	GHz
Gain	Linear Gain		28		dB
Pout	Saturated Output Power		39.5		dBm
PAE	Power Added Efficiency		23		%

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Specifications

$T_{Backside}$ = +25°C, Vd = +20V, CW excitation

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	37.5		41.5	GHz
Gain	Linear Gain		28		dB
Pout	Saturated Output Power		39.5		dBm
PAE	Power Added Efficiency		22		%
Id	Drain current at saturation		2.5		A
S11	Input Return Loss		-12		dB
S22	Output Return Loss		-8		dB
Idq	Quiescent Drain bias current		290		mA
Vd	Drain voltage		20		V

These values are representative of on-board measurements as defined on the drawing in paragraph "Recommended assembly plan".

Absolute Maximum Ratings (1)

$T_{Backside}$ = +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	27	V
Id	Quiescent Drain bias current	800	mA
Vg	Gate bias voltage	-7 to -1	V
Pin	Maximum Input Power	22	dBm

(1) Operation of this device above anyone of these parameters may cause permanent damage.

Recommended Operating Range (2), (3)

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	18 to 25	V
Id	Drain bias current	100 to 450	mA
Vg	Gate bias voltage	-5 to -2.5	V
Tj	Maximum Junction temperature (4)	200	°C

(2) Electrical performances are defined for specified test conditions

(3) Electrical performances are not guaranteed over all recommended operating conditions

(4) See Device thermal performances section

Temperature Range

$T_{Backside}$	Operating temperature range at MMIC backside level	-40 to +95	°C
T_{stg}	Storage temperature range	-55 to +150	°C

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Typical Bias Conditions

$T_{Backside}$=+25°C

Symbol	Pad N°	Parameter	Values	Unit
Vg	3, 5, 7, 25, 27, 29	Gate voltage tuned for Idq~290mA	-3.1	V
Vd	9, 11, 13, 19, 21, 23	Drain Voltage	20	V

"Power ON" sequence

1. Bias HPA gate voltage at Vg close to Vpinch-off (Vg~-5V)
2. Set Vd bias voltage to 0V: Id=0mA
3. Apply Vd bias voltage, Vd = 20V: Id=0mA
4. Set Vc bias voltage to 5V for Detector biasing
5. Increase Vg up to quiescent bias drain current Idq=216mA
6. Apply RF input Power

"Power OFF" sequence

1. Turn off RF input power
2. Bias HPA Gate voltage at Vg~-5V: Id=0mA
3. Decrease Vd bias voltage down to 0V
4. Set Vc bias voltage to 0V
5. Turn Vg bias voltage to 0V

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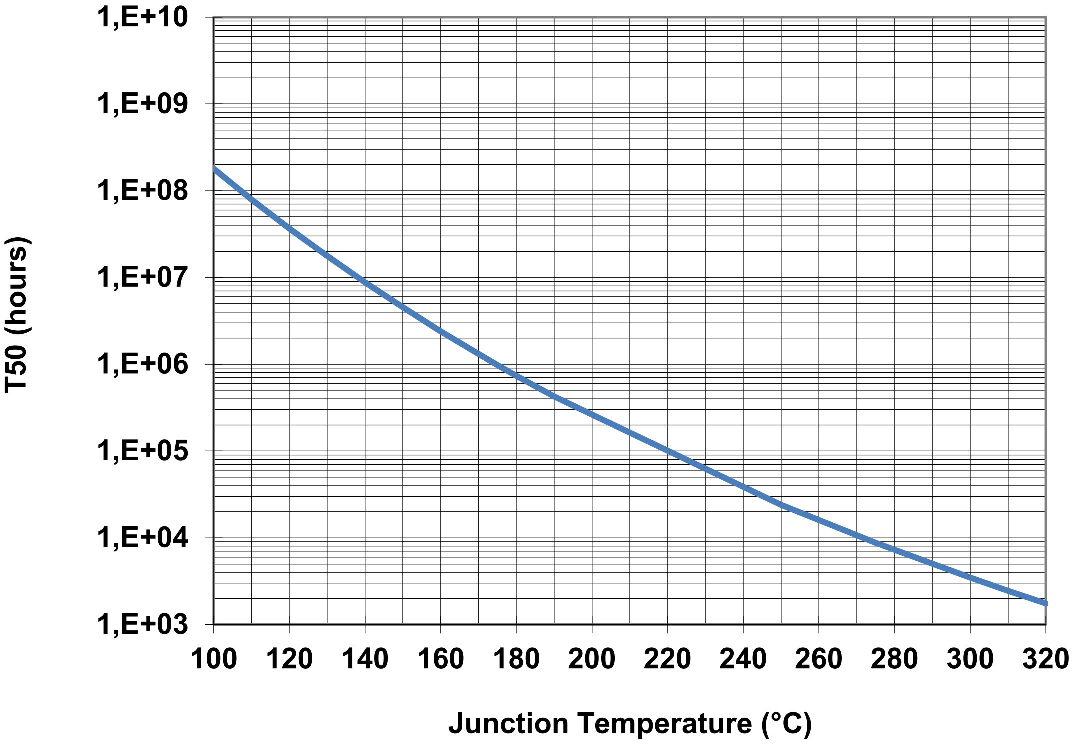
Device thermal performances

All the figures given in this section are obtained assuming that the device is only cooled down by conduction through the thermal pad (no convection mode considered).
The temperature is monitored at the chip back-side interface (Tcase).
For nominal operating, the system maximum temperature must be adjusted in order to guarantee that the Junction Temperature remains below the maximum value specified in the Recommended Operating Ratings table.
Therefore, the system PCB must be designed to comply with this requirement.

Thermal Resistance [1]	R_{th_eq}	$T_{Backside}$ = 85°C, Vd = 20V, Idq = 290 mA, Pin = 18 dBm, Freq = 41GHz, Pdiss = 28 W	2.36	°C/W
Junction Temperature	T_j		151	°C
Median Life	T50		3.5E6	Hrs

[1] Thermal resistance measured at the backside of the chip



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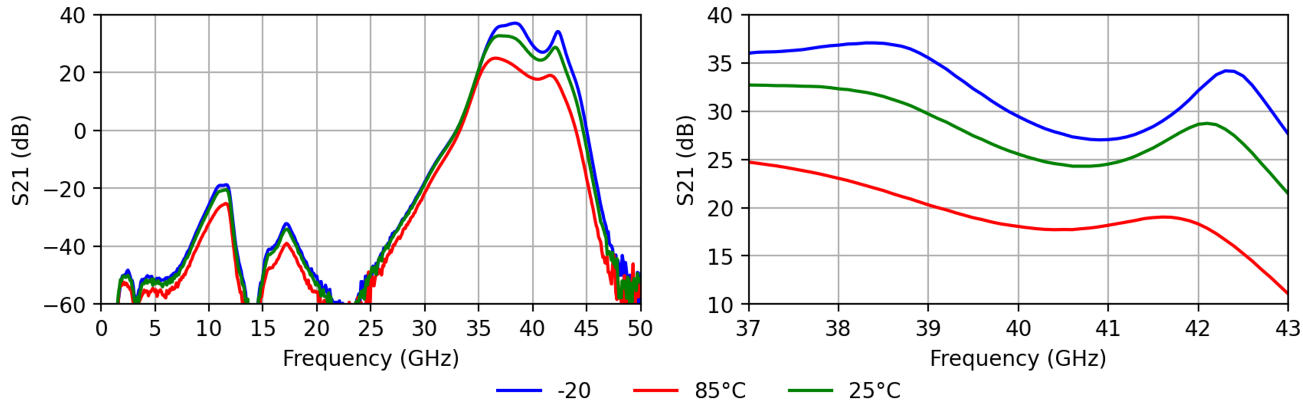
Typical Board Measurements : Small Signal Performances

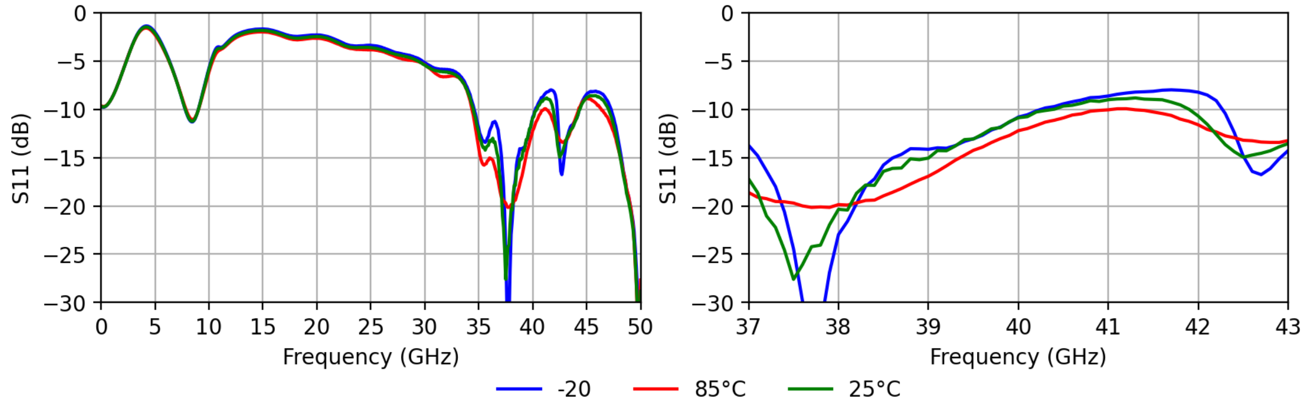
Measurements reference plane is de-embedded at the wire-bondings planes of the RF lines.

Performance versus frequency and temperature
Test conditions : V_D = 20V, I_{dq} = 290mA, $T_{Backside}$ = -20°C / 25°C / 85°C

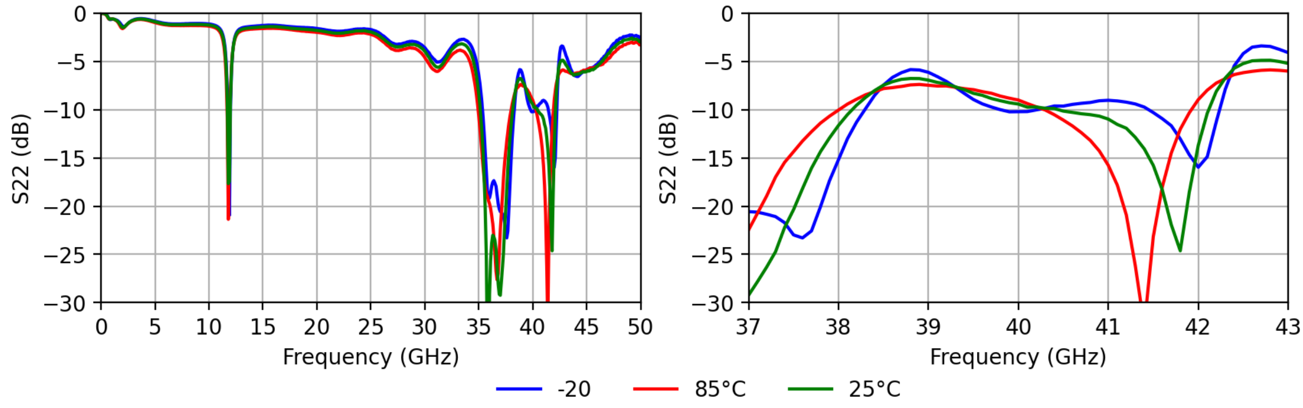
S21 versus Frequency and Temperature



S11 versus Frequency and Temperature



S22 versus Frequency and Temperature



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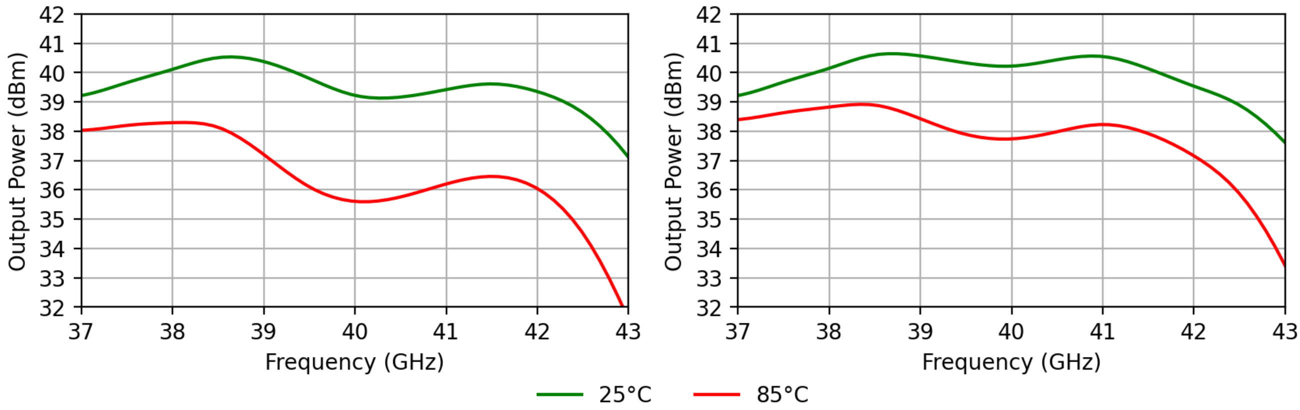
Typical Board Measurements : Large Signal Performances

Measurements reference plane is de-embedded at the wire-bondings planes of the RF lines.

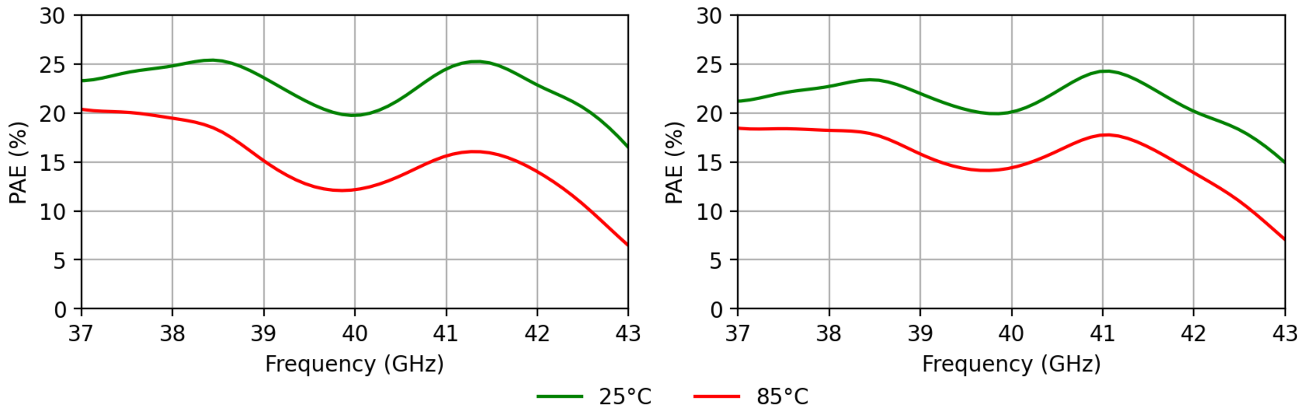
Performance versus frequency and temperature

Test conditions : V_D = 20V, I_{dq} = 290mA, $T_{Backside}$ = 25°C / 85°C

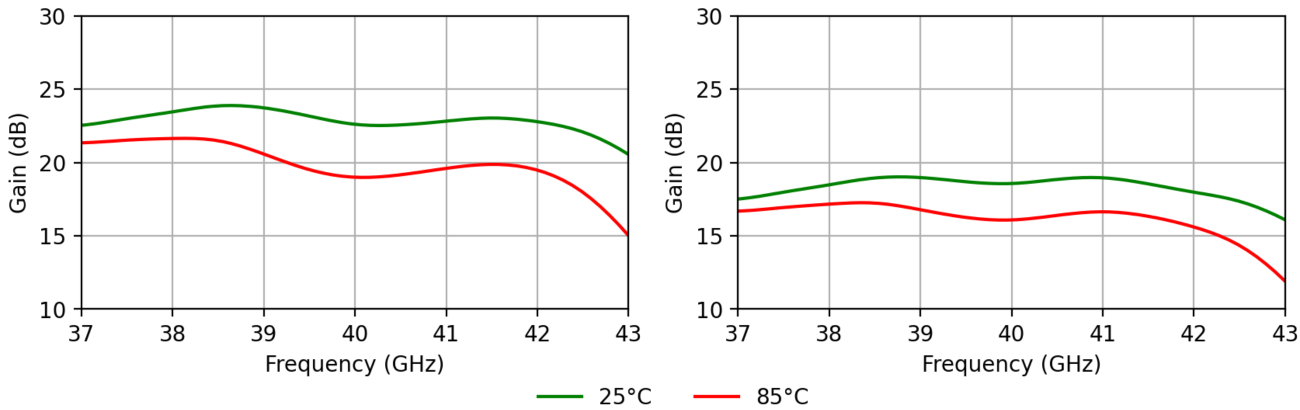
Output Power versus Frequency and Temperature



Power Added Efficiency versus Frequency and Temperature



Gain versus Frequency and Temperature



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Typical Board Measurements : Large Signal Performances

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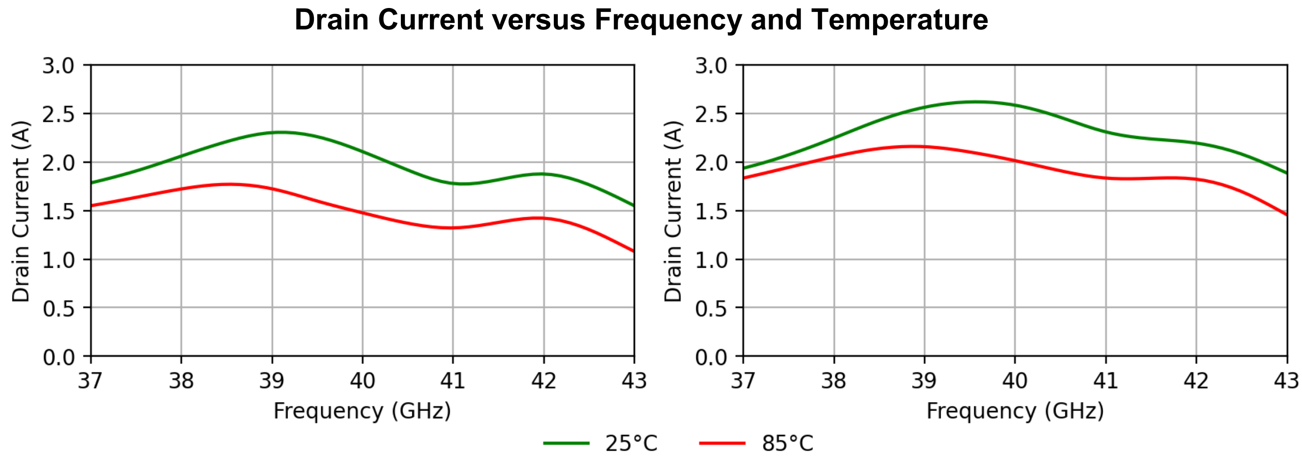
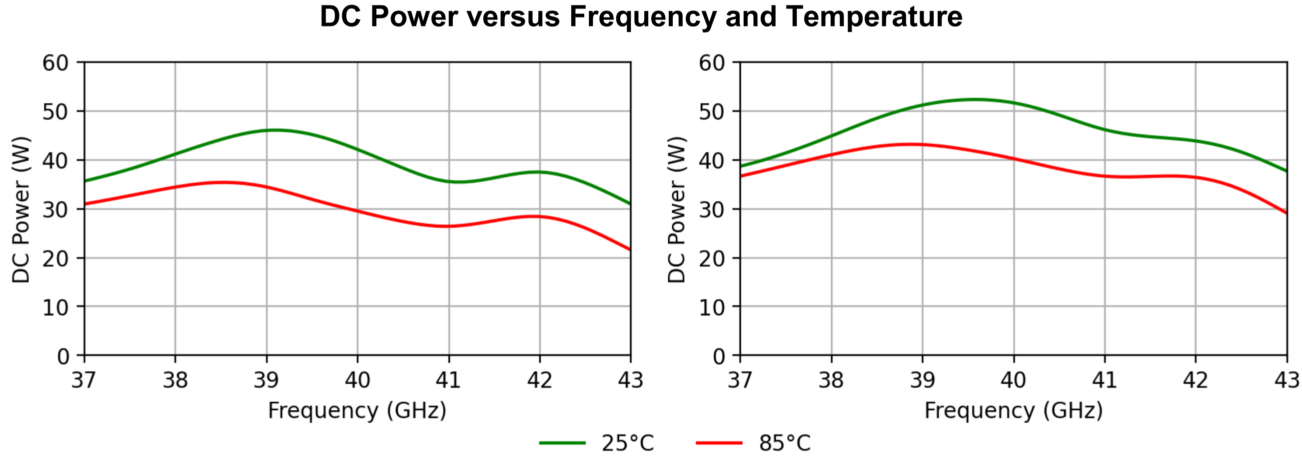
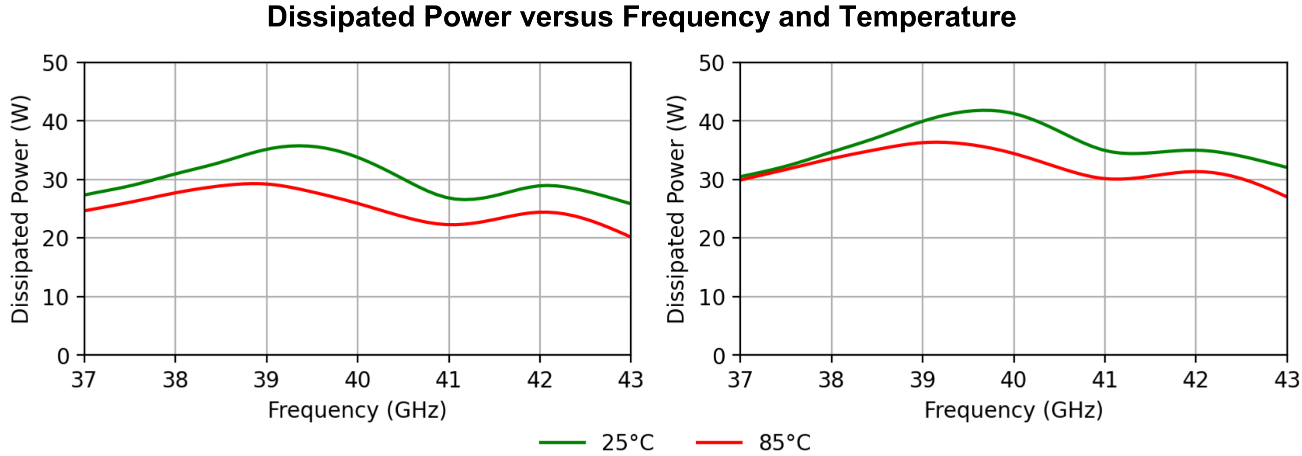
Performance versus frequency and temperature

Test conditions : V_D = 20V, I_{dq} = 290mA, $T_{Backside}$ = 25°C / 85°C







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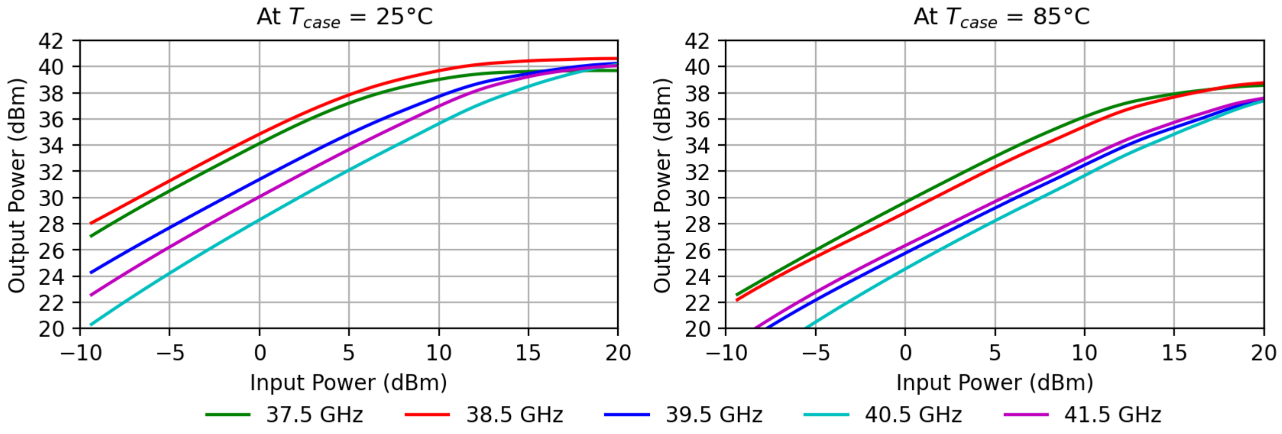
Typical Board Measurements : Large Signal Performances

Measurements reference plane is de-embedded at the wire-bondings planes of the RF lines.

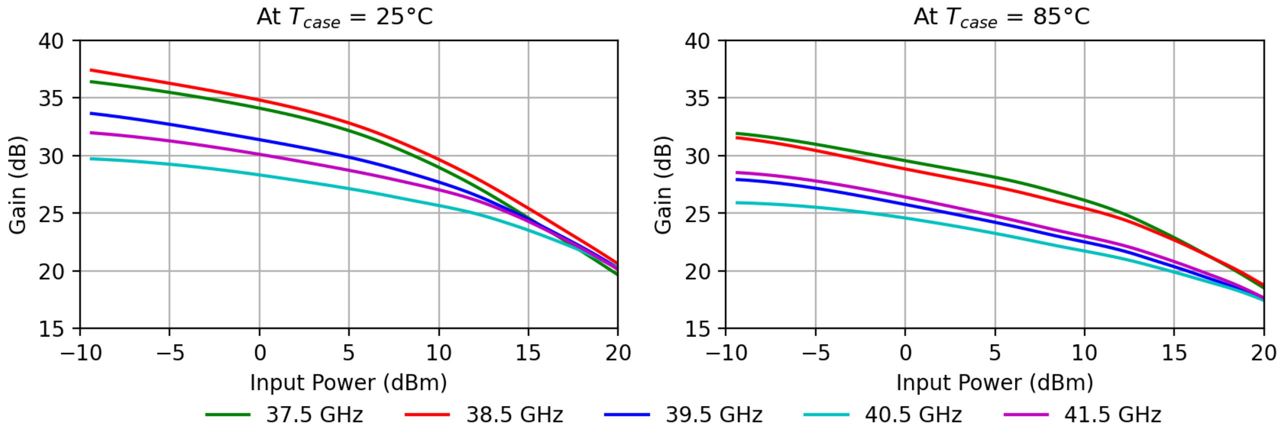
Performance versus Input Power and Frequency

Test conditions : V_D = 20V, I_{dq} = 290mA, $T_{Backside}$ = 25°C / 85°C

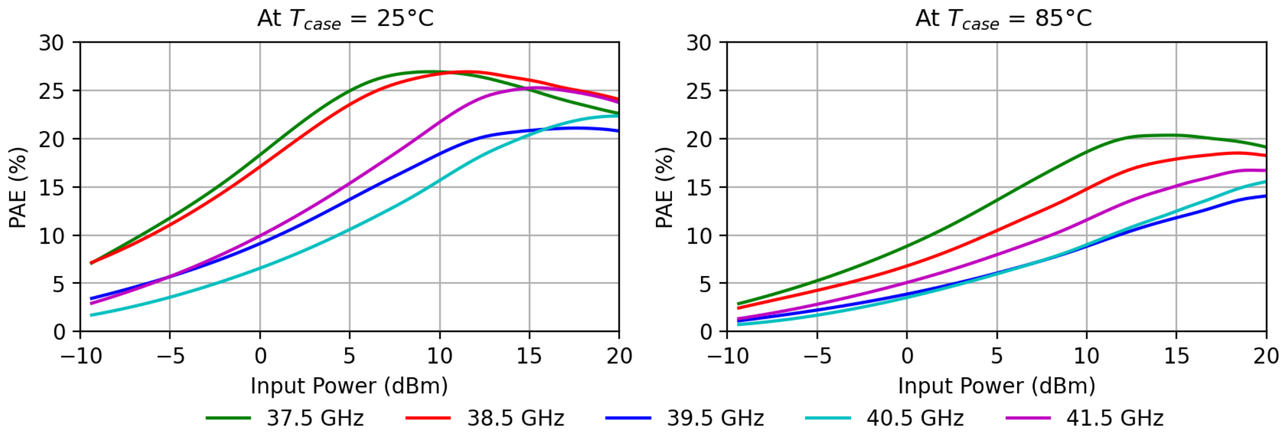
Output Power versus Input Power and Frequency



Gain versus Input Power and Frequency



Power Added Efficiency versus Input and versus Frequency



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Typical Board Measurements : Large Signal Performances

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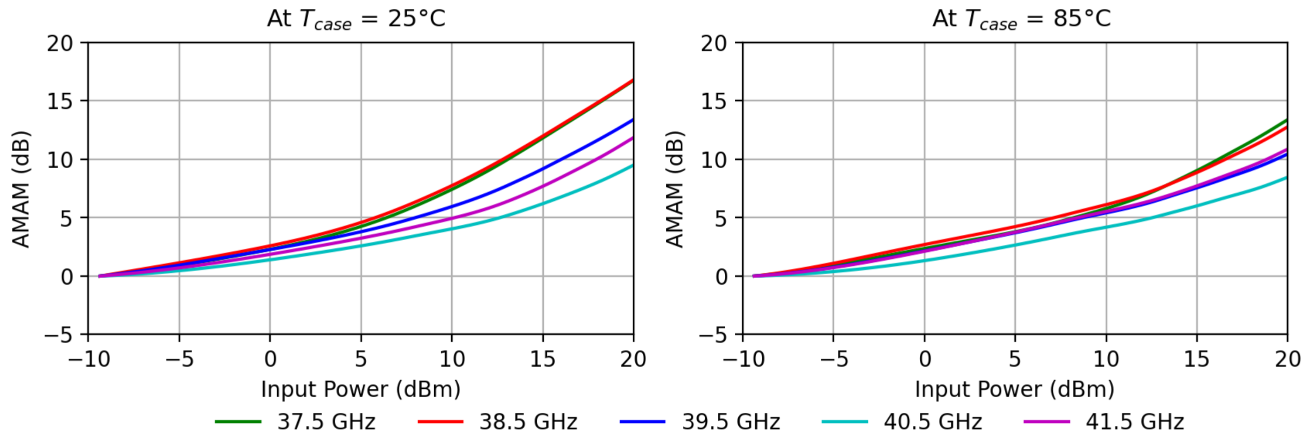
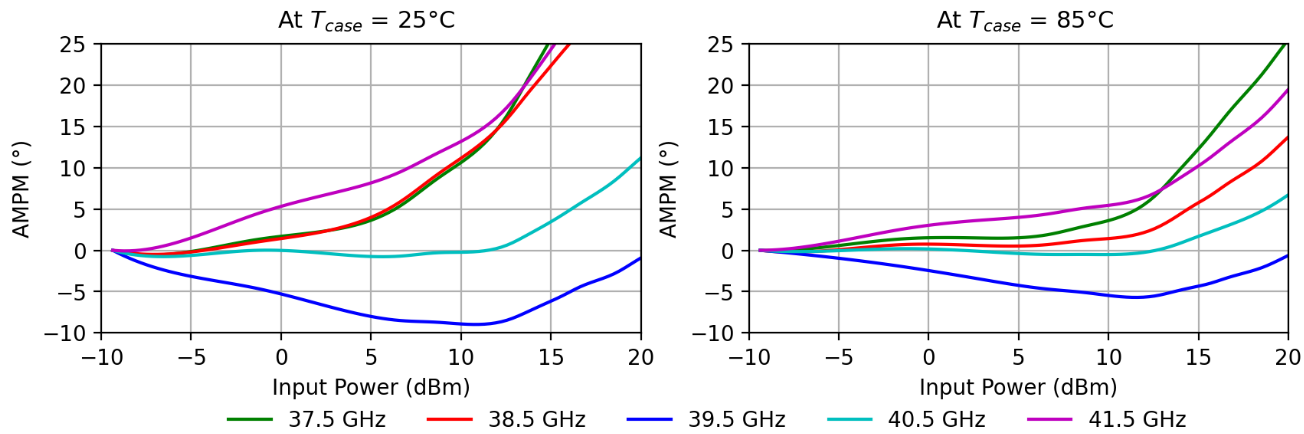
Performance versus Output Power and Frequency

Test conditions : V_D = 20V, I_{dq} = 290mA, $T_{Backside}$ = 25°C / 85°C

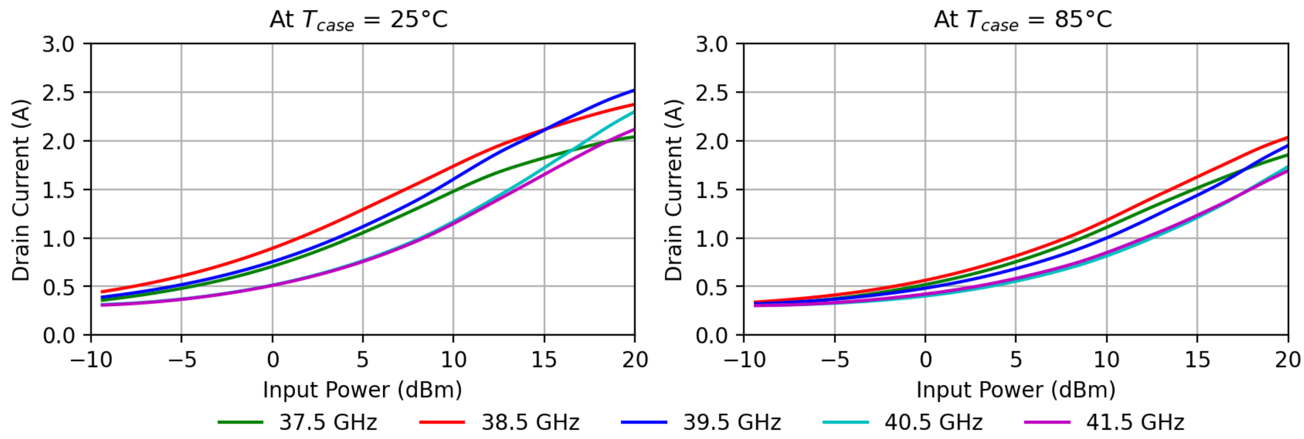
AMAM distortion versus Input Power and Frequency



AMPM versus Input Power and Frequency



Drain Current versus Input Power and Frequency



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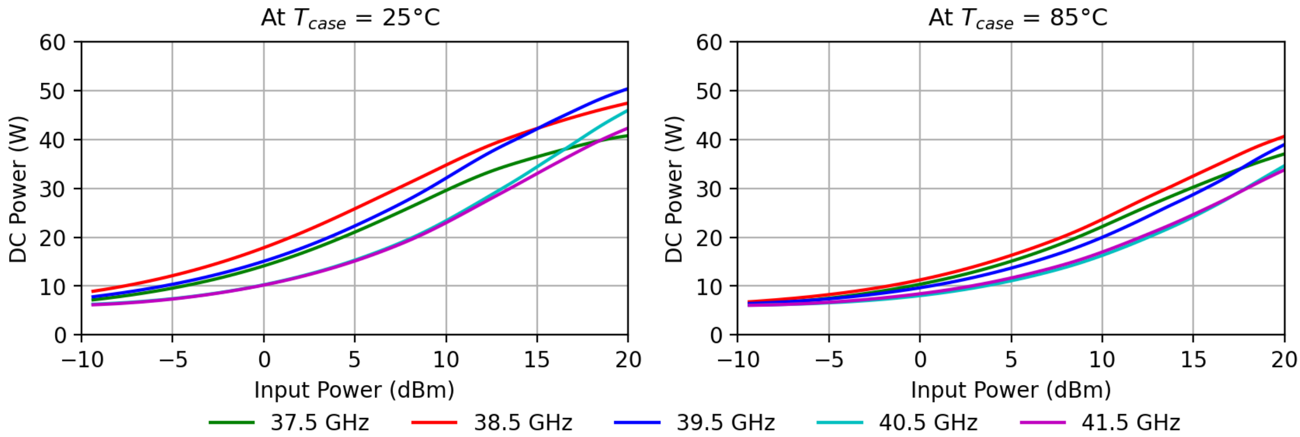
Typical Board Measurements : Large Signal Performances

Measurements reference plane is de-embedded at the wire-bondings planes of the RF lines.

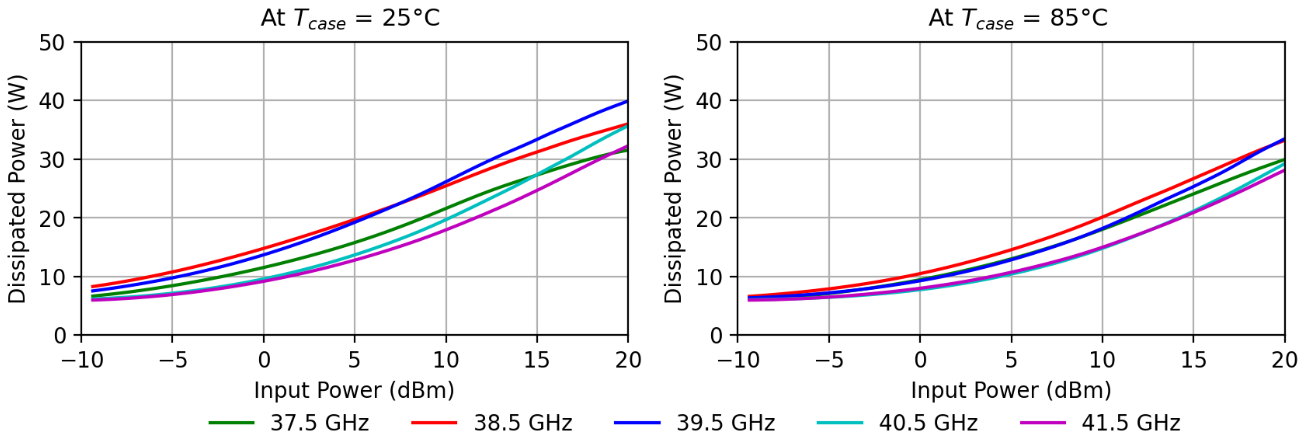
Performance versus Input Power and Frequency

Test conditions : V_D = 20V, I_{dq} = 290mA, $T_{Backside}$ = 25°C / 85°C

DC Power versus Input Power and Frequency



Dissipated Power versus Input Power and Frequency



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Typical Board Measurements : Large Signal Performances

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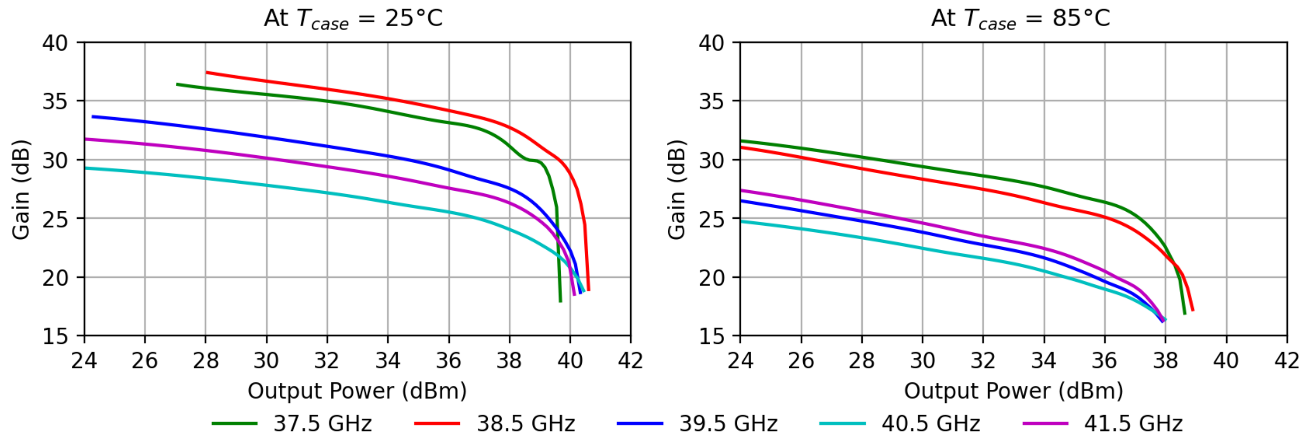
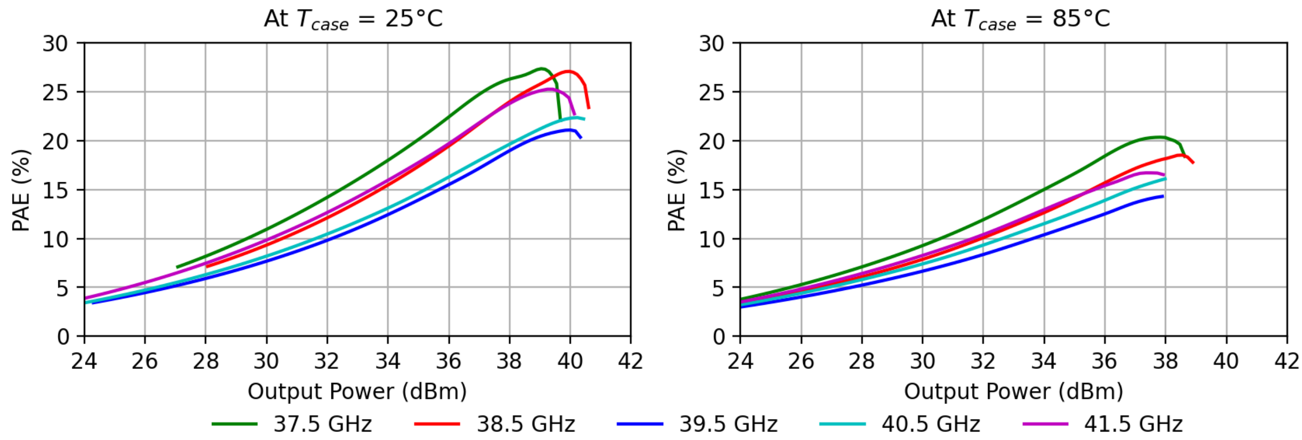
Performance versus Output Power and Frequency

Test conditions : V_D = 20V, I_{dq} = 290mA, $T_{Backside}$ = 25°C / 85°C

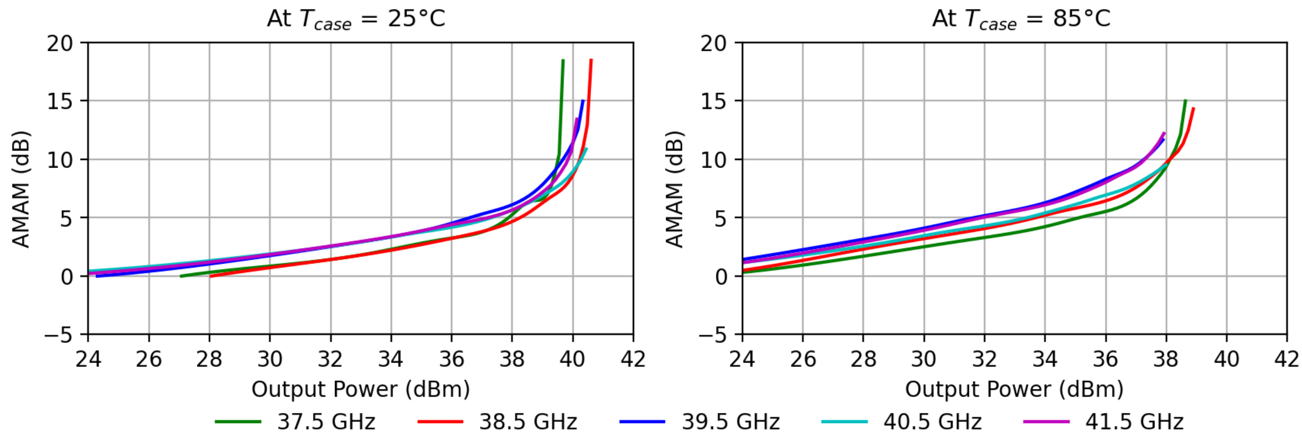
Gain versus Output Power and Frequency



Power Added Efficiency versus Output Power and Frequency



AMAM distortion versus Output Power and Frequency



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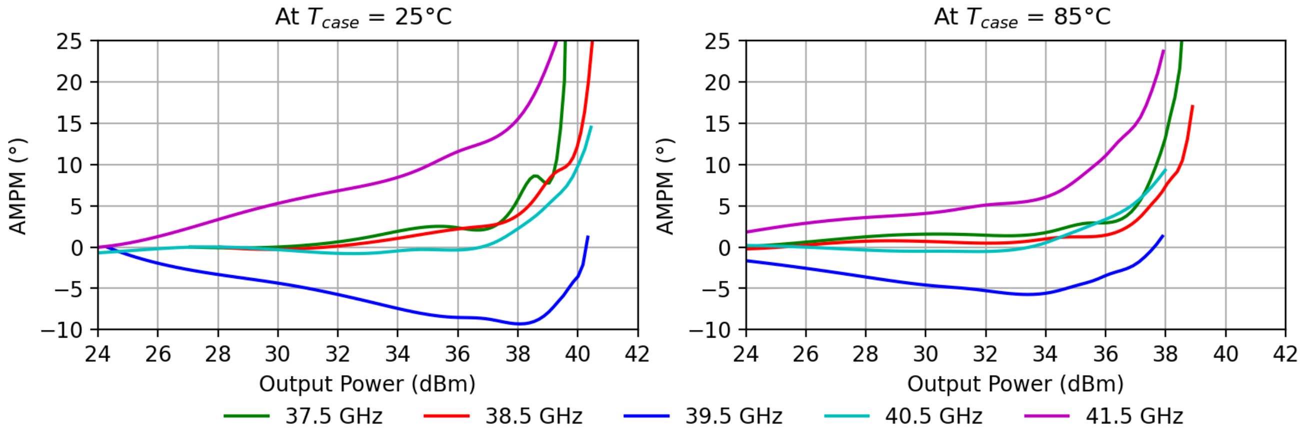
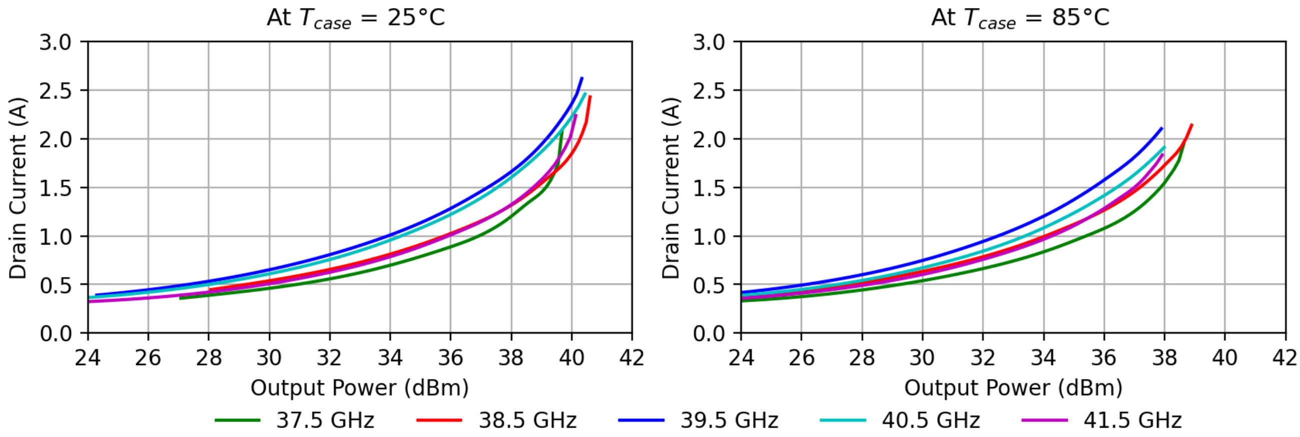
Performance versus Output Power and Frequency

Test conditions : V_D = 20V, I_{dq} = 290mA, $T_{Backside}$ = 25°C / 85°C

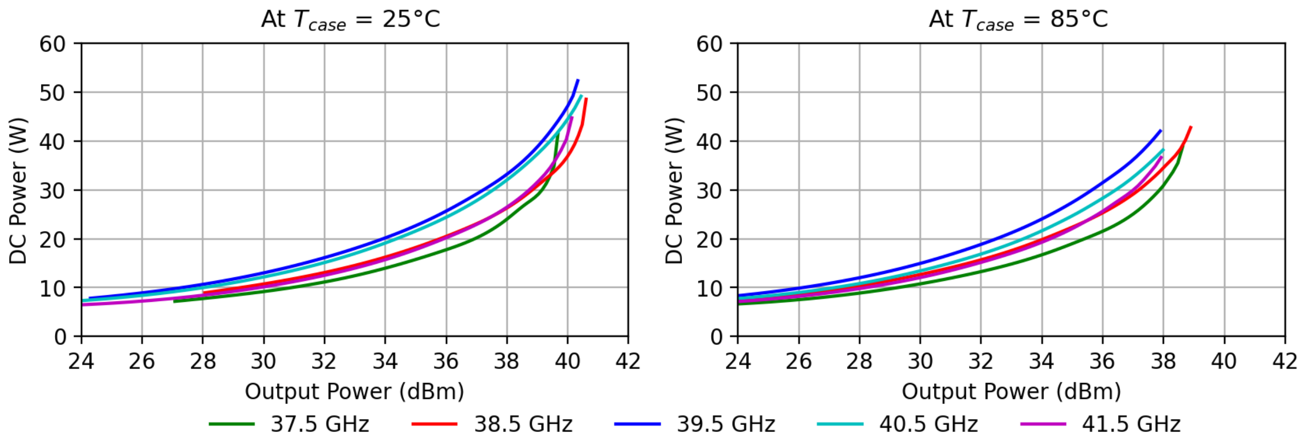
AMPM distortion versus Output Power and Frequency



Drain Current versus Output Power and Frequency



DC Power versus Output Power and Frequency



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Typical Board Measurements : Large Signal Performances

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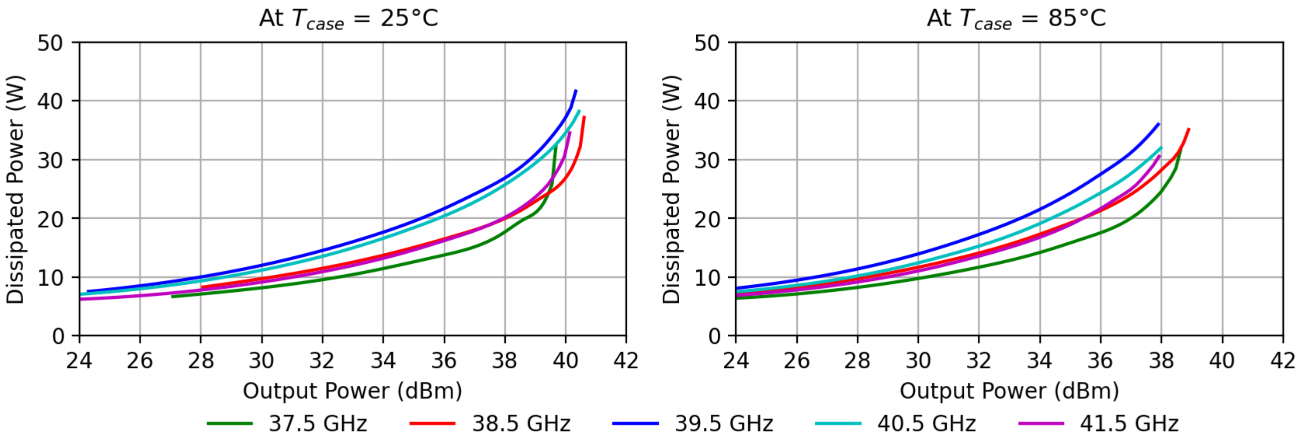
Performance versus Output Power and Frequency

Test conditions : V_D = 20V, I_{dq} = 290mA, $T_{Backside}$ = 25°C / 85°C

Dissipated Power versus Output Power and Frequency



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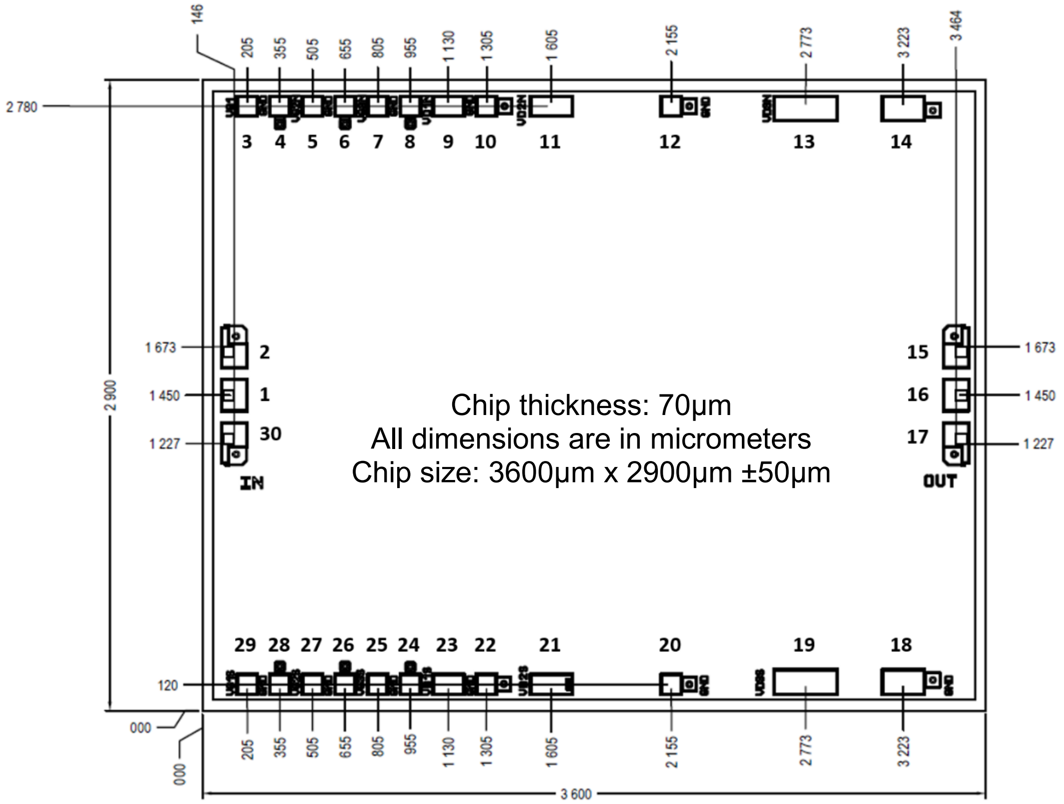
Mechanical Data



PAD Number	Name	Description	Pad size
1	RF IN	Input RF port	186µm x 105µm
3	G12	DC Gait voltage, 1st & 2st stage, North	96µm x 96µm
5	G3	DC Gate voltage 3d stage, North	96µm x 96µm
7	G4	DC Gate voltage 4th stage, North	96µm x 96µm
9	D12	DC Drain voltage, 1st & 2st stage, North	146µm x 96µm
11	D3	DC Drain voltage 3d stage, North	196µm x 96µm
13	D4	DC Drain voltage 4th stage, North	296µm x 116µm
16	RF OUT	Output RF port	118 µm x146 µm
19	D4	DC Drain voltage 4th stage, South	296µm x 116µm
21	D3	DC Drain voltage 3d stage, South	196µm x 96µm
23	D12	DC Drain voltage, 1st & 2st stage, South	146µm x 96µm
25	G4	DC Gate voltage 4th stage, South	96µm x 96µm
27	G3	DC Gate voltage 3d stage, South	96µm x 96µm
29	G12	DC Gait voltage, 1st & 2st stage, South	96µm x 96µm
2,4,6,8,10,12,14 ,15,17,18,20,22, 24,26,28,30	GND	Ground	96µm x 96µm

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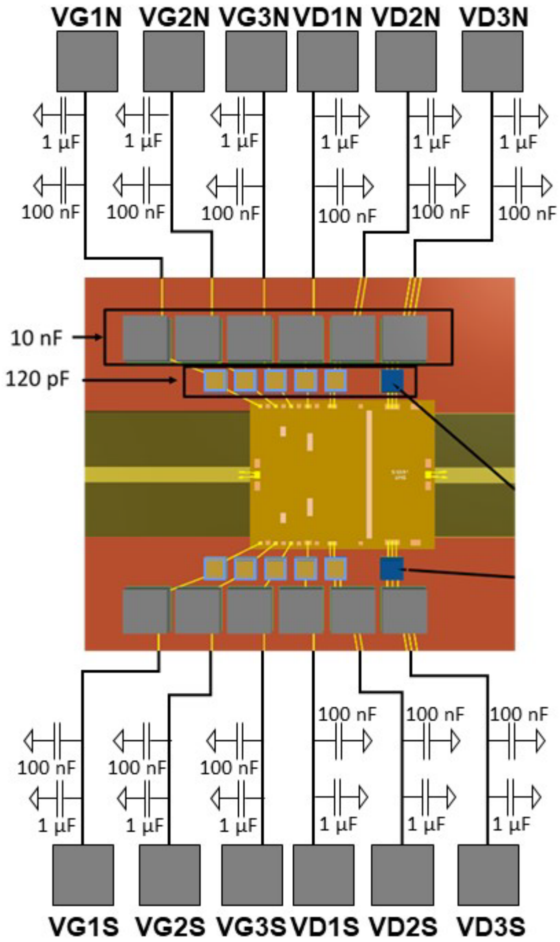
Recommended Assembly Plan



4 levels of decoupling capacitor have been used, 2 on the tab and 2 on the board. The first level is composed of 120 pF chip capacitors, the second level is composed of 10nF chip capacitors, the third level is composed of 100nF SMD 1210 capacitors and the fourth stage is composed of 1µF SMD 1206 capacitors. The first two levels should be as close as possible to the die.

ESD Sensitivity

Parameter	Classification	Standard
Human Body Model (HBM)	1A	ANSI/ESDA/JEDEC - JS-001

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Recommended reflow process assembly

Refer to the application note AN0001 available at https://www.ums-rf.com for die attach.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at https://www.ums-rf.com.

Recommended ESD management

Refer to the application note AN0020 available at https://www.ums-rf.com for ESD sensitivity and handling recommendations for the UMS products.

Ordering Information

Chip form : CHA7453-99F/00

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