

## 10-12.75GHz High Power Amplifier

### GaN Monolithic Microwave IC in SMD leadless package

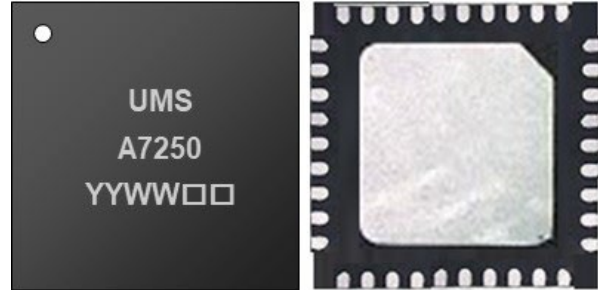
#### Description

The CHA7250-QAB is a two stage monolithic GaN Power Amplifier exhibiting 10W saturated output power over 10-12.75GHz frequency range.

It features 37% Power Added Efficiency and a linear gain of 20dB.

The circuit is realized on Gallium Nitride on Silicon Carbide (AlGaN/GaN on SiC) technology.

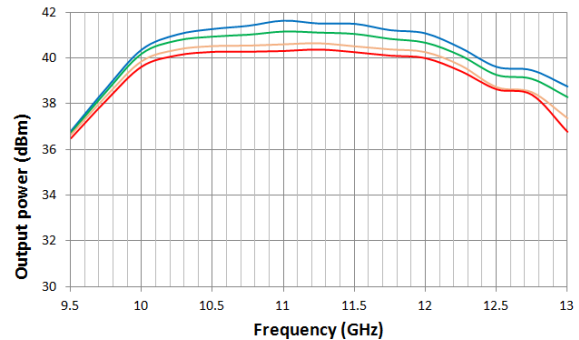
It is designed for Point To Point Radio and is provided on low cost SMD RoHS compliant plastic package.



#### Main Features

- RF bandwidth: 10-12.75GHz
- Gain: 20dB
- Psat: 40dBm
- PAE: 37% @28dBm Pin
- DC bias: Vd = 20V @ Idq = 130mA
- 38 leads QFN 6x6mm<sup>2</sup>
- MSL3

Output power at Pin=28dBm vs Frequency & temperature  
Tcase: -30°C 25°C 75°C 95°C



#### Main Electrical Characteristics

T<sub>case</sub> (QFN backside temperature) = +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	10		12.75	GHz
Gain	Linear Gain		20		dB
P <sub>sat</sub>	Saturated output power		40		dBm
Idq	Total drain current		130		mA

## Specifications

$T_{case} = +25^{\circ}\text{C}$ ,  $V_d = +20\text{V}$ ;  $I_{dq} = 130\text{mA}$

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	10		12.75	GHz
Gain	Linear Gain		20		dB
RL <sub>in</sub>	Input return loss		11		dB
RL <sub>out</sub>	Output return loss		10		dB
Psat	Saturated output Power		40		dBm
Vdetect	Voltage detection $V_{REF} - V_{DET}$ up to Psat		5 to 2500		mV
Pdc@32dBm	DC power consumption @ Pout=32dBm		12		W

These values are representative of on board measurements as defined on the drawing in paragraph "Evaluation board".

### “Power ON” sequence

1. Ground the device
2. Bias HPA gate voltage at Vg low enough (Typically:  $V_g \approx -5\text{V}$ )
3. Apply Vd bias voltage (Typically:  $V_d = 20\text{V}$ )
4. Apply Vc bias voltage (Typically:  $V_c = 6\text{V}$ )
5. Increase slowly Vg up to quiescent bias drain current Idq
6. Apply RF signal

### “Power OFF” sequence

1. Turn off RF signal
2. Bias HPA gate voltage at Vg low enough (Typically:  $V_g \approx -5\text{V}$ )
3. Turn Vd bias voltage to 0V
4. Turn Vc bias voltage to 0V
5. Turn Vg bias voltage to 0V

**Absolute Maximum Ratings** <sup>(1)</sup>T<sub>case</sub> = +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	27V	V
Id	Drain bias current (no RF)	480	mA
Vg	Gate bias voltage	-7 to -2.6	V
Vc	Detector Control Voltage	7	V
Pin	Maximum peak input power	+30	dBm

<sup>(1)</sup> Operation of this device above anyone of these parameters may cause permanent damage.

**Recommended Operating Range** <sup>3, 4</sup>

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	18 to 25	V
Id	Drain bias current (no RF)	130 to 260	mA
Vg	Gate bias voltage	-5 to -2.9	V
Vc	Detector Control Voltage	6	V
Pin	Maximum peak input power overdrive	28	dBm

<sup>(3)</sup> Electrical performances are defined for specified test conditions

<sup>(4)</sup> Electrical performances are not guaranteed over all recommended operating conditions

**Temperature Range**

T <sub>case</sub>	Operating temperature range	-30 to +95	°C
T <sub>stg</sub>	Storage temperature range	-55 to +150	°C

**Typical Bias Conditions**T<sub>case</sub> = +25°C

Symbol	Pad N°	Parameter	Values	Unit
VG1	11, 37	DC Gate voltage 1 <sup>st</sup> stage	-3	V
VG2	14, 34	DC Gate voltage 2 <sup>nd</sup> stage	-3	V
VD1	13, 35	DC Drain voltage 1 <sup>st</sup> stage	20	V
VD2	16, 32	DC Drain voltage 2 <sup>nd</sup> stage	20	V
VC	18, 30	DC control voltage of detector	6	V

## Device thermal performances

All the figures given in this section are obtained assuming that the die is only cooled down by conduction through the package case.

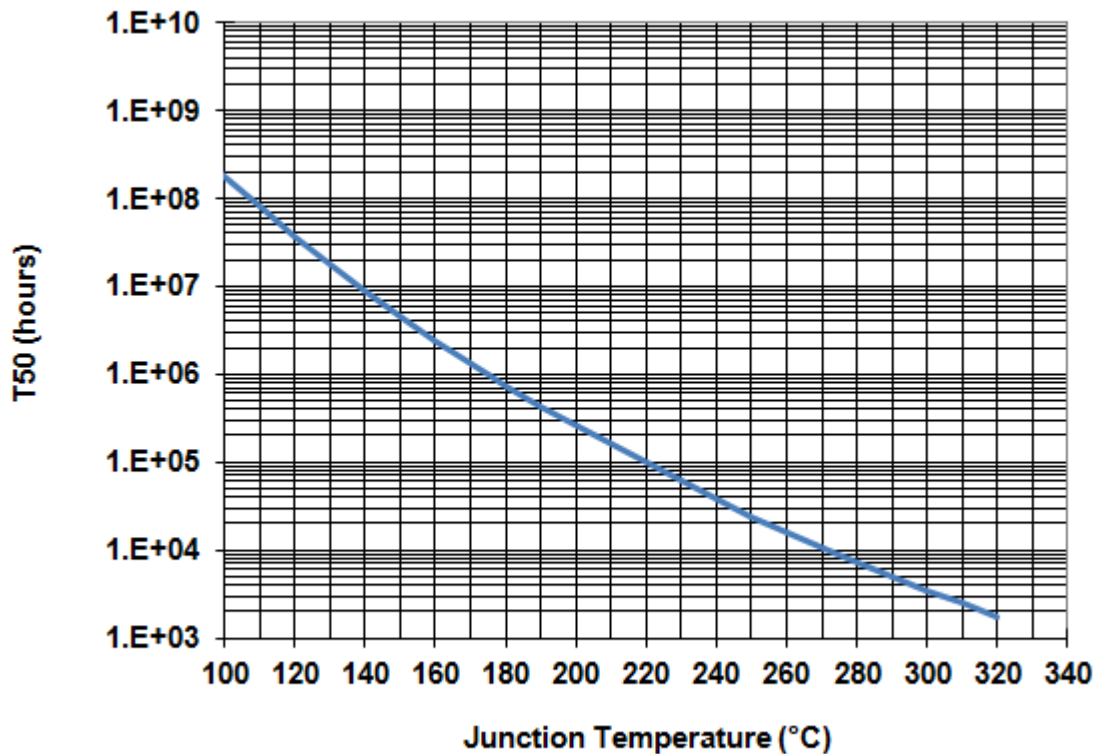
The temperature is monitored at the QFN back-side interface ( $T_{case}$ ).

For nominal operating, the system maximum temperature must be adjusted in order to guarantee that  $T_{junction}$  remains below the maximum value specified in the Recommended Operating Ratings table.

So, the system PCB must be designed to comply with this requirement.

Parameter	Biassing conditions	Tjunction (°C)	RTH (°C/W)	T50 (hours)
RTH <sup>(1)</sup> Thermal Resistance (Junction to Case)	Vd = 20V Pout = 32dBm Pdiss = 8.36W CW	151	6.70	4.24E+6

<sup>(1)</sup> Assuming 95°C  $T_{case}$



**Typical Package Sij parameters**T<sub>case</sub> = +25°C, V<sub>d</sub> = +20V, I<sub>d</sub> = 130mA

Freq (GHz)	S11 (dB)	PhS11 (°)	S12 (dB)	PhS12 (°)	S21 (dB)	PhS21 (°)	S22 (dB)	PhS22 (°)
2.5	-1.032	120.6	-69.778	79.2	-64.848	77.0	-0.261	-159.8
3	-1.168	108.1	-69.529	64.7	-64.247	79.1	-0.298	-178.5
3.5	-1.429	95.3	-67.353	53.2	-60.098	97.7	-0.333	164.8
4	-1.707	82.9	-66.673	28.6	-53.150	91.8	-0.391	149.3
4.5	-1.831	69.6	-66.586	16.7	-47.841	62.0	-0.469	134.4
5	-1.999	54.5	-66.008	1.9	-46.029	32.0	-0.561	120.0
5.5	-2.172	38.3	-67.459	-22.7	-46.473	27.1	-0.671	106.5
6	-2.408	20.2	-70.114	-42.5	-42.323	48.6	-0.657	92.3
6.5	-2.672	0.2	-73.488	-62.5	-33.759	47.7	-0.607	76.8
7	-3.036	-22.6	-81.726	-74.0	-25.384	27.4	-0.680	59.8
7.5	-3.497	-48.9	-77.378	144.9	-17.473	-1.5	-0.915	41.2
8	-3.981	-79.1	-69.546	82.2	-9.464	-36.7	-1.267	19.1
8.5	-4.408	-113.8	-63.953	41.2	-1.101	-79.3	-2.036	-8.2
9	-4.736	-154.2	-62.439	11.5	8.005	-135.2	-3.605	-45.1
9.5	-6.218	159.5	-55.881	-16.0	16.532	141.9	-7.182	-98.5
10	-9.258	136.2	-51.738	-102.1	19.391	42.8	-10.773	-164.4
10.5	-8.884	116.5	-51.136	179.1	19.616	-34.2	-8.952	127.3
11	-9.548	87.8	-50.647	113.2	20.436	-104.0	-7.466	76.5
11.5	-13.349	69.0	-49.180	44.3	21.139	-179.1	-8.824	42.3
12	-14.831	90.7	-49.920	-32.9	20.396	104.1	-10.582	32.5
12.5	-12.142	94.6	-50.821	-109.4	19.357	29.8	-12.276	11.2
13	-8.922	92.9	-50.300	156.0	17.619	-55.5	-19.878	119.9
13.5	-6.129	74.0	-53.006	75.8	11.908	-139.8	-5.915	79.9
14	-4.899	56.3	-57.158	20.5	4.911	157.3	-3.488	48.6
14.5	-3.879	41.0	-66.826	-5.9	-1.291	106.1	-2.585	28.1
15	-2.982	25.9	-65.848	99.9	-6.593	59.8	-2.015	12.0
15.5	-2.290	10.8	-55.767	68.7	-10.888	13.7	-1.558	-2.4
16	-1.775	-4.0	-53.323	22.5	-14.040	-39.4	-1.193	-15.8
16.5	-1.432	-18.5	-55.770	-36.4	-18.046	-114.5	-0.853	-28.9
17	-1.188	-31.9	-68.511	141.5	-26.860	174.1	-0.711	-41.8
17.5	-1.047	-44.6	-57.963	46.4	-35.638	126.4	-0.646	-53.8
18	-0.895	-57.1	-58.985	65.1	-41.659	95.0	-0.549	-65.3
18.5	-0.804	-69.4	-50.836	52.5	-43.451	64.9	-0.520	-77.2
19	-0.727	-80.9	-49.615	3.2	-45.376	23.4	-0.467	-89.1

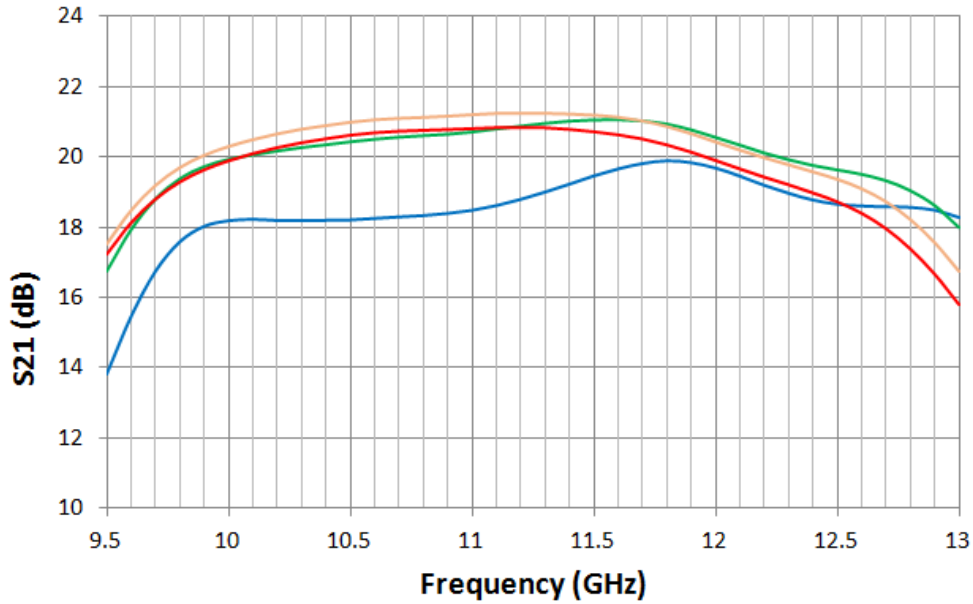
## Typical Board Measurements

$T_{case} = -30^{\circ}\text{C} / 25^{\circ}\text{C} / 75^{\circ}\text{C} / 95^{\circ}\text{C}$  (Backside QFN),  $V_d = +20\text{V}$ ,  $I_d = 130\text{mA}$ ,  $V_c = +6\text{V}$

### Linear Gain vs. Frequency & Temperature

Losses due to board are de-embedded. Measurements are given in the QFN access plan

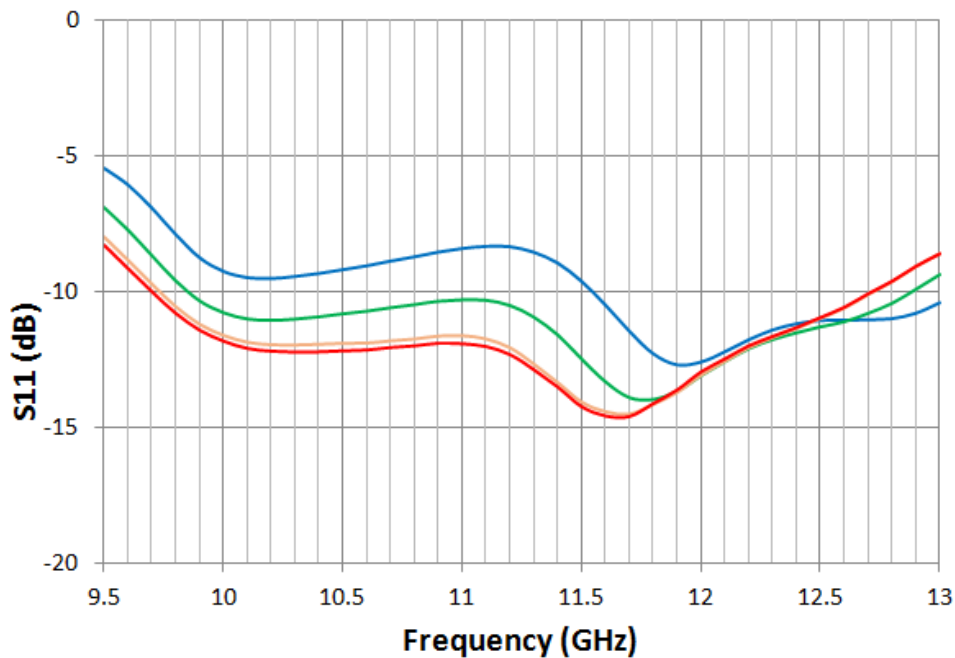
$T_{case}$ : -30°C 25°C 75°C 95°C



### Input Return Loss vs. Frequency & Temperature

Measurements are given in the connectors access plan

$T_{case}$ : -30°C 25°C 75°C 95°C



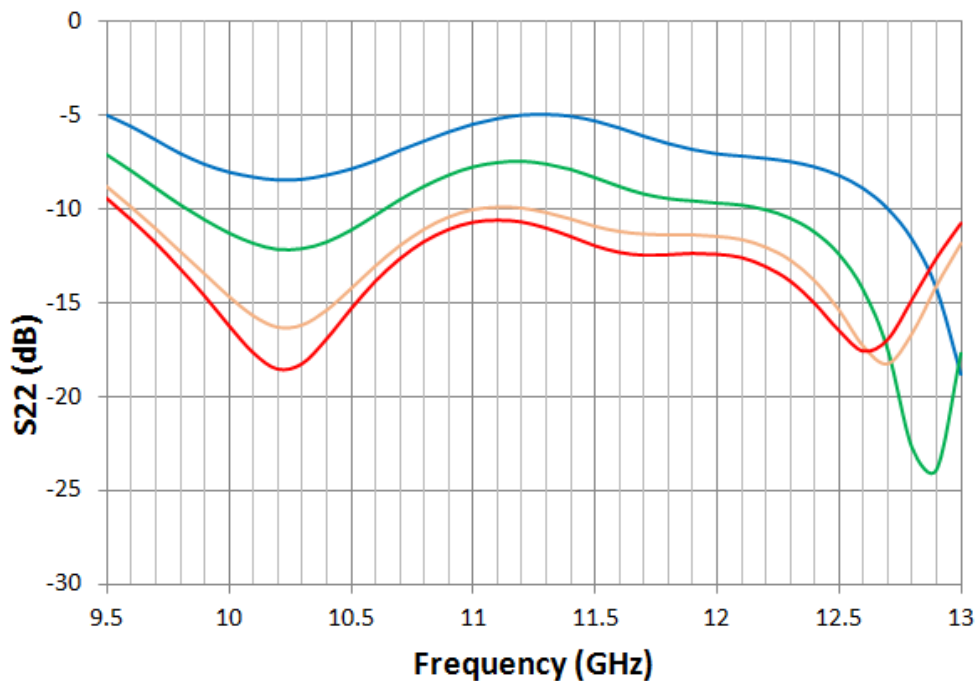
**Typical Board Measurements**

$T_{case} = -30^{\circ}C / 25^{\circ}C / 75^{\circ}C / 95^{\circ}C$  (Backside QFN),  $V_d = +20V$ ,  $I_d = 130mA$ ,  $V_c = +6V$

**Output Return Loss vs. Frequency & Temperature**

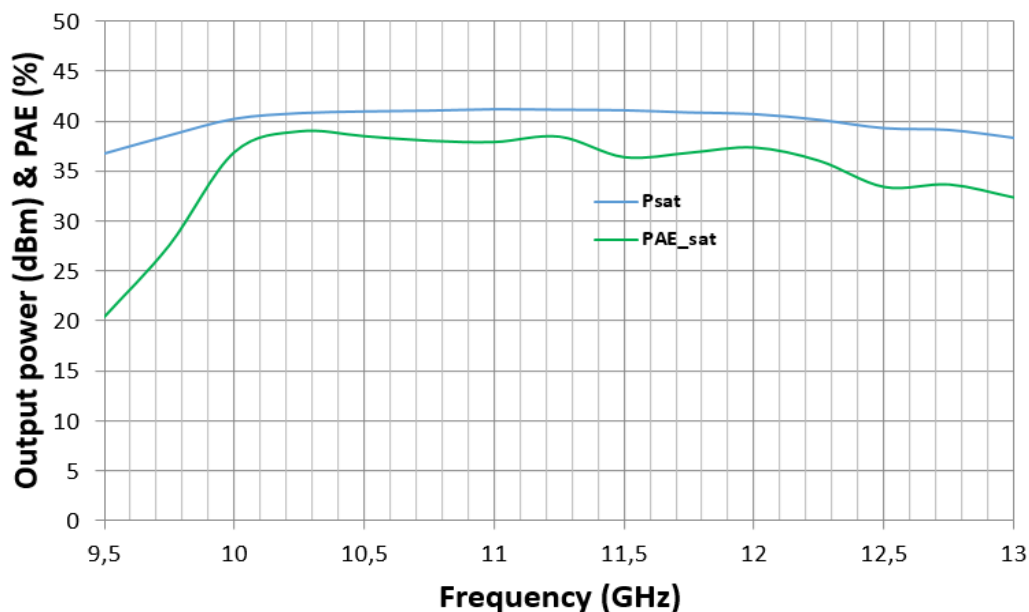
Measurements are given in the connector access plan

**T<sub>case</sub>: -30°C 25°C 75°C 95°C**



$T_{case} = 25^{\circ}C$  (Backside QFN),  $V_d = +20V$ ,  $I_d = 130mA$ ,  $V_c = +6V$

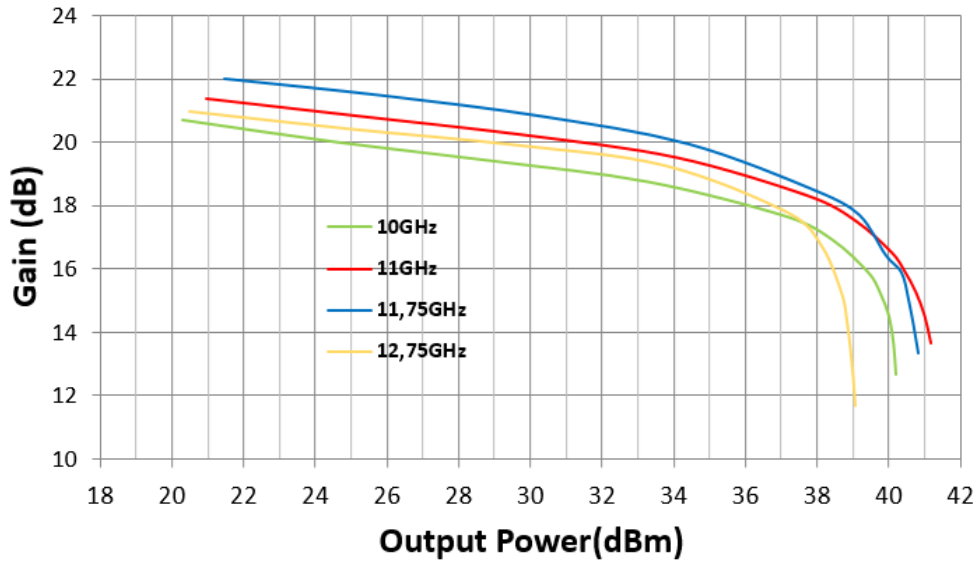
**Output Power & PAE vs. Frequency**



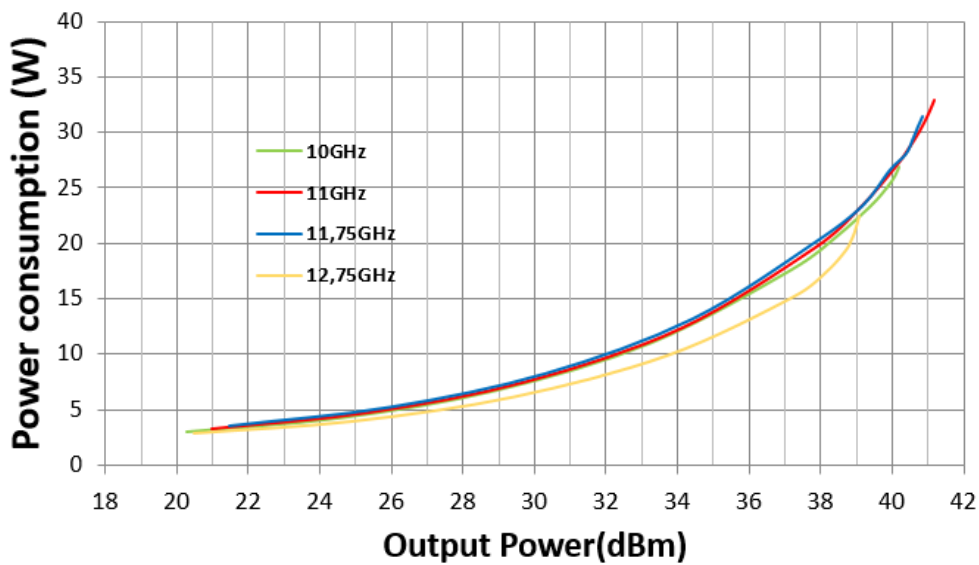
## Typical Board Measurements

$T_{case} = 25^{\circ}C$  (Backside QFN),  $V_d = +20V$ ,  $I_d = 130mA$ ,  $V_c = +6V$

### Gain vs. Output Power



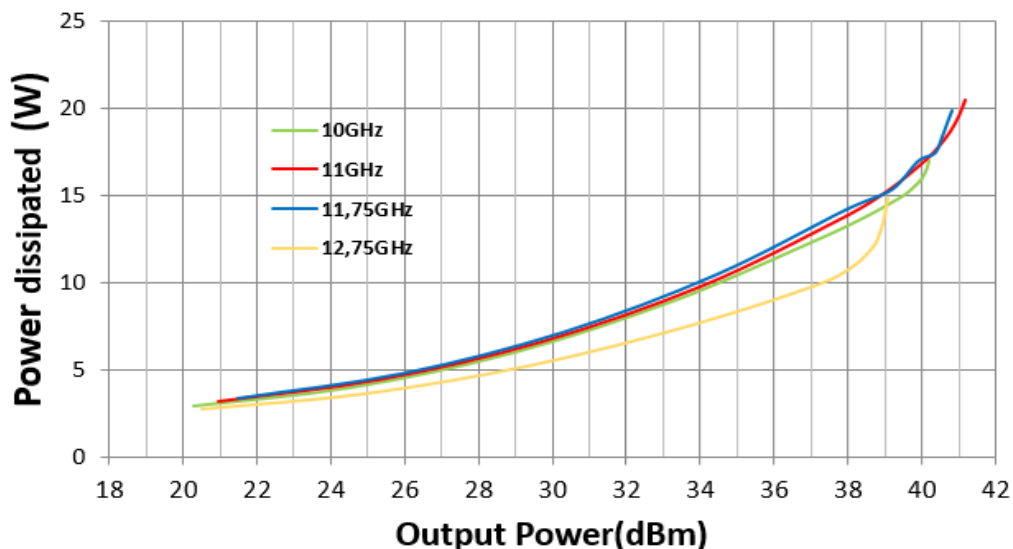
### DC power Consumption vs. Output Power



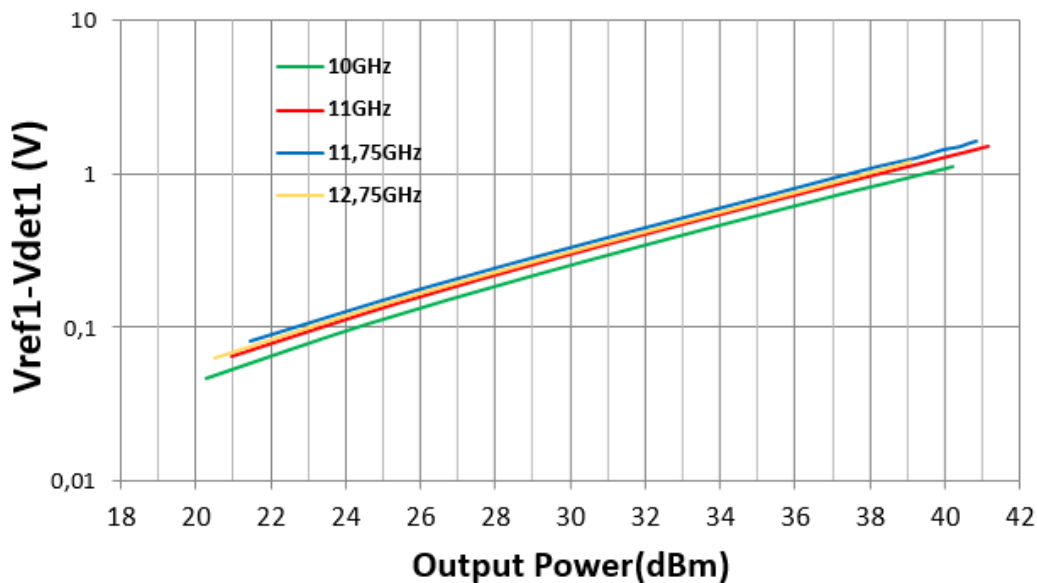
**Typical Board Measurements**

$T_{case} = 25^{\circ}C$  (Backside QFN),  $V_d = +20V$ ,  $I_d = 130mA$ ,  $V_c = +6V$

**Power dissipated vs. Output Power**



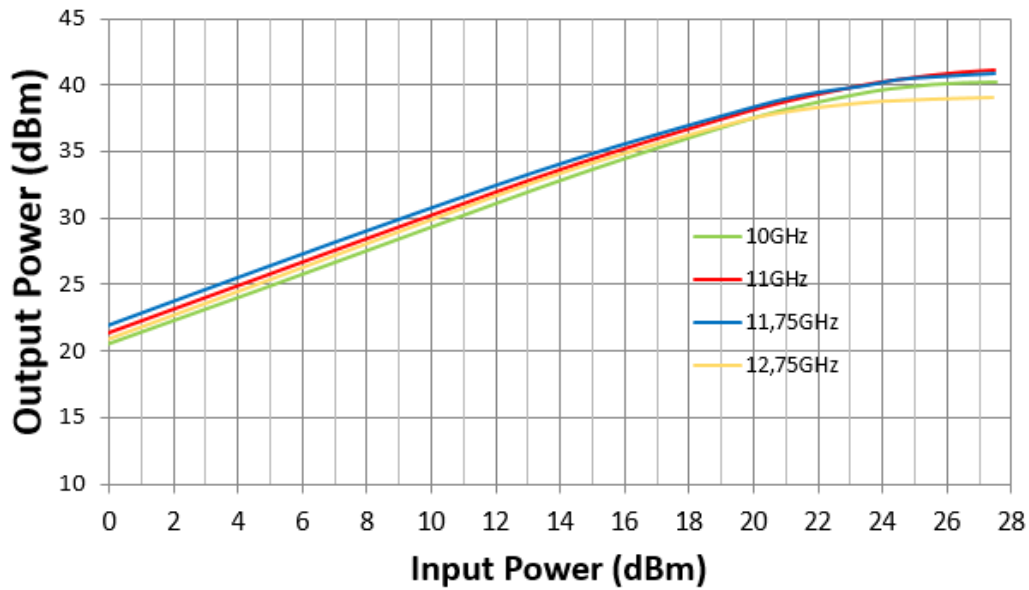
**Vref1-Vdet1 vs. Output Power**



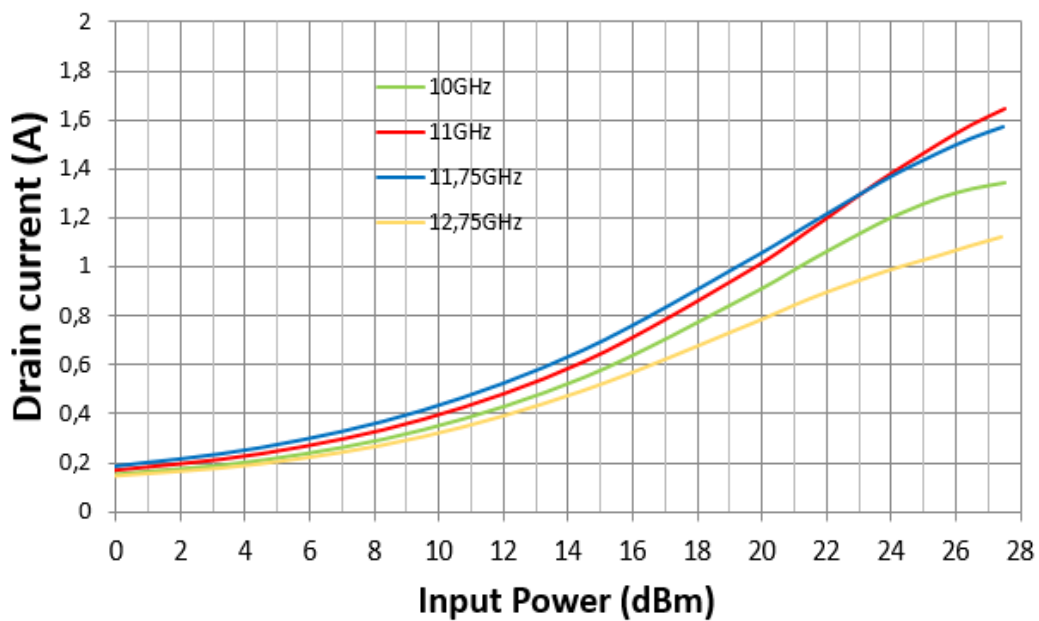
## Typical Board Measurements

$T_{case} = 25^{\circ}C$  (Backside QFN),  $V_d = +20V$ ,  $I_d = 130mA$ ,  $V_c = +6V$

**Output Power vs. Input Power**



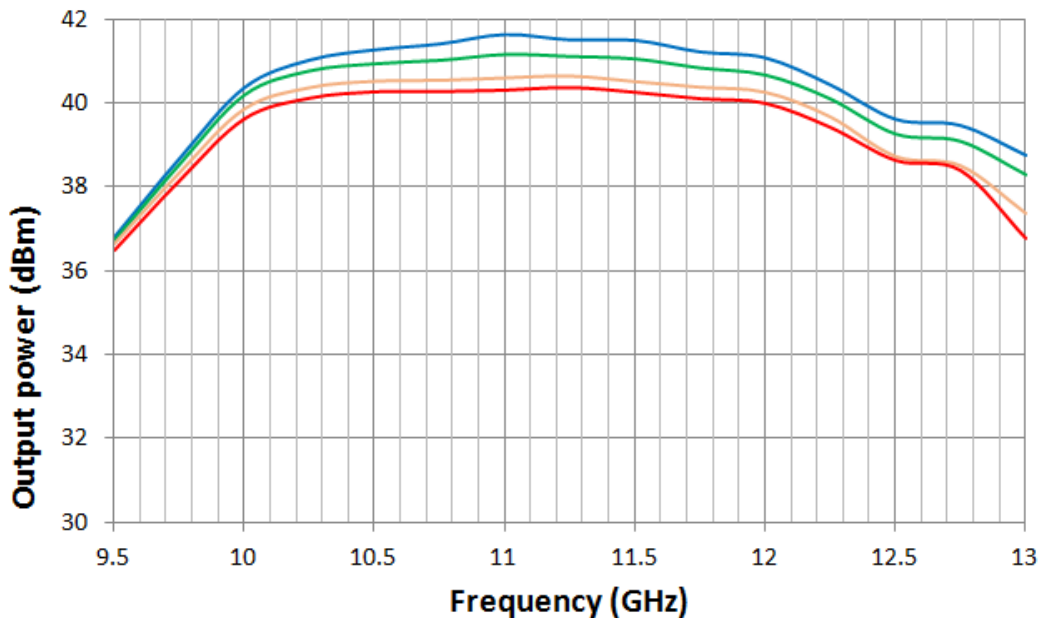
**Total HPA Drain Current vs. Input Power**



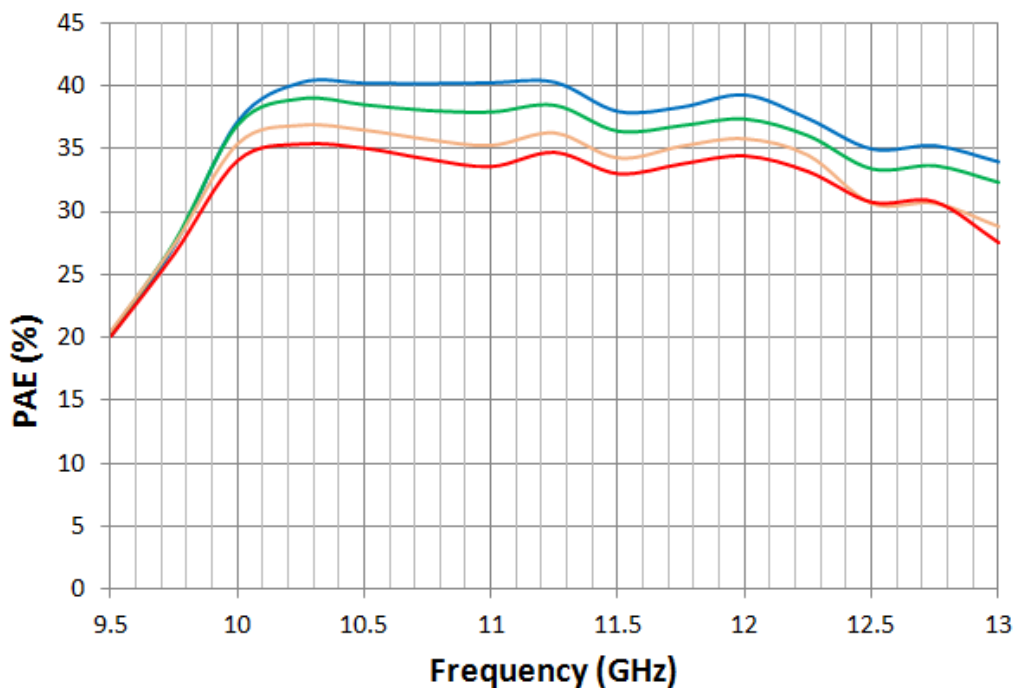
**Typical Board Measurements**

T<sub>case</sub> = -30°C / 25°C / 75°C / 95°C (Backside QFN), V<sub>d</sub> = +20V, I<sub>d</sub> = 130mA, V<sub>c</sub> = +6V

**Output power at Pin=28dBm vs Frequency & temperature**  
T<sub>case</sub>: -30°C 25°C 75°C 95°C



**PAE at Pin=28dBm vs Frequency & temperature**  
T<sub>case</sub>: -30°C 25°C 75°C 95°C



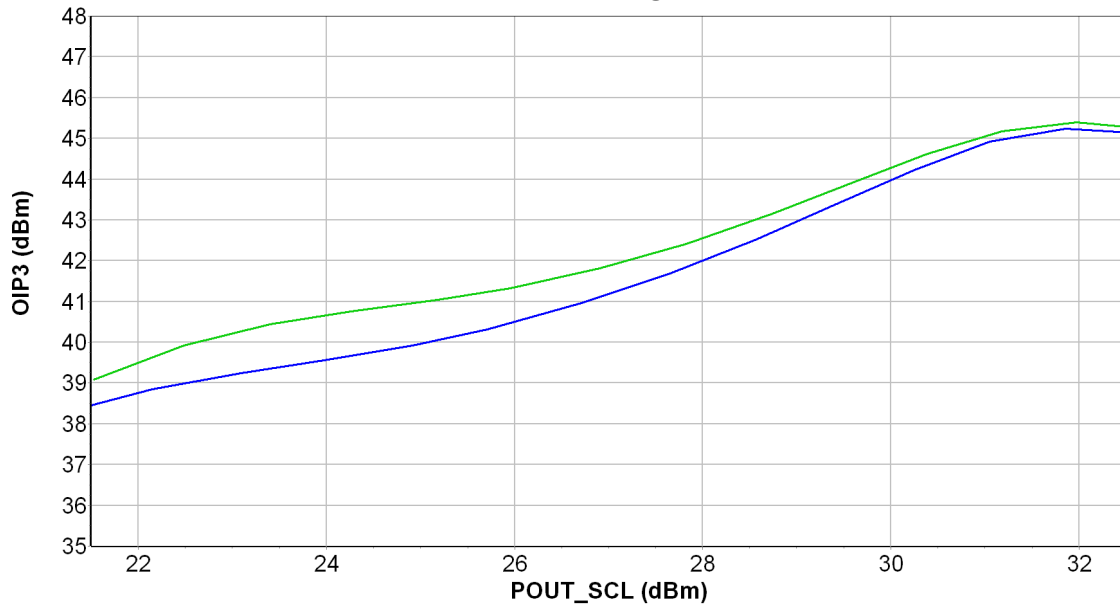
## Typical Board Measurements of linearity performance

$T_{case} = 25^{\circ}C$ ;  $V_d = +20V$ ,  $I_d = 130mA$

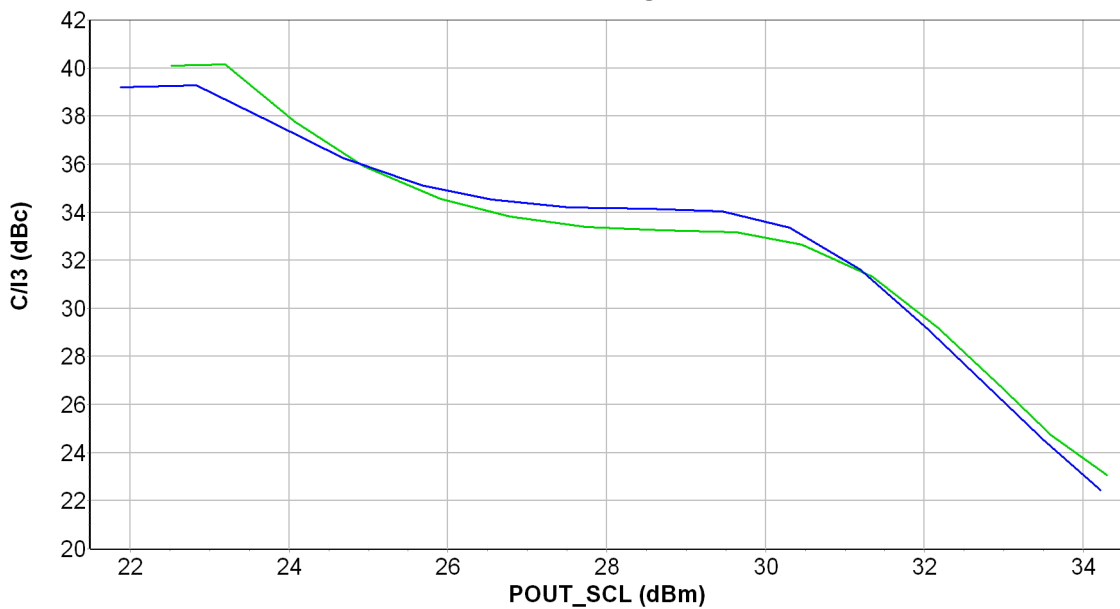
Measurements are given in connector access plans

Delta F = 10MHz (green) and 50MHz (blue)

**OIP3 vs. Output power Single carrier level**



**C/I3 vs. Output power Single carrier level**

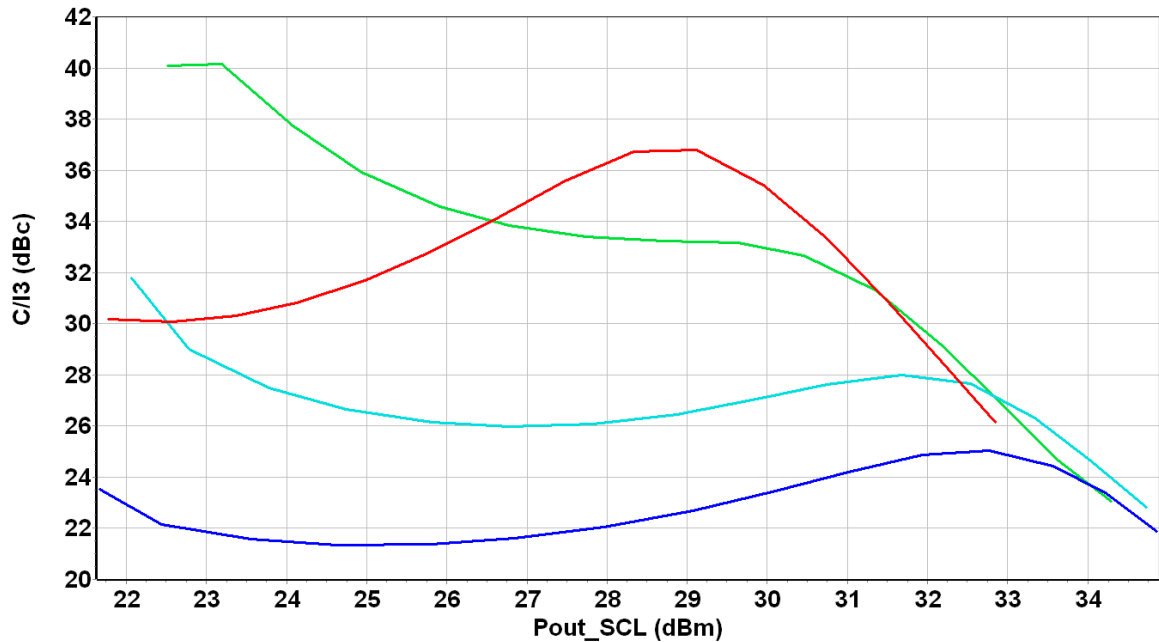


**Typical Board Measurements of linearity performance**

T<sub>case</sub> = -30°C / 0°C / 25°C / 95°C (Backside QFN), V<sub>d</sub> = +20V, I<sub>d</sub> = 130mA, V<sub>c</sub> = +6V (connector access plans)

**C/I3 vs. Output power Single carrier level and temperature**

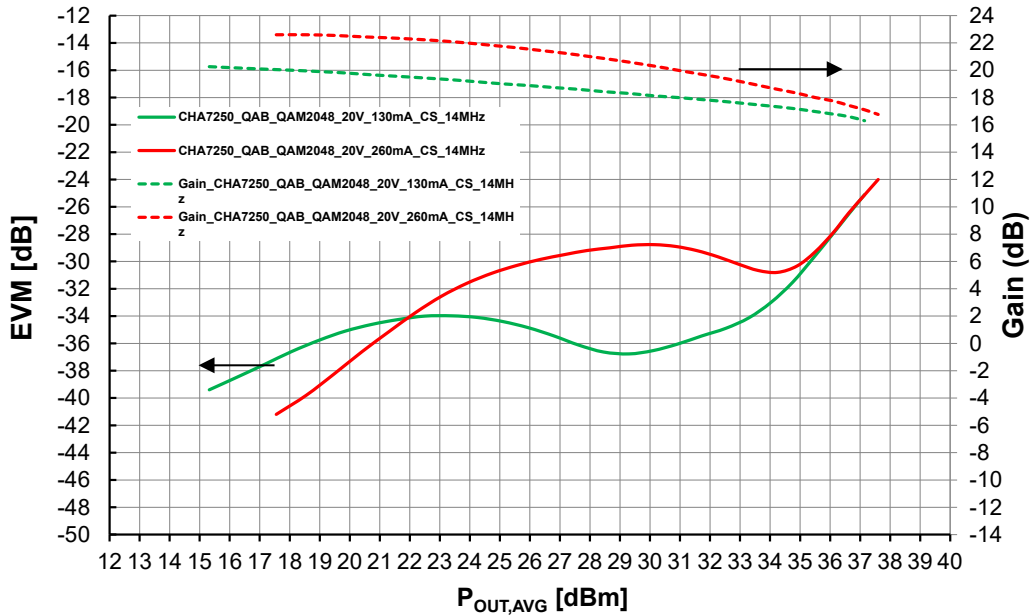
T<sub>case</sub>: -30°C 0°C 25°C 95°C      DeltaF = 10MHz, RF Frequency = 10.75GHz



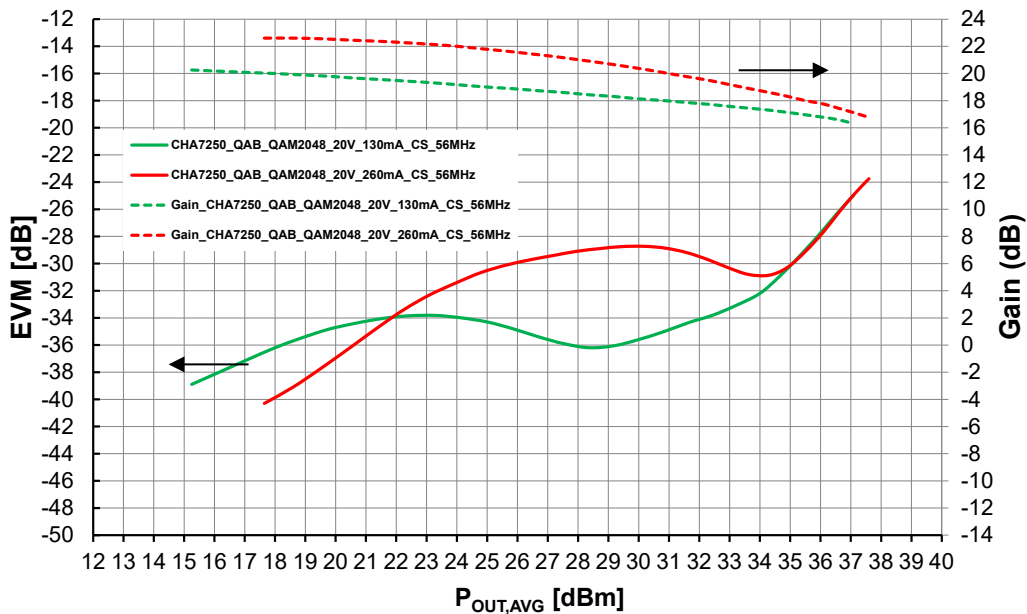
## Typical Board Measurements of linearity performances

Modulation QAM4 & QAM2048/ Channel Spacing=14MHz:  $T_{case} = 25^{\circ}C$ ;  $V_d = +20V$ ,  $I_d = 130$  and  $260mA$  ; Freq = 11.5GHz (connector access plan)

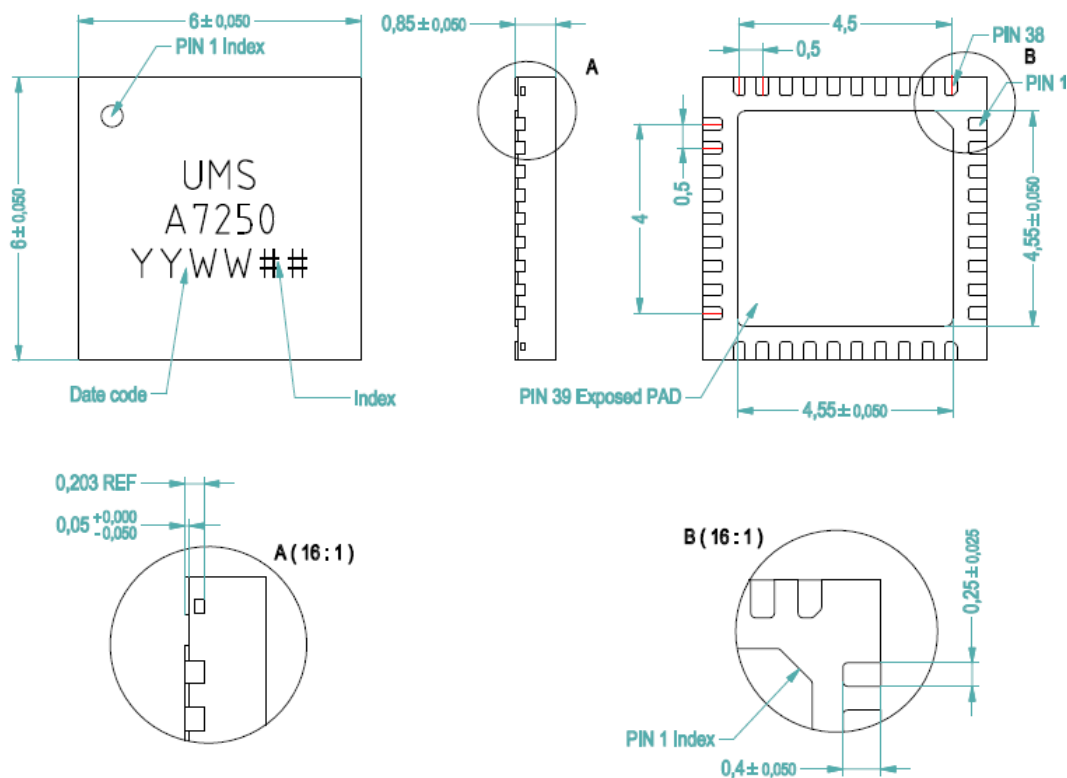
**Error Vector Magnitude vs. & Gain Pout: QAM4/CS=14MHz**



**Error Vector Magnitude vs. & Gain Pout: QAM2048/CS=56MHz**



**Package outline (1)**



Unit : mm  
 Finish : NiPdAuAg  
 Lead free (Green)

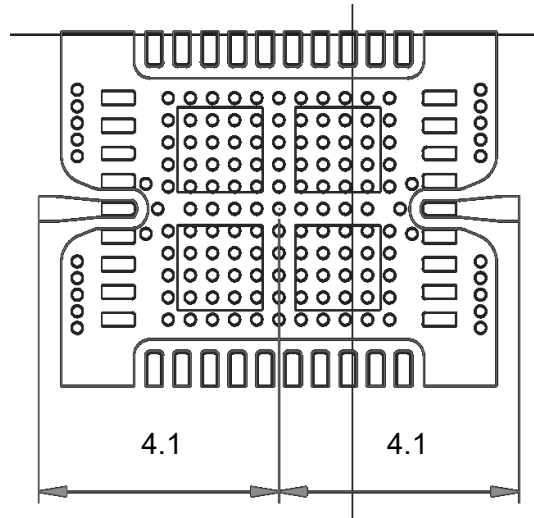


NiPdAuAg, Lead Free (Green)	1- Nc	14- VG2	27- Nc
Units : mm	2- Nc	15- Gnd	28- Nc
From the standard : JEDEC MO-220	3- Nc	16- VD2	29- Nc
(VGGD)	4- Nc	17- Vref	30- Vdet
	5- RF in	18- VC	31- Vref
	6- Nc	19- Nc	32- VD2
	7- Nc	20- Nc	33- Gnd
	8- Nc	21- Vdet	34- VG2
	9- Nc	22- Nc	35- VD1
	10- Nc	23- Nc	36- Gnd
	11- VG1	24- RF out	37- VG1
	12- Gnd	25- Nc	38- Nc
	13- VD1	26- Nc	39- Gnd

(1) Refer to the application note AN0017 (<https://www.ums-rf.com>) for general consideration and recommendations for Molded Plastic QFN/DFN packages.

## Definition of the Sij reference planes

The reference planes used for Sij measurements given above are symmetrical from the symmetrical axis of the package (see drawing beside). The input and output reference planes are located at 4.1mm offset (input wise and output wise respectively) from this axis. Then, the given Sij parameters incorporate the land pattern of the evaluation board recommended in paragraph "Evaluation board" (units in mm).



## ESD sensitivity

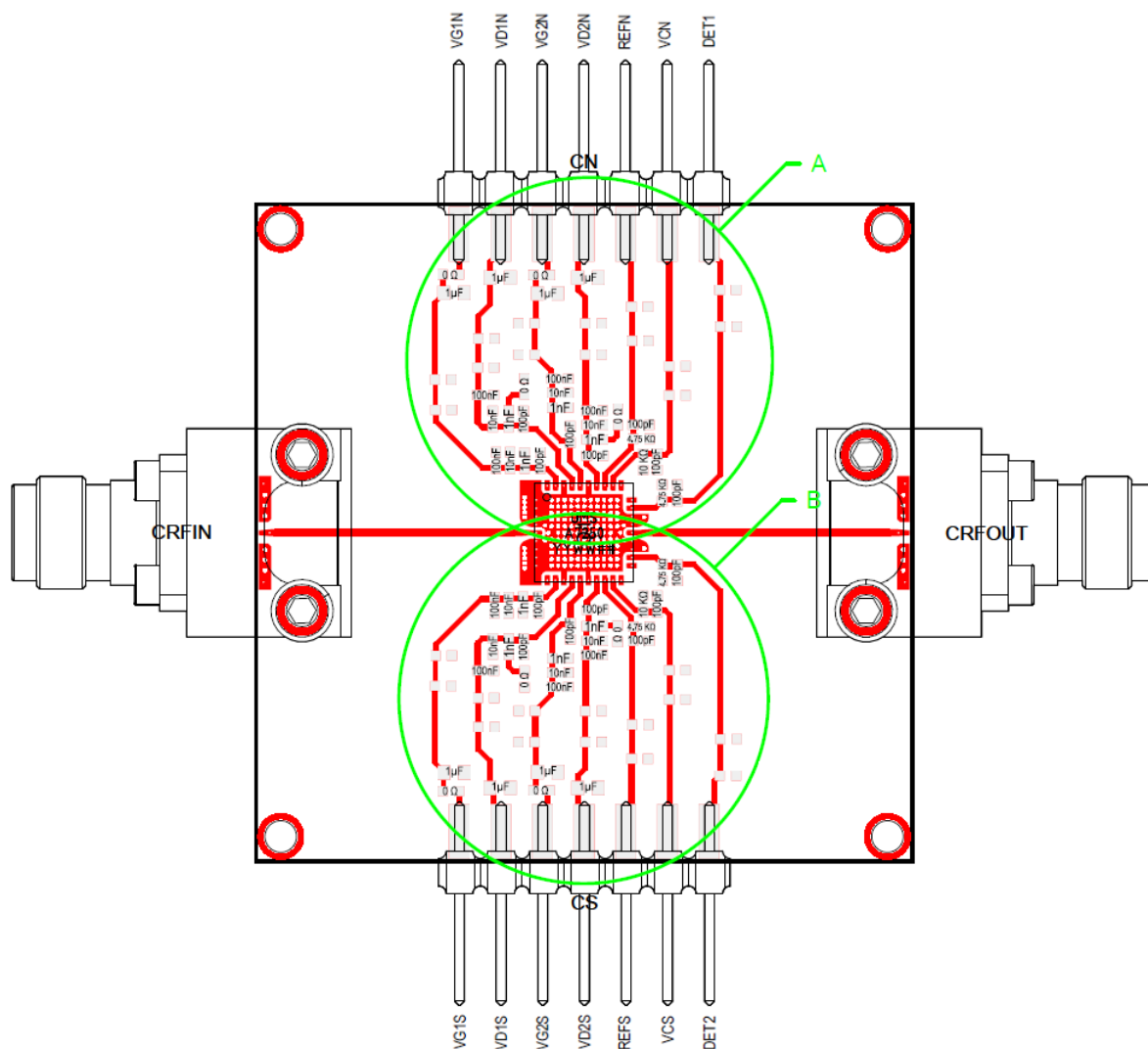
Standard	Value
MIL-STD-1686C	HBM Class 1 (<2000V)

## Package Information

Parameter	Value
Package body material	RoHS-compliant
	Low stress Injection Molded Plastic
Lead finish	Ni-Pd-Au-Ag
MSL Rating	MSL3

### Evaluation Board (EVB)

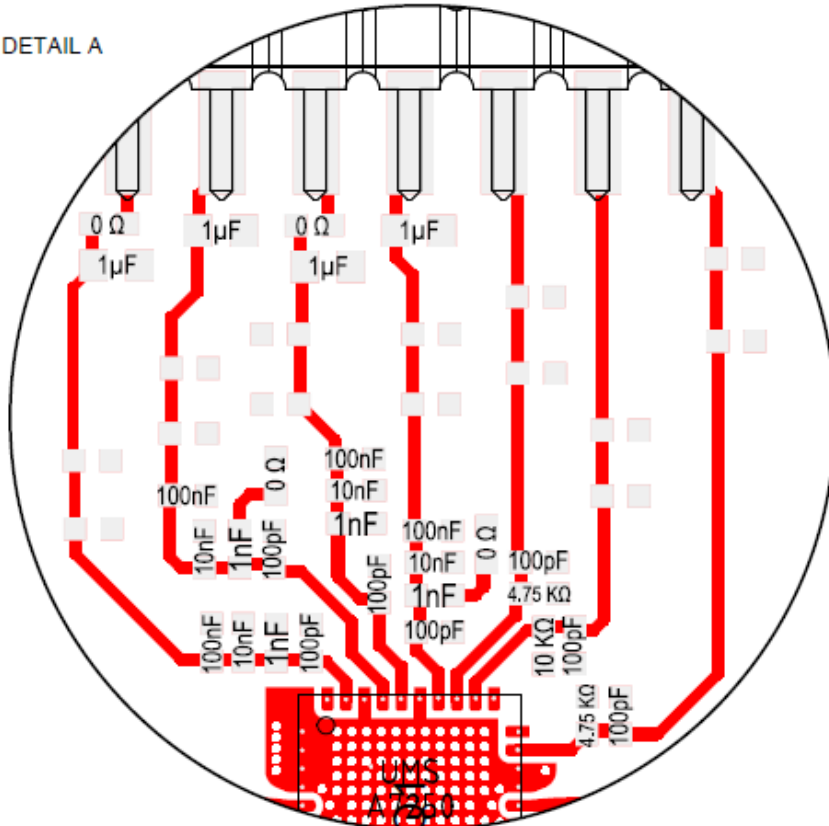
- Compatible with the proposed footprint.
- Based on typically Ro4350B / 10mils or equivalent.
- Using a micro-strip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 100pF  $\pm$ 5%, 1 nF  $\pm$ 10%, 10nF  $\pm$ 10%, 100nF  $\pm$ 10% and 1 $\mu$ F  $\pm$ 10% are recommended for all DC accesses.
- See application note AN0017 for details.



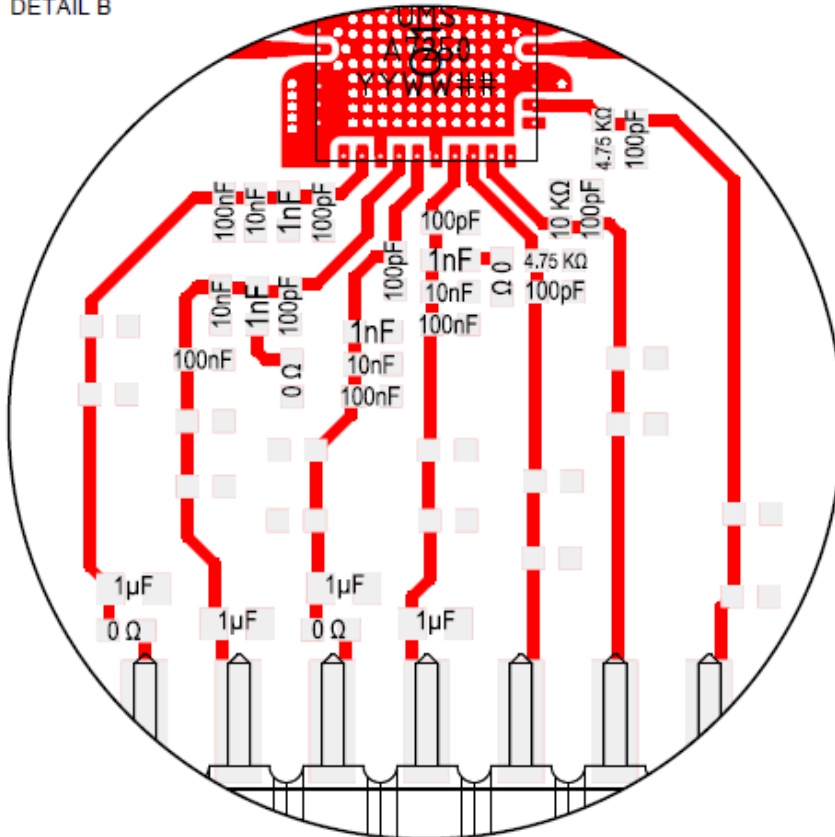
Note: All board measurements are performed using shielded cables, even for DC bias, to ensure safe operation.

## Evaluation Board

DETAIL A

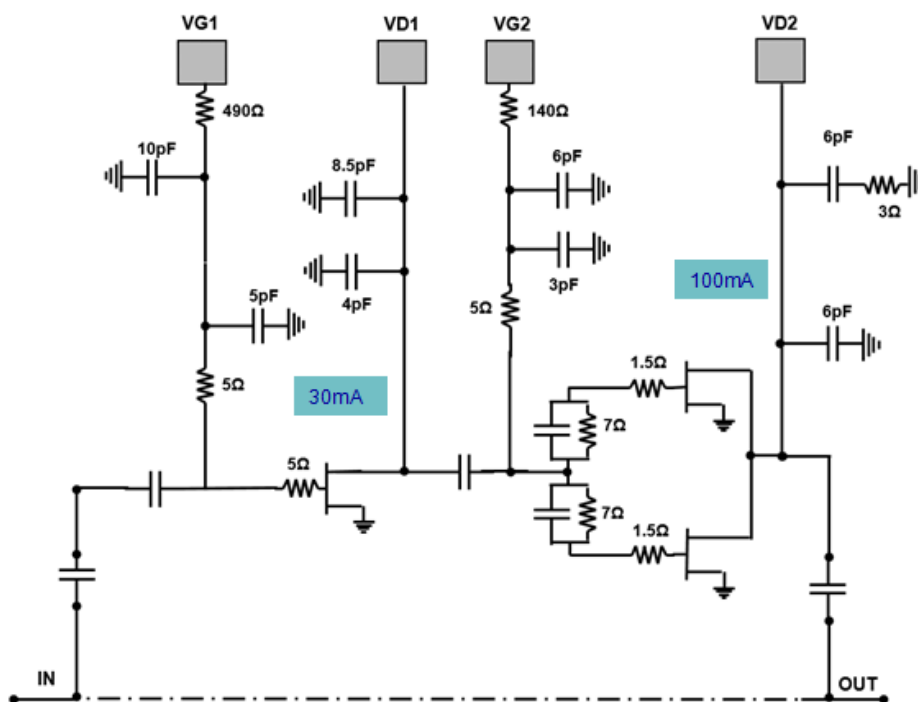


DETAIL B



**DC Schematic**

20V, 130 mA (no RF)



**Notes**

Due to ESD protection circuits on RF input, an external capacitance might be requested to isolate the product from external voltage that could be present on the RF accesses.

The DC connections do not include any decoupling capacitor in package, therefore it is mandatory to provide a good external DC decoupling (100pF, 1nF, 10nF, 100nF, 1μF) on the PC board, as close as possible to the package.

It is recommended to use the detector only on south side (VC applied on south side)

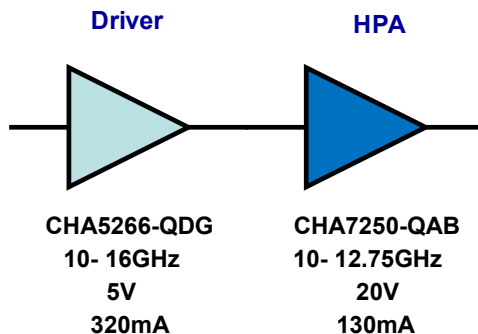
**Recommended UMS Power chain**

The CHA7250-QAB is recommended with the CHA5266-QDG as driver.

Total Gain: 44dB

Gain control: 30dB for the two amplifiers.

For more information about CHA5266-QDG, see our [web site](#).



## Recommended package footprint

Refer to the application note AN0017 available at <https://www.ums-rf.com> for package footprint recommendations.

## SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017 at <https://www.ums-rf.com>.

## Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACH N°1907/2006. More environmental data are available in the application note AN0019 also available at <https://www.ums-rf.com>.

## Recommended ESD management

Refer to the application note AN0020 available at <https://www.ums-rf.com> for ESD sensitivity and handling recommendations for the UMS package products.

## Description of Evaluation Board

Refer to the application note AN0031 available at <https://www.ums-rf.com> for the description of Evaluation Board for Packaged Die and recommendations for this UMS package product.

## Ordering Information

Evaluation Board:	EDG-CHA7250-QAB	
QFN 6x6 package:	CHA7250-QAB/XY	
	Stick: XY = 20	Tape & reel: XY = 21

Information furnished is believed to be accurate and reliable. However **United Monolithic Semiconductors S.A.S.** assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of **United Monolithic Semiconductors S.A.S.**. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. **United Monolithic Semiconductors S.A.S.** products are not authorised for use as critical components in life support devices or systems without express written approval from **United Monolithic Semiconductors S.A.S.**