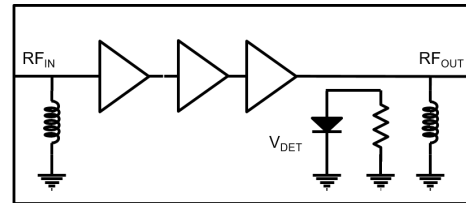
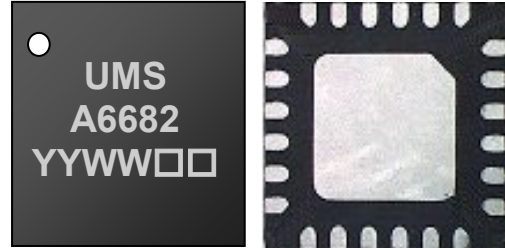


24 - 27.5GHz 4W Linear Power Amplifier

GaN Monolithic Microwave IC in QFN package

Description

The CHA6682-QKB is a three-stage packaged monolithic High Power Amplifier. It is well suited for VSAT, SatCom, 5G communication and RADAR applications. The CHA6682-QKB provides high linearity with low consumption and can be used as a driver stage. It includes a RF power detector. The circuit is manufactured on a robust GaN-on-SiC HEMT technology. The input and output are internally matched to 50Ω and integrate ESD RF protection. It is available in standard surface mount 24 Leads QFN 4x4. It is supplied in RoHS compliant SMD package.

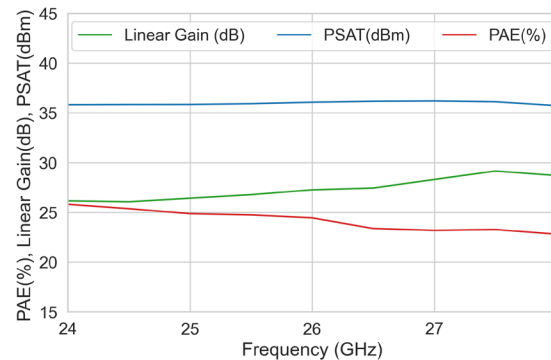


Main Features

- Broadband performances: 24-27.5GHz
- 25dB of Small Signal Gain
- 36dBm Pout for +20dBm of Input Power
- ACPR = -32dBc at 26dBm Average Pout⁽¹⁾
- DC bias: Vd=20V @ Id=140mA
- 24Leads QFN 4x4mm²
- MSL3

⁽¹⁾ 160MHz modulation bandwidth, 256QAM

Output power and PAE at Pin = 20dBm & Linear Gain at Tcase = 25°C



Main Electrical Characteristics

Tcase = +25°C, Vd = +20V (Tcase: QFN backside temperature)

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	24		27.5	GHz
Gain	Linear Gain		25		dB
ACPR	ACPR @ Pout = 26dBm with 256QAM modulation (BW=160MHz)		-32		dBc
Pout	Saturated Output Power		36		dBm
PAE	Associated Power Added Efficiency		26		%

Specifications

T_{case} = +25°C, V_d = +20V

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	24		27.5	GHz
Gain	Linear Gain		25		dB
Psat	Saturated Output Power		36		dBm
PAE	Associated Power Added Efficiency		26		%
S11	Input Return Loss		-8		dB
S22	Output Return Loss		-11		dB
Vdetect	Voltage detection V _{REF} - V _{DET} up to Psat	5		1500	mV
Idq	Total quiescent drain current		140		mA
Id	Total Drain current at saturation		1000		mA

These values are representative of on-board measurements as defined on the drawing in paragraph "Evaluation board".

Absolute Maximum Ratings ⁽¹⁾

T_{case} = +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	27	V
Idq	Quiescent Drain bias current	400	mA
Vg	Gate bias voltage	-7 to -1	V
Pin	Maximum input power	25	dBm

⁽¹⁾ Operation of this device above any one of these parameters may cause permanent damage.

Recommended Operating Range ^{(3), (4)}

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	20	V
Idq	Quiescent Drain bias current	140	mA
Pin	Maximum input power	22	dBm
Tj	Maximum Junction temperature ⁽²⁾	200	°C

⁽²⁾ See Device thermal performances section

⁽³⁾ Electrical performances are defined for specified test conditions

⁽⁴⁾ Electrical performances are not guaranteed over all recommended operating conditions

Temperature Range

Tcase	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +150	°C

Typical Bias Conditions

Tcase=+25°C

Symbol	Pad N°	Parameter	Values	Unit
G1	7	Stage 1 Gate Supply	-5 to -2	V
G2	8	Stage 2 Gate Supply	-5 to -2	V
G3S	10	Stage 3 South Gate Supply	-5 to -2	V
G3N	22	Stage 3 North Gate Supply	-5 to -2	V
D1	24	Stage 1 Drain Supply	20 to 25	V
D2S	9	Stage 2 South Drain Supply	20 to 25	V
D2N	23	Stage 2 North Drain Supply	20 to 25	V
D3S	12	Stage 3 Drain Supply	20 to 25	V
VC	20	Detector Supply	5	V
REF	19	Detector reference voltage		V
DET	21	Detector detected voltage		V

“Power ON” sequence

1. Ground the device
2. Bias HPA gate voltage at Vg close to Vpinch-off (Vg~-5V)
3. Set Vd bias voltage to 0V
4. Apply Vd bias voltage, Vd = 20V
5. Set Vc bias voltage to 5V for detector biasing
6. Increase Vg up to quiescent bias drain current Idq
7. Apply RF input Power

“Power OFF” sequence

1. Turn off RF signal
2. Decrease the Gate voltage Vg to -5V
3. Decrease the Drain voltage Vd to 0V
4. Set Vc bias voltage to 0V
5. Turn off Vg supply

Device thermal performances

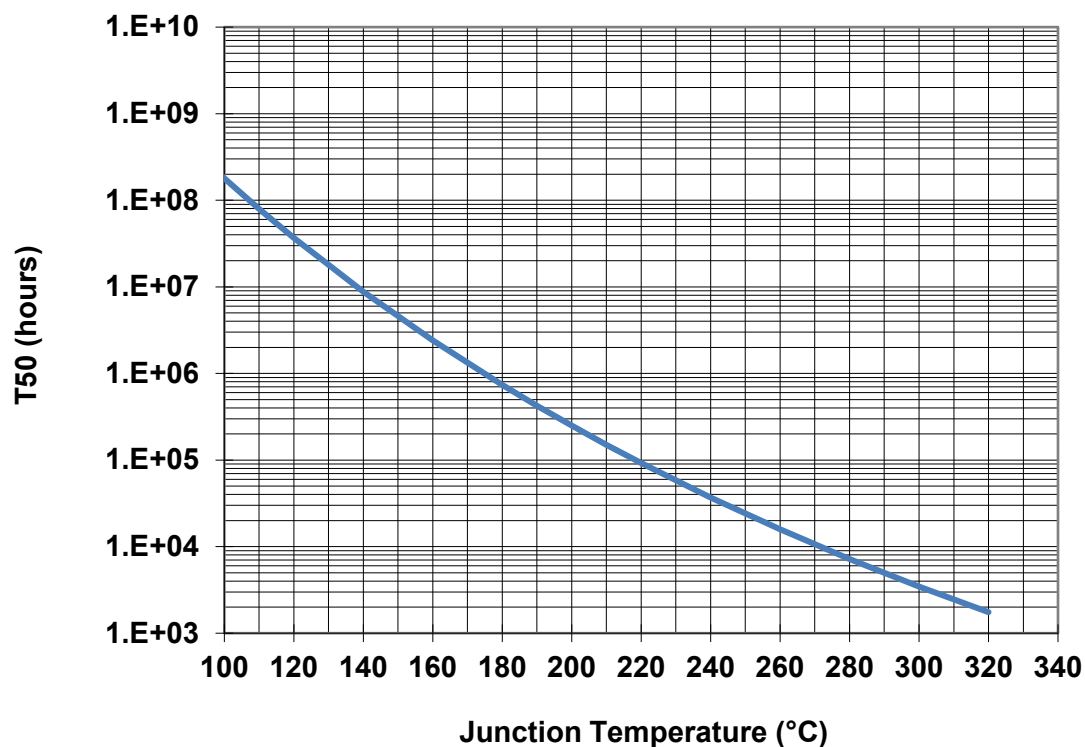
All the figures given in this section are obtained assuming that the QFN device is only cooled down by conduction through the package thermal pad (no convection mode considered).

The temperature is monitored at the package backside interface (Tcase).

For nominal operating, the system maximum temperature must be adjusted in order to guarantee that Tjunction remains below the maximum value specified in the Recommended Operating Ratings table. So the system PCB must be designed to comply with this requirement

Parameter	Biasing conditions	T _{JUNCTION} (°C)	R _{TH} (°C/W)	T50 (hours)
R _{TH} ⁽¹⁾ Thermal Resistance (Junction to QFN Backside)	Vd=20V Pout=35.5dBm Pdiss=12W	200	9.6	2.5E+5
	Vd=20V Pout=32dBm Pdiss=7.6W	143	7.7	7E+6
	Vd=20V Pout=26dBm Pdiss=4.7W	115	6.3	5E+7

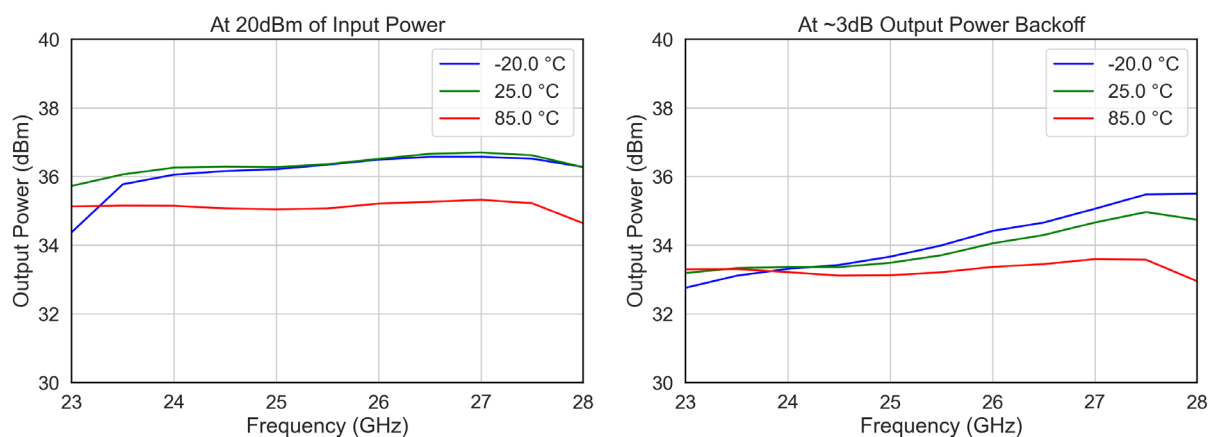
⁽¹⁾ Assuming 85°C Tcase



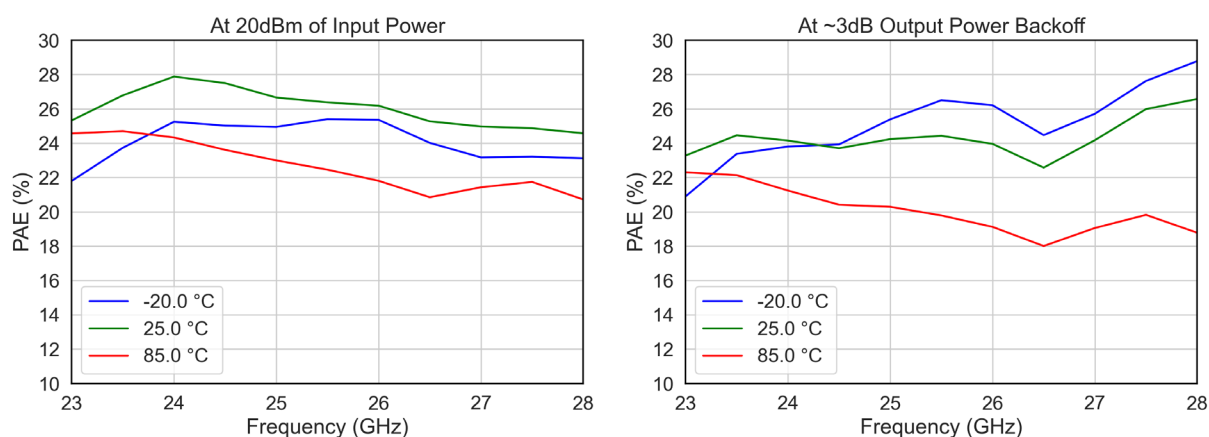
Typical Board Measurements : Large Signal

Test conditions : CW mode , $V_d = +20V$, $I_{dq} = 140mA$, $T_{case} = -20 / +25 / +85^{\circ}C$

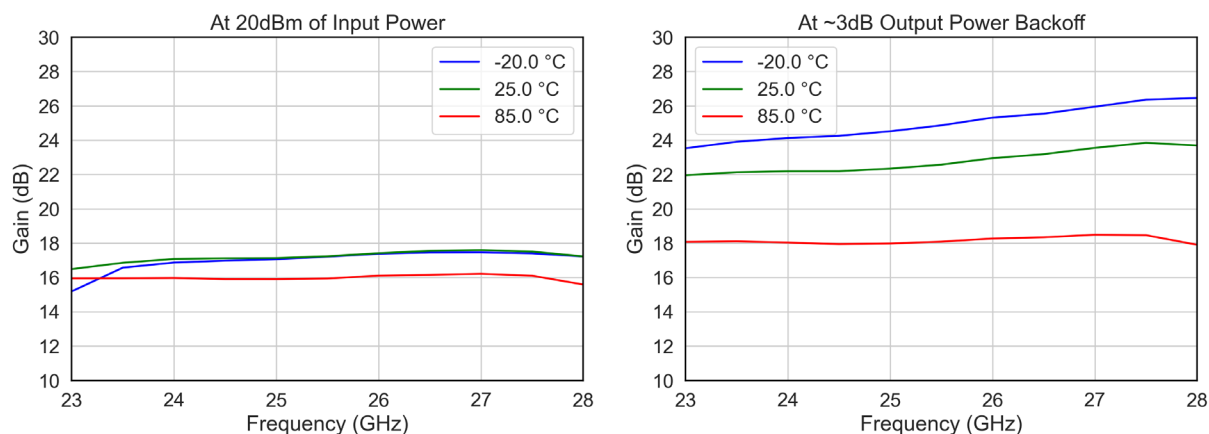
Output Power [dBm] vs. Frequency [GHz]



Power Added Efficiency [%] vs. Frequency [GHz]

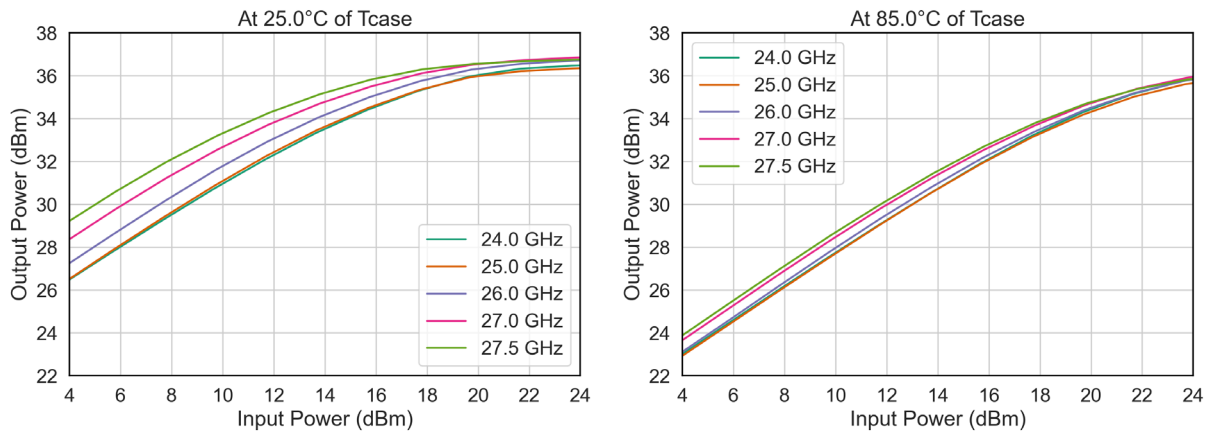
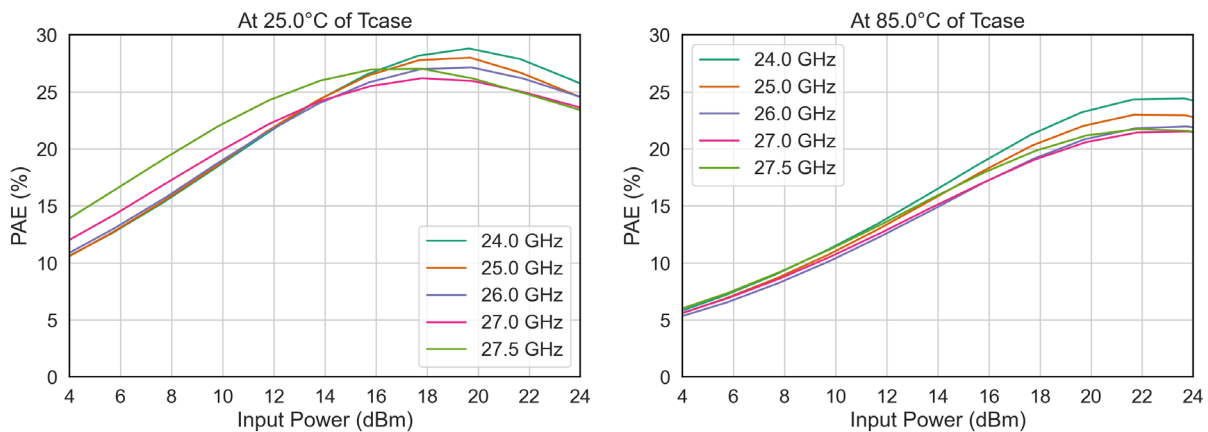
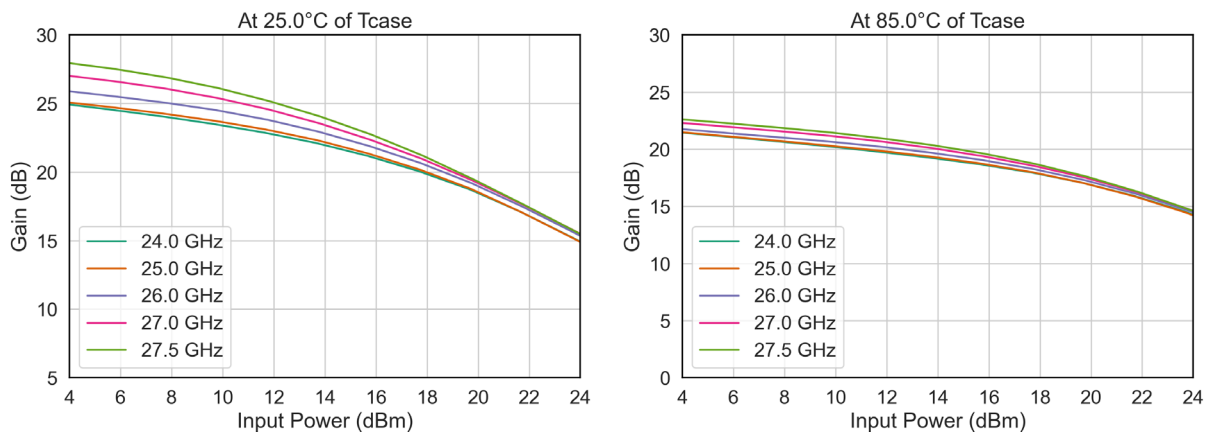


Gain [dB] vs. Frequency [GHz]



Typical Board Measurements : Large Signal

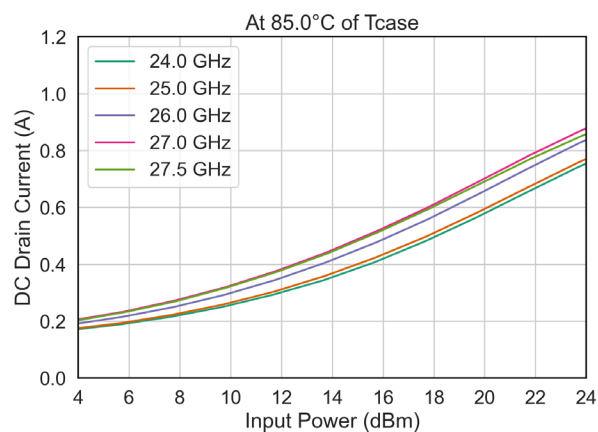
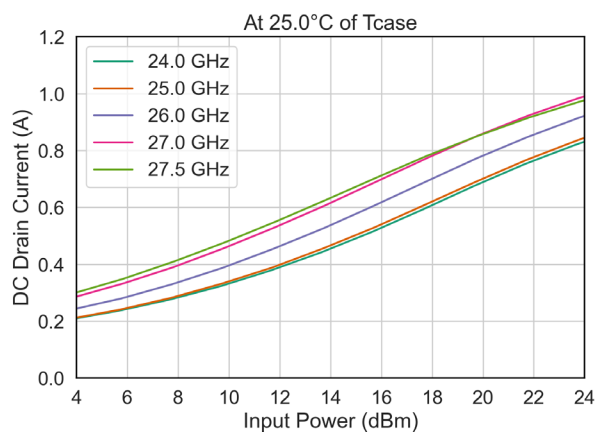
Test conditions : CW mode, $V_d = +20V$, $I_{dq} = 140mA$, $T_{case} = 25 / 85^\circ C$

Output Power [dBm] vs. Input Power [dBm]**Power Added Efficiency [%] vs. Input Power [dBm]****Available Gain [dB] vs. Input Power [dBm]**

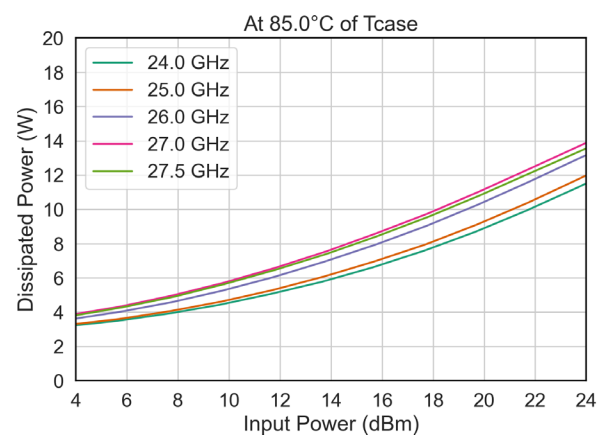
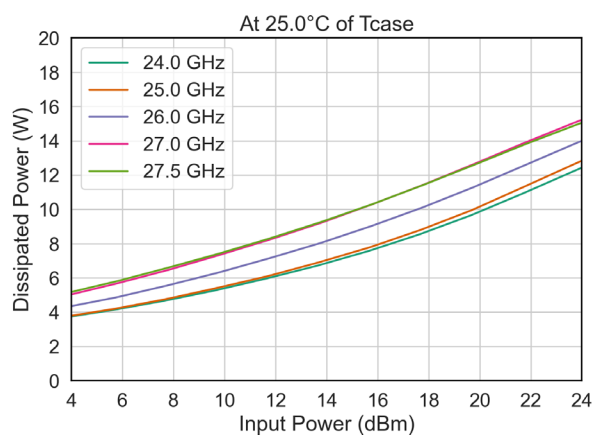
Typical Board Measurements : Large Signal

Test conditions : CW mode, $V_d = +20V$, $I_{dq} = 140mA$, $T_{case} = 25 / 85^{\circ}C$

DC Drain Current [A] vs. Input Power [dBm]



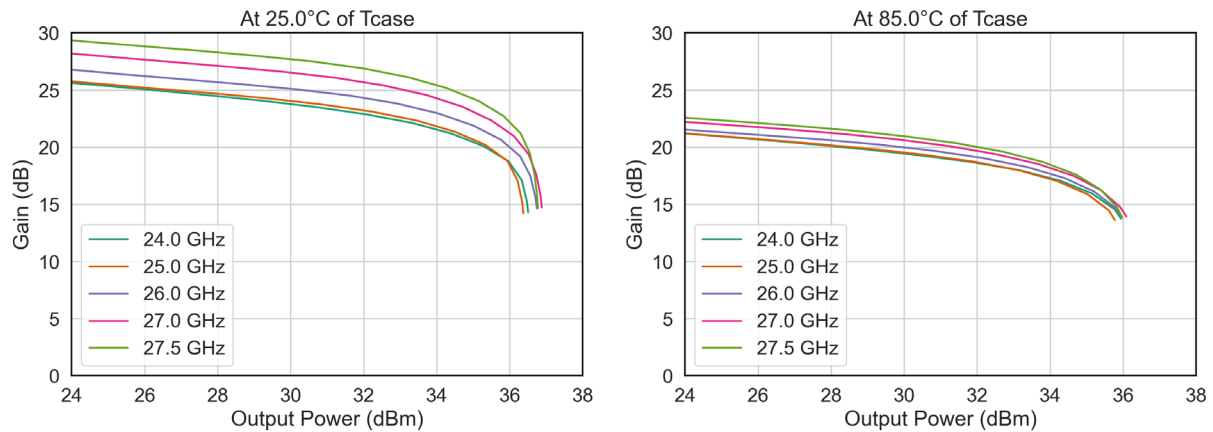
Dissipated Power [W] vs. Input Power [dBm]



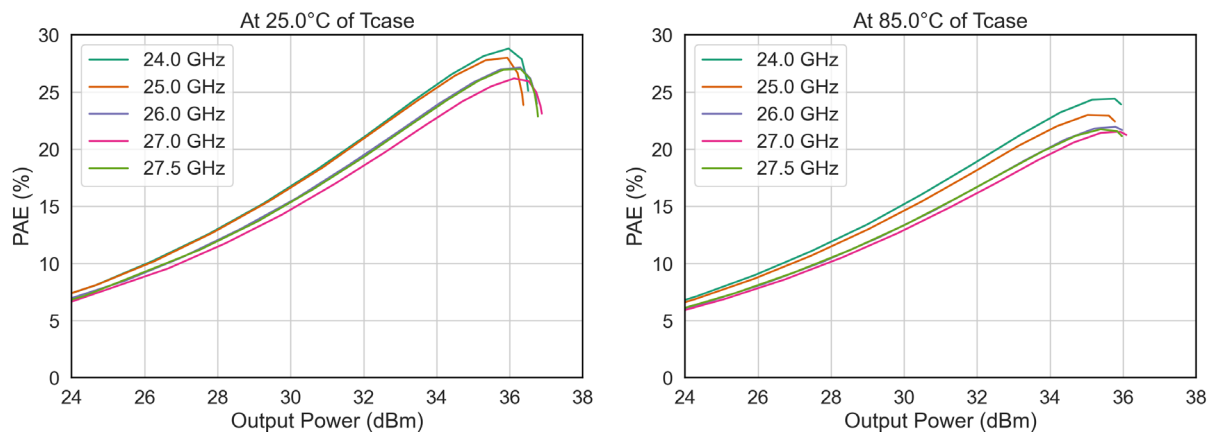
Typical Board Measurements : Large Signal

Test conditions : CW mode, $V_d = +20V$, $I_{dq} = 140mA$, $T_{case} = 25 / 85^\circ C$

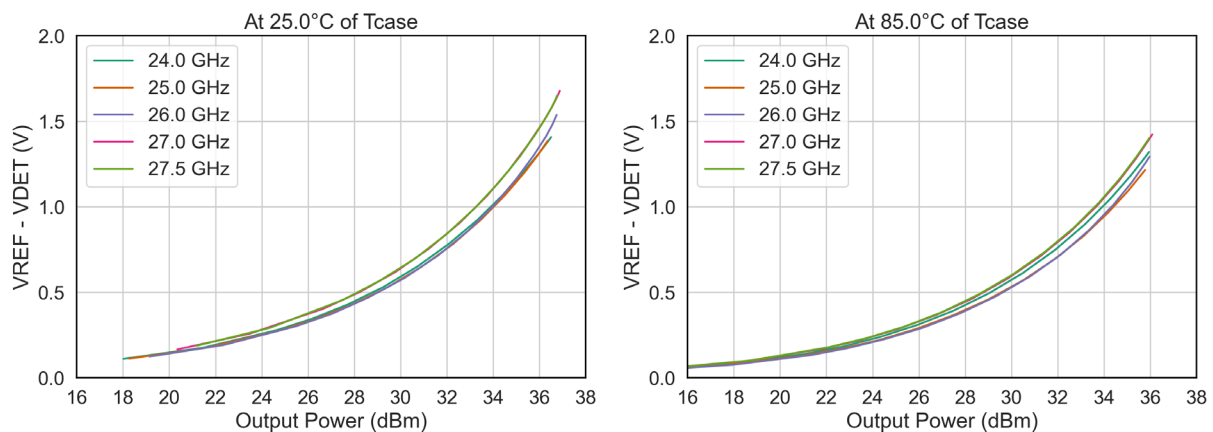
Available Gain [dB] vs. Output Power [dBm]



Power Added Efficiency [%] vs. Output Power [dBm]



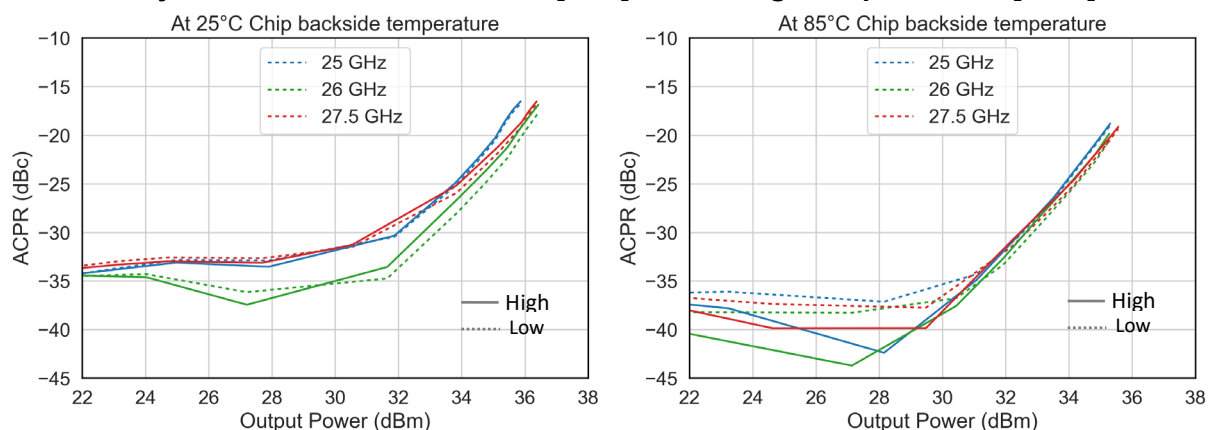
Vref-Vdet [V] vs. Output Power [dBm]



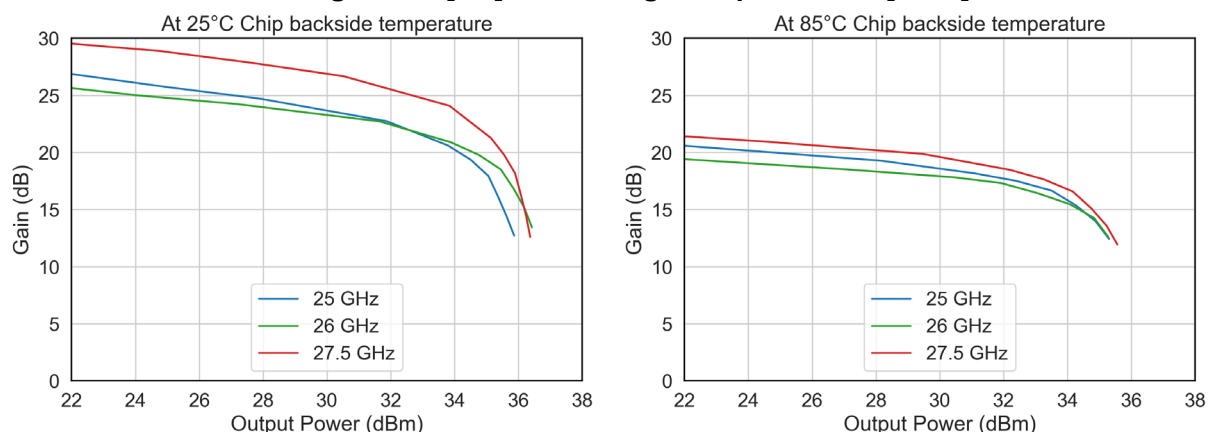
Typical Board Measurements : Modulation Results

Test conditions : $V_d = +20V$, $I_{dq} = 140mA$, 256QAM, 100MHz, Roll-off = 0.2, $f_{CARRIER} = 25/26/27.5GHz$, $T_{case} = 25 / 85^{\circ}C$

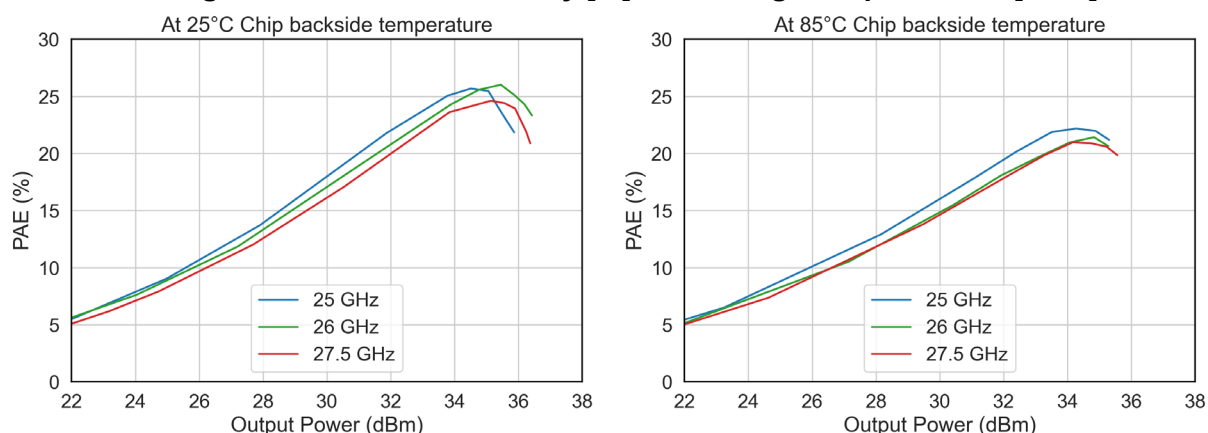
Adjacent Channel Power Ratio [dBc] vs. Average Output Power [dBm]



Average Gain [dB] vs. Average Output Power [dBm]



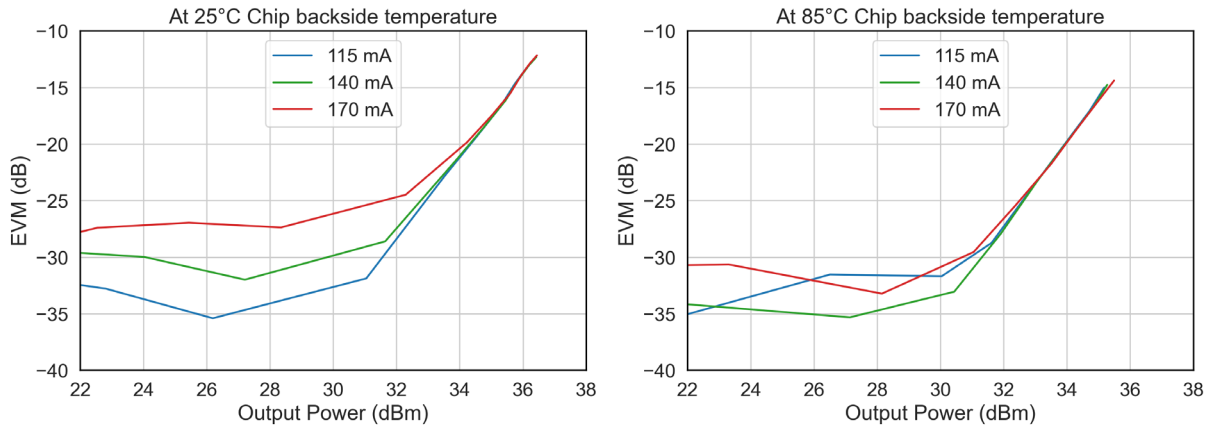
Average Power Added Efficiency [%] vs. Average Output Power [dBm]



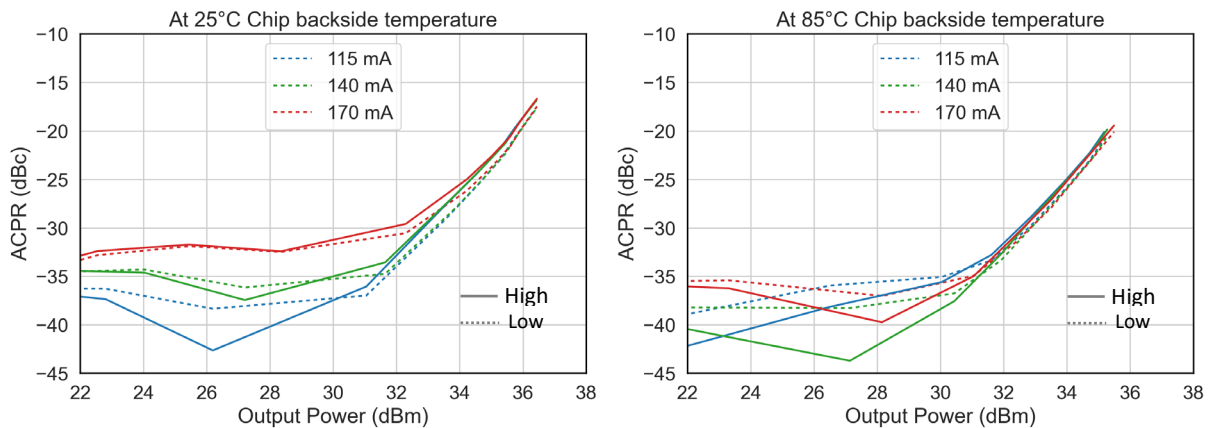
Typical Board Measurements : Modulation Results

Test conditions : $V_d = +20V$, $f_{CARRIER} = 26GHz$, 256QAM, 100MHz, Roll-off = 0.2, $I_{dq} = 115/140/170mA$, $T_{case} = 25/85^{\circ}C$

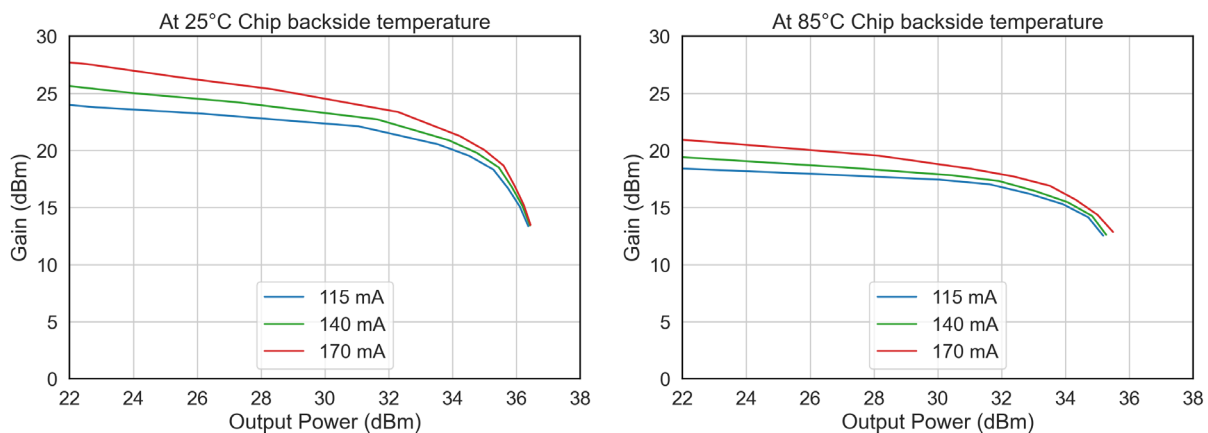
Error Vector Magnitude [dB] vs. Average Output Power [dBm]



Adjacent Channel Power Ratio [dBc] vs. Average Output Power [dBm]



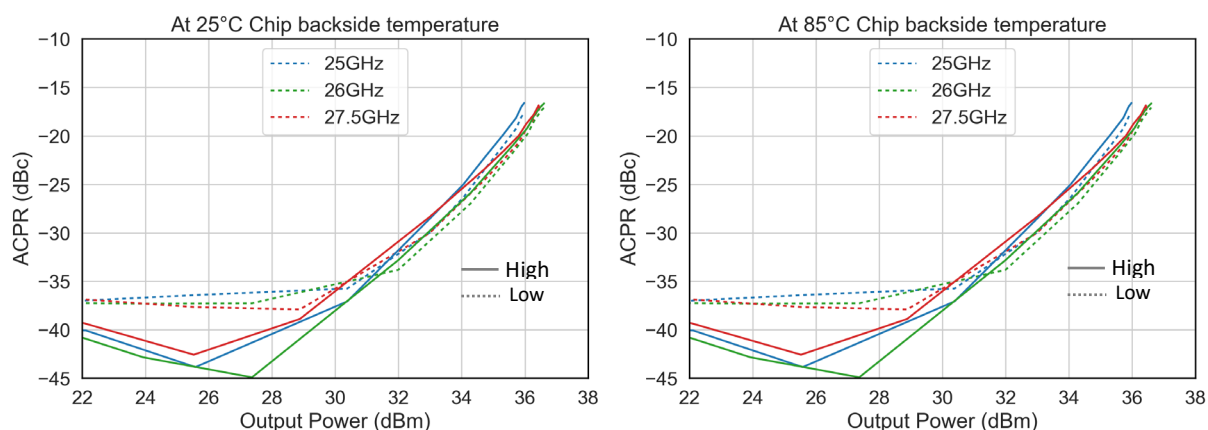
Average Gain [dB] vs. Average Output Power [dBm]



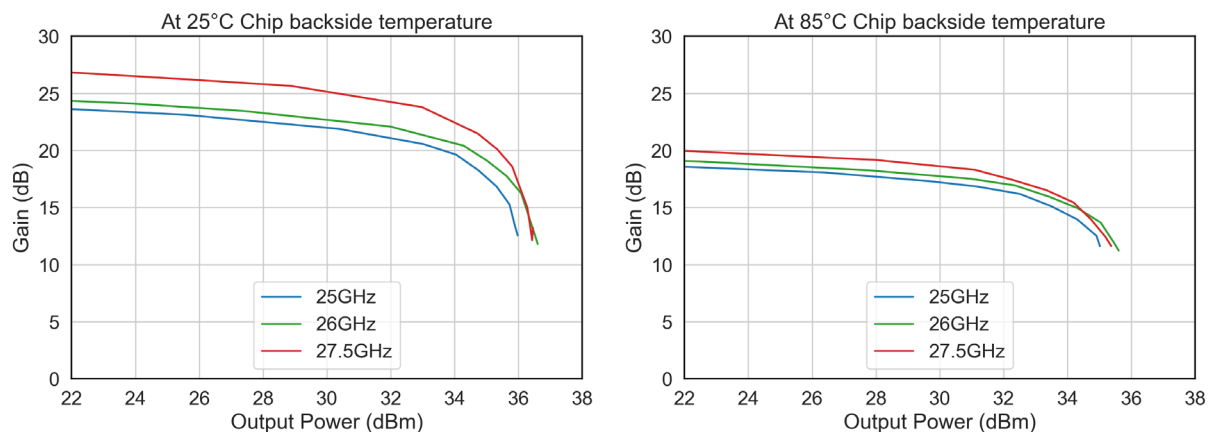
Typical Board Measurements : Modulation Results

Test conditions : $V_d = +20V$, $I_{dq} = 140mA$, 256QAM, 160MHz, Roll-off = 0.2, $f_{CARRIER} = 25/26/27.5GHz$, $T_{case} = 25 / 85^{\circ}C$

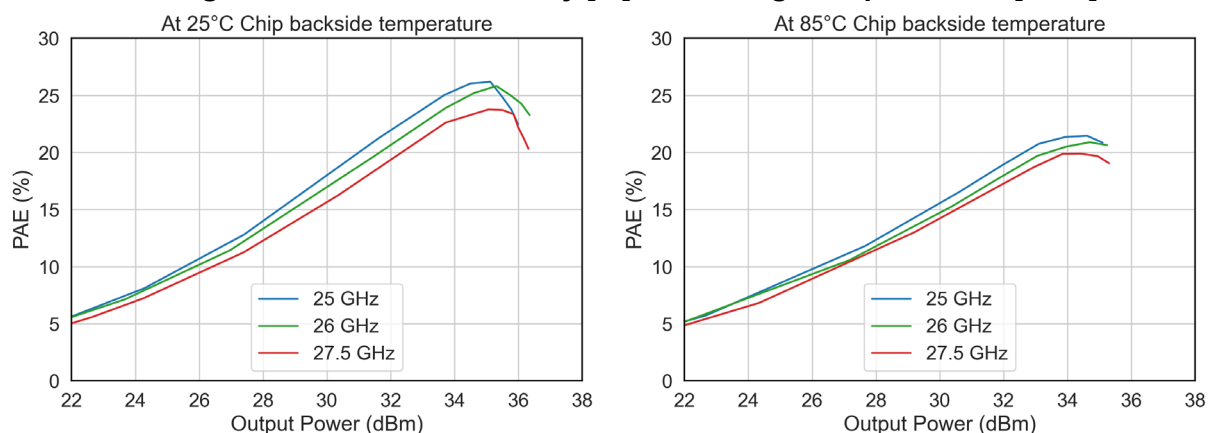
Adjacent Channel Power Ratio [dBc] vs. Average Output Power [dBm]



Average Gain [dB] vs. Average Output Power [dBm]



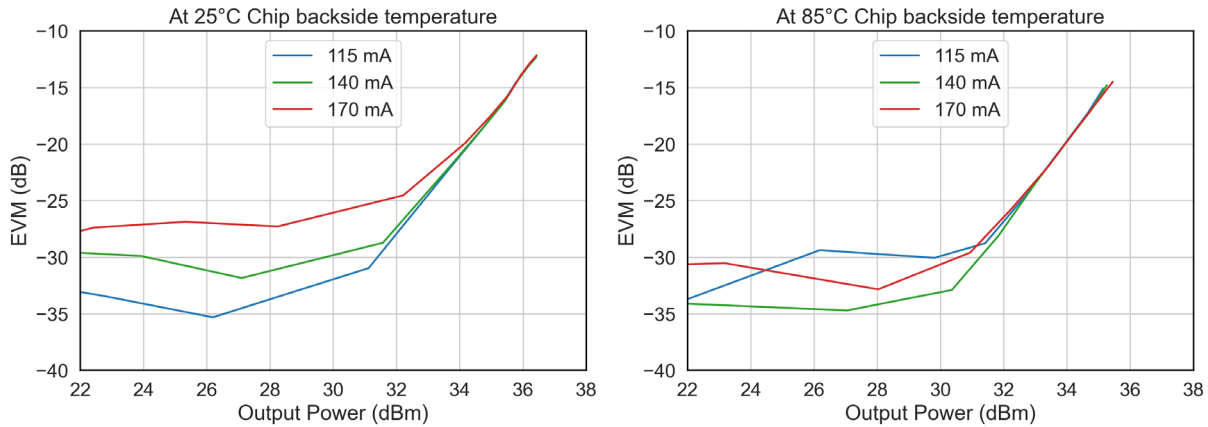
Average Power Added Efficiency [%] vs. Average Output Power [dBm]



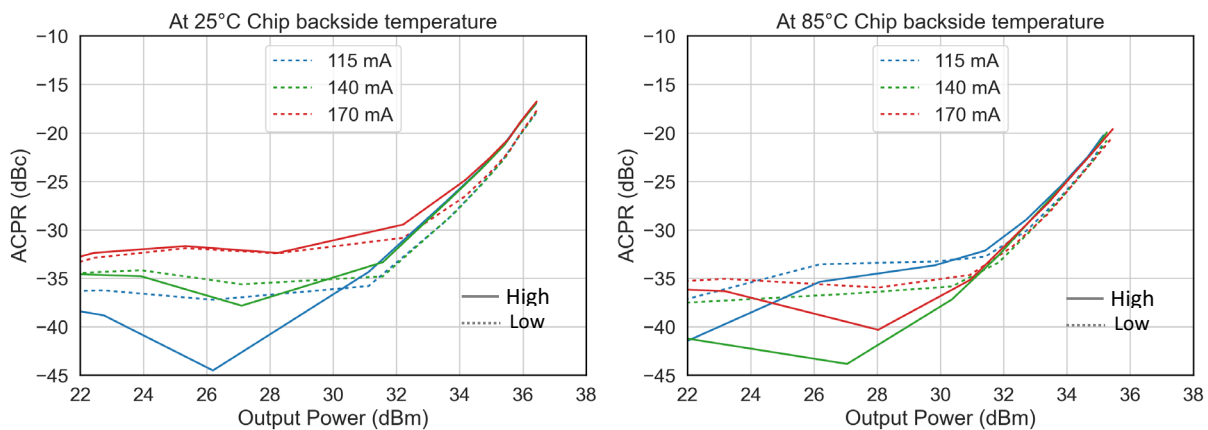
Typical Board Measurements : Modulation Results

Test conditions : $V_d = +20V$, $f_{CARRIER} = 26GHz$, 256QAM, 160MHz, Roll-off = 0.2, $f_{carrier} = 115/ 140/ 170mA$, $T_{case} = 25/ 85^{\circ}C$

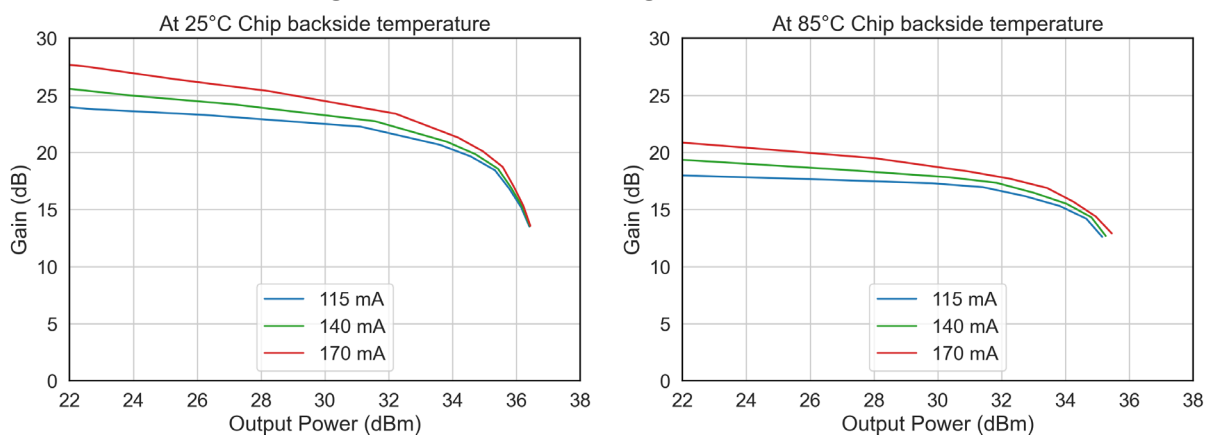
Error Vector Magnitude [dB] vs. Average Output Power [dBm]



Adjacent Channel Power Ratio [dBc] vs. Average Output Power [dBm]



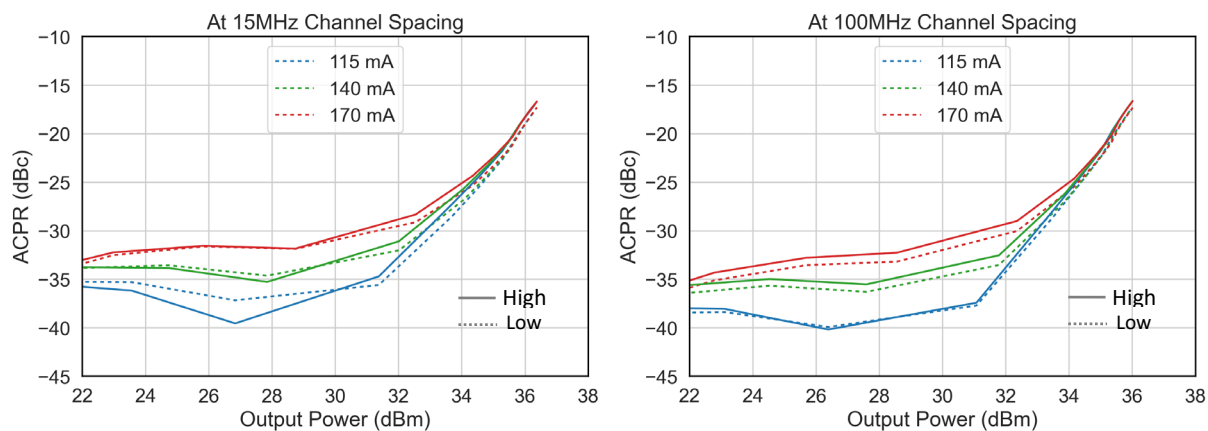
Average Gain [dB] vs. Average Output Power [dBm]



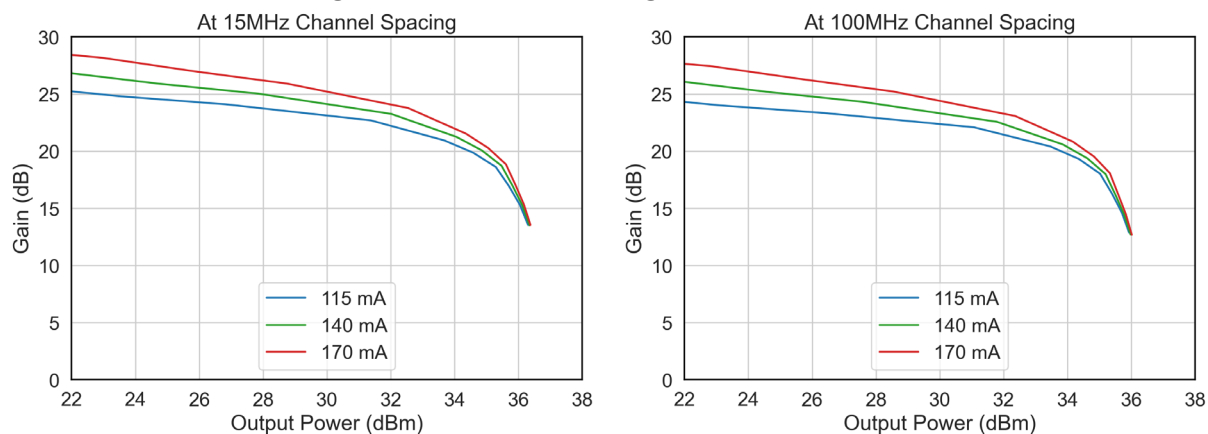
Typical Board Measurements : Modulation Results

Test conditions : $V_d = +20V$, $f_{CARRIER} = 26GHz$, 16QAM, Roll-off = 0.2, $T_{case} = 25^{\circ}C$

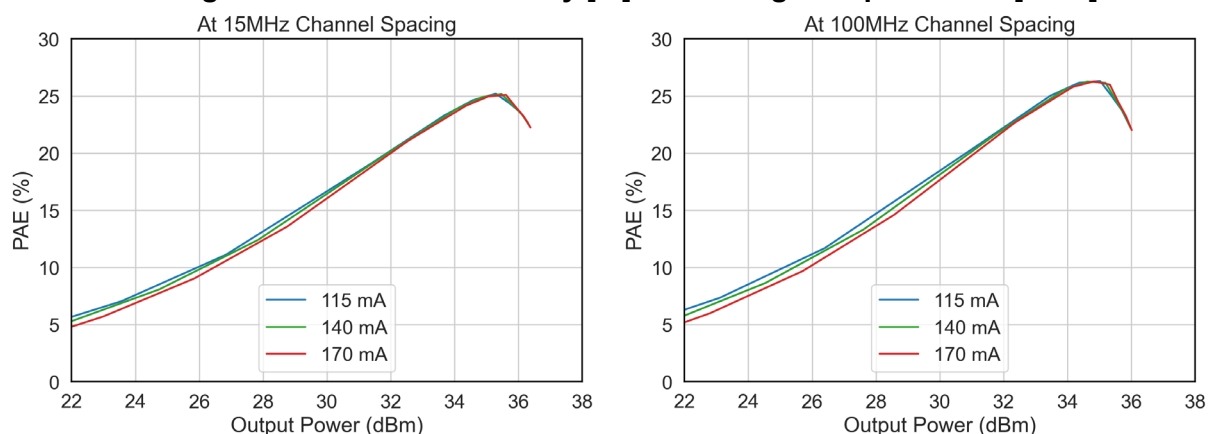
Adjacent Channel Power Ratio [dBc] vs. Average Output Power [dBm]



Average Gain [dB] vs. Average Output Power [dBm]



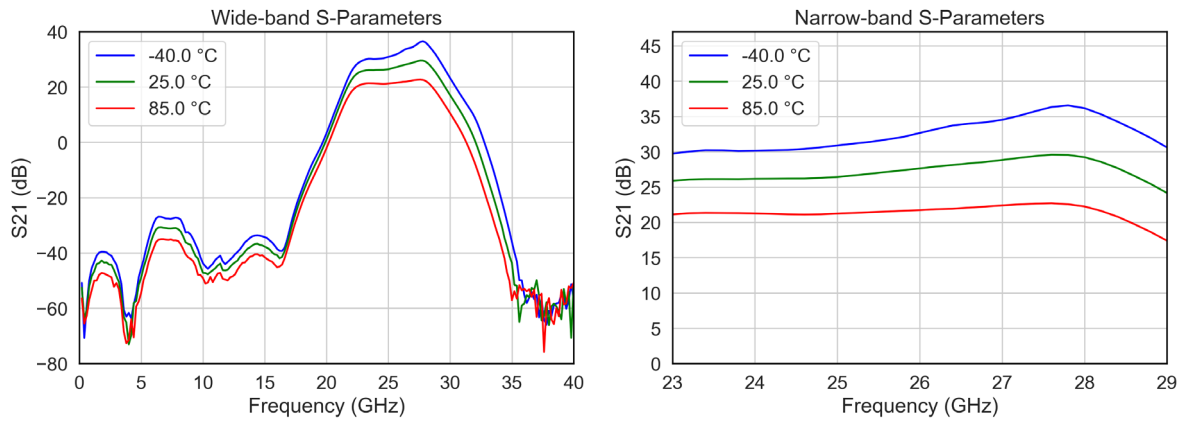
Average Power Added Efficiency [%] vs. Average Output Power [dBm]



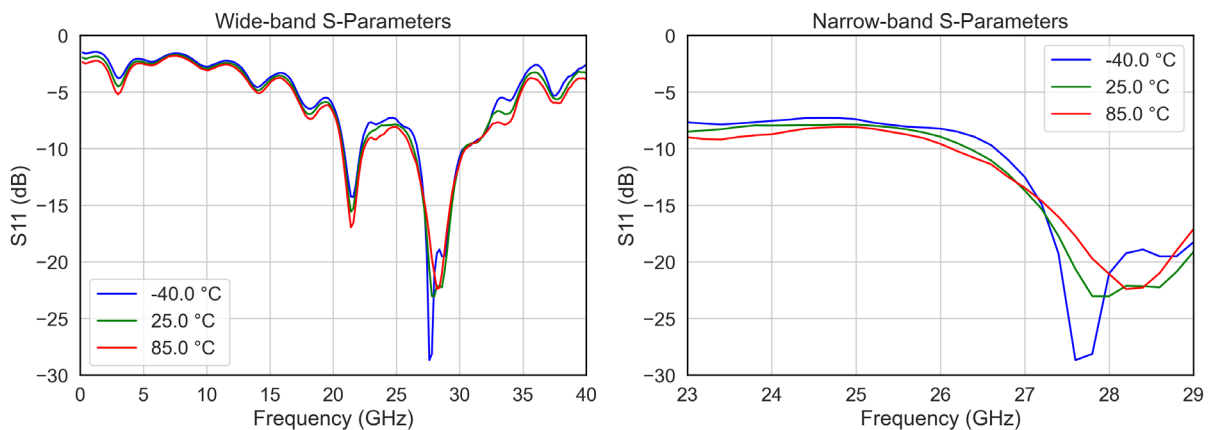
Typical Board Measurements : Small Signal

Test conditions : CW, $V_d = +20V$, $I_{dq} = 140mA$, $T_{case} = -40 / 25 / 85^{\circ}C$

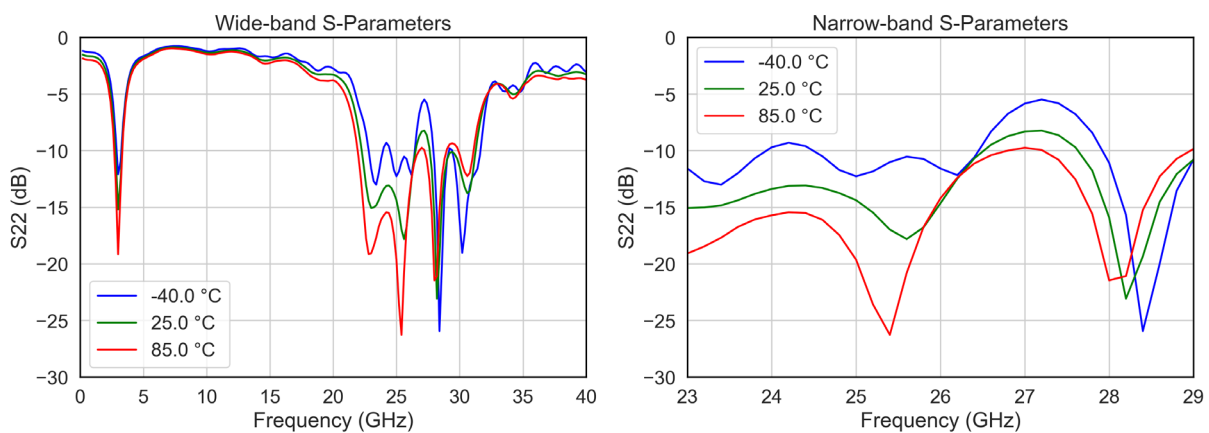
Linear Gain [dB] vs. Frequency [GHz]

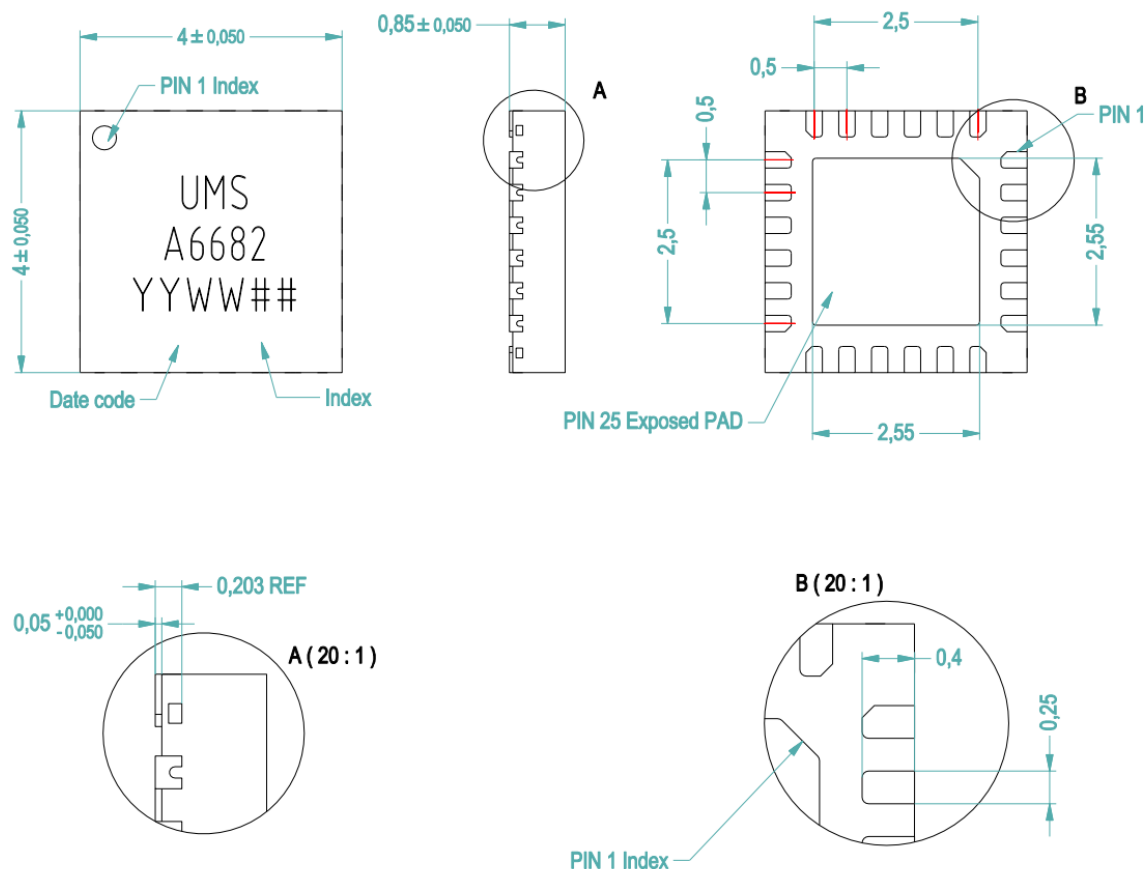


Input Return Loss [dB] vs. Frequency [GHz]



Output Return Loss [dB] vs. Frequency [GHz]



Package outline ⁽¹⁾

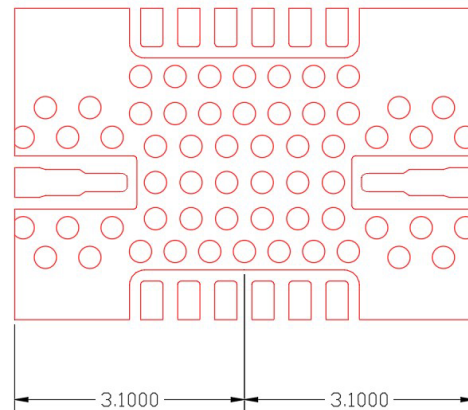
NiPdAuAg, Lead Free (Green)	1- NC	10- G3S	19- DET
Units : mm	2- NC	11- GND ⁽²⁾	20- VC
From the standard : JEDEC MO-220	3- GND ⁽²⁾	12- D3S	21- REF
NC : Not Connected	4- RF IN	13- NC	22- G3N
VGGD	5- GND ⁽²⁾	14- GND ⁽²⁾	23- D2N
	6- NC	15- RF OUT	24- D1
	7- G1	16- GND ⁽²⁾	25- GND ⁽²⁾
	8- G2	17- NC	
	9- D2S	18- NC	

⁽¹⁾ Refer to the application note AN0017 (<https://www.ums-rf.com>) for general consideration and recommendations for Molded Plastic QFN/DFN packages.

⁽²⁾ It is strongly recommended to ground all pins marked “GND” through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

Definition of measurement reference planes

The reference planes used for measurements given above are symmetrical from the symmetrical axis of the package (see drawing beside). The input and output reference planes are located at 3.1mm offset (input wise and output wise respectively) from this axis.



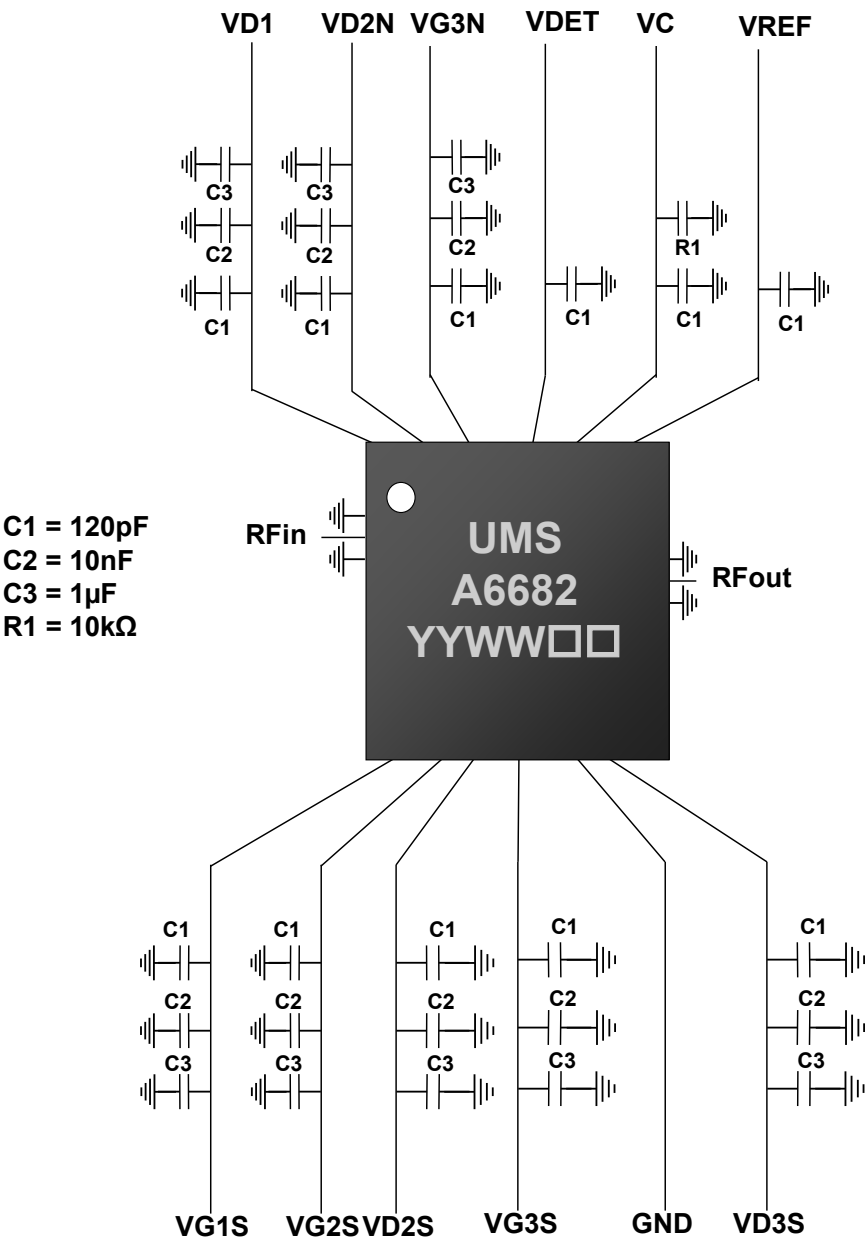
ESD sensitivity

Parameter	Classification	Standard
Human Body Model (HBM)	1A	ANSI/ESDA/JEDEC - JS-001

Package Information

Parameter	Value
Package body material	RoHS-compliant
	Low stress Injection Molded Plastic
Lead finish	100% Ni-Pd-Au-Ag
Moisture Sensitivity Level	MSL3

Recommended assembly plan



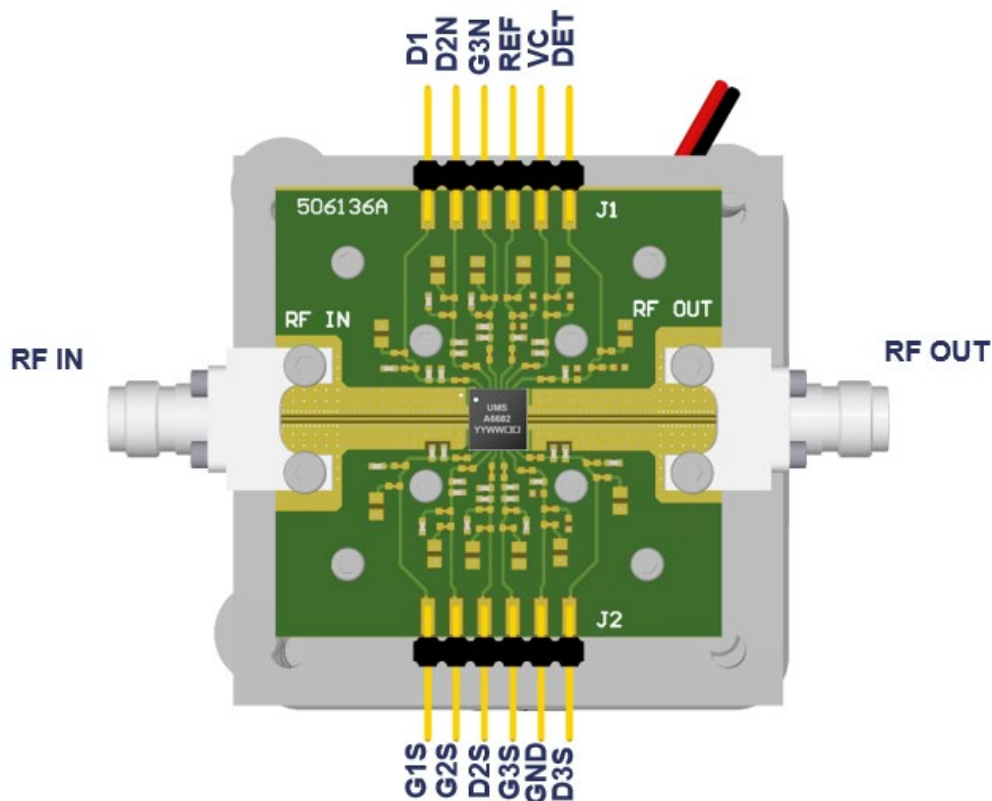
Recommended circuit bonding table

Label	Pin	Type	Decoupling	Comment
D1, D2S, D2N, D3S	9, 12, 24	Vd	120pF, 10nF & 1μF	Drain Supply
G1, G2, G3S, G3N	7, 8, 10, 22	Vg	120pF, 10nF & 1μF	Gate Supply
VC	20	Vc	120pF, 10kΩ	Detector Supply
DET, REF	19, 21	Detector	120pF	

Evaluation board

- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a micro-strip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 10nF $\pm 10\%$ are recommended for all DC access.
- See application note AN0017 for details.

Note: All board measurements are performed using **shielded cables**, even for DC bias, to ensure safe operation.



Notes

Due to ESD protection circuits on RF input and output, an external capacitance might be requested to isolate the product from external voltage that could be present on the RF accesses.

ESD protections are also implemented on gate and control access.

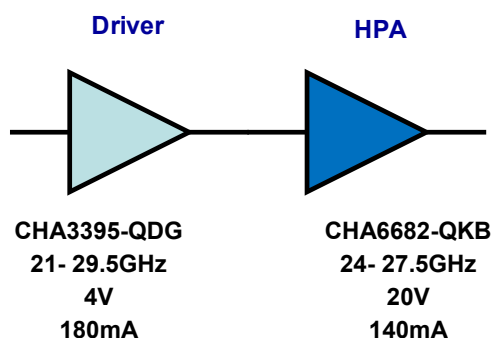
The DC connections do not include any decoupling capacitors in the package. Therefore it is mandatory to provide a good external DC decoupling (120pF, 10nF & 1µF) on the PC board as close as possible to the package.

Recommended UMS Power chain

The CHA6682-QKB is recommended with the CHA3395-QDG as driver.

Total Gain: 49dB

For more information about the CHA3395-QDG, see our web site <https://www.ums-rf.com>



SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017 at <https://www.ums-rf.com>.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACH N°1907/2006. More environmental data are available in the application note AN0019 also available at <https://www.ums-rf.com>.

Recommended ESD management

Refer to the application note AN0020 available at <https://www.ums-rf.com> for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

QFN 4x4 package:

CHA6682-QKB/XY

Stick: XY = 20

Tape & reel: XY = 21

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