United Monolithic Semiconductors

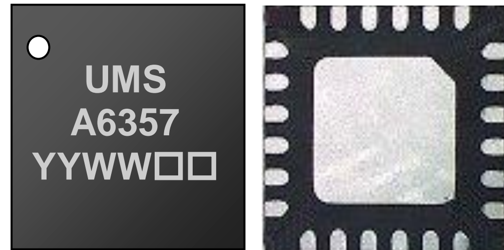
CHA6357-QKB

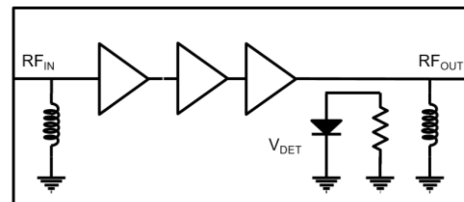
27 - 31 GHz 4W Power Amplifier

GaN Monolithic Microwave IC in SMD leadless package

Description

The CHA6357-QKB is a packaged monolithic High Power Amplifier exhibiting 4W output Power and 22 % of Power Added Efficiency over 27-31GHz bandwidth.
It is well suited for VSAT, SatCom uplink and 5G communication applications.
The circuit internally matches the input and output to 50Ohm and integrates ESD RF protection.
The circuit is manufactured on a robust GaN-on-SiC HEMT process and it is available in a standard surface mount 24 leads QFN 4x4 plastic package, compliant with the standards such as the directives RoHS N°2011/65 and REACh N°1907/2006.
In addition, the CHA6357, with output power back-off, provides high linearity with low consumption and can be used as a driver stage.

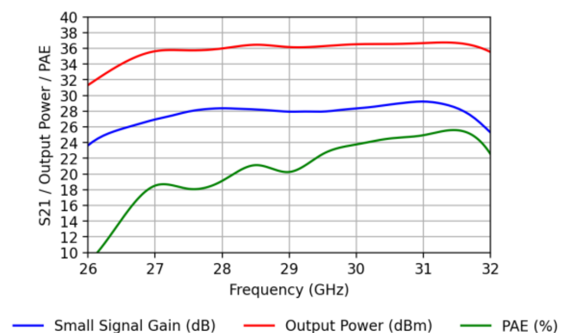




Main Features

- Broadband performances: 27-31GHz
- 28dB of small signal gain
- 36dBm Pout for +14dBm Input power
- >35 dBc ACPR at 26dBm Output power
- 20% PAE at 36dBm Output power
- DC bias: Vd=25V@Idq=70mA
- Output Power detector included
- 24 leads QFN plastic package 4x4mm²
- MSL3

Small Signal gain [dB], Output Power [dBm] and PAE [%] at Pin=14dBm & Tcase=25°C



Main Electrical Characteristics

Tcase = +25°C (Tcase : QFN backside temperature)

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	27		31	GHz
Gain	Linear Gain		28		dB
Psat	Saturated Output Power		36		dBm
PAE	Power Added Efficiency		20		%

Specifications

Tcase = +25°C, Vd = +25V

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	27		31	GHz
Gain	Linear Gain		28		dB
Psat	Saturated Output Power		36		dBm
PAE	Power Added Efficiency		20		%
S11 [1]	Input Return Loss		-11		dB
S22 [1]	Output Return Loss		-12		dB
Vdetect	Voltage detection V_{REF}- V_{DET} up to Psat		10 to 1200		mV
Idq	Total quiescent drain current		70		mA
Id	Total Drain current at saturation		800		mA

These values are representative of onboard measurements as defined on the drawing in paragraph "Evaluation mother board".

[1] Input and Output Return Losses are given at RF reference plan of Evaluation board (see Definition of the Sii reference plan section).

Absolute Maximum Ratings[2]

Tcase = +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	27	V
Id	Total Drain Current at saturation	1000	mA
Vg	Gate bias voltage	-7 to -1	V
Pin	Maximum peak input power overdrive	+20	dBm

[2] Operation of this device above anyone of these parameters may cause permanent damage.

Recommended Operating Range[3], [4]

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	25V	V
Idq	Total Quiescent Drain Current	55 to 140	mA
Pin	Input Power	14	dBm
Tj	Maximum Junction temperature[5]	200	°C

[3] Electrical performances are defined for specified test conditions

[4] Electrical performances are not guaranteed over all recommended operating conditions

[5] See Device thermal performances section

Temperature Range

Tcase	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +150	°C

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Typical Bias Conditions

Tcase=+25°C

Symbol	Pad N°	Parameter	Values	Unit
G1	7	Stage 1 Gate Supply	-5 to -1	V
G2	8	Stage 2 Gate Supply	-5 to -1	V
G3S	10	Stage 3 South Gate Supply	-5 to -1	V
G3N	22	Stage 3 North Gate Supply	-5 to -1	V
D1	24	Stage 1 Drain Supply	20 to 25	V
D2S	9	Stage 2 South Drain Supply	20 to 25	V
D2N	23	Stage 2 North Drain Supply	20 to 25	V
D3	12	Stage 3 Drain Supply	20 to 25	V
VC	20	Detector Supply	5	V
REF	19	Detector reference voltage		V
DET	21	Detector detected voltage		V

“Power ON” sequence

1. Bias HPA gate voltage at Vg close to Vpinch-off (Vg~-5V)
2. Set Vd bias voltage to 0V: Id=0mA
3. Apply Vd bias voltage, Vd = 25V: Id=0mA
4. Set Vc bias voltage to 5V for Detector biasing
5. Increase Vg up to quiescent bias drain current Idq
6. Apply RF input Power

“Power OFF” sequence

1. Turn off RF input power
2. Bias HPA Gate voltage at Vg~-5V: Id=0mA
3. Decrease Vd bias voltage down to 0V
4. Set Vc bias voltage to 0V
5. Turn Vg bias voltage to 0V

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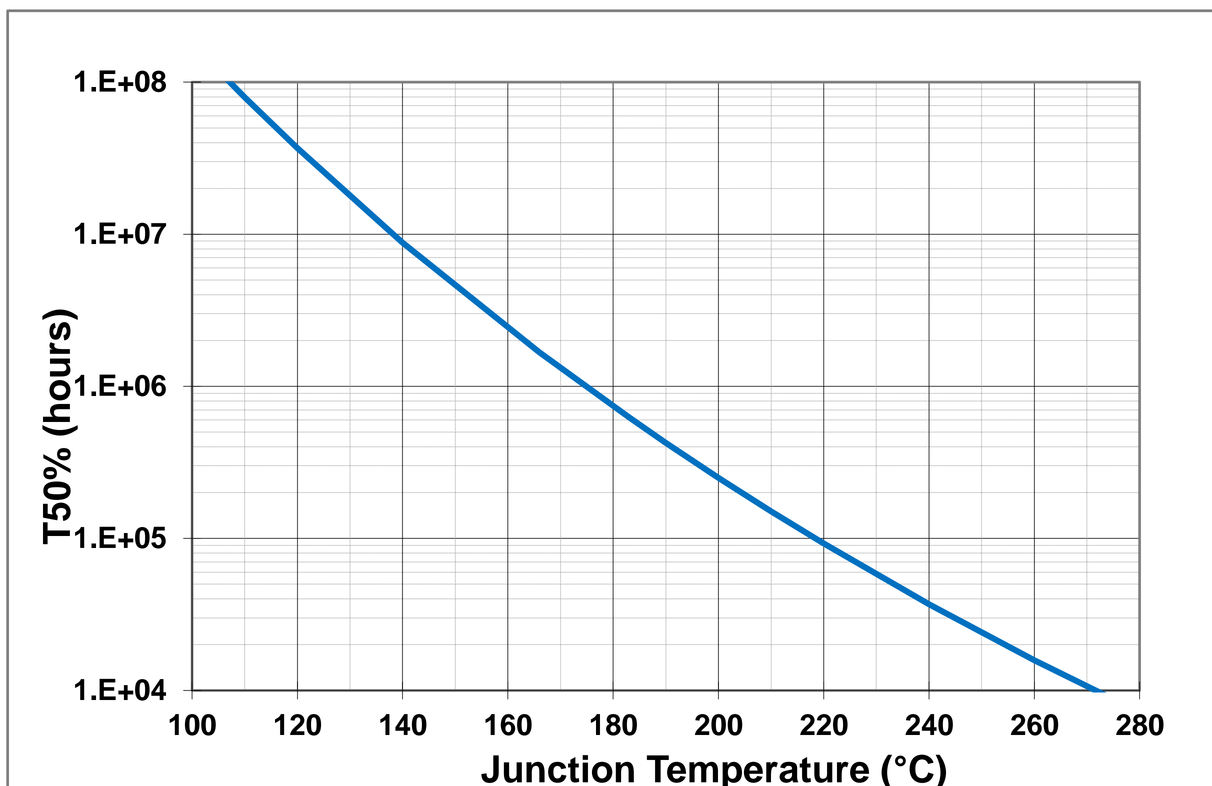
Device thermal performances

All the figures given in this section are obtained assuming that the QFN device is only cooled down by conduction through the package thermal pad (no convection mode considered).
The temperature is monitored at the package backside interface (Tcase).
For nominal operating, the system maximum temperature must be adjusted in order to guarantee that Tjunction remains below the maximum value specified in the Recommended Operating Ratings table. So the system PCB must be designed to comply with this requirement

Parameter	Biasing conditions	Tjunction (°C)	R_{TH} (°C/W)	T50 (hours)
R_{TH} (1) Thermal Resistance (Junction to Backside)	Vd=25V Pout=35.5dBm Pdiss=11.5W	198	9.8	2.8E+5
R_{TH} (1) Thermal Resistance (Junction to Backside)	Vd=25V Pout=32dBm Pdiss=7.6W	157	9.5	2.9E+6
R_{TH} (1) Thermal Resistance (Junction to Backside)	Vd=25V Pout=25dBm Pdiss=3.8W	118	8.7	4.3E+7

(1) Assuming 85°C Tcase



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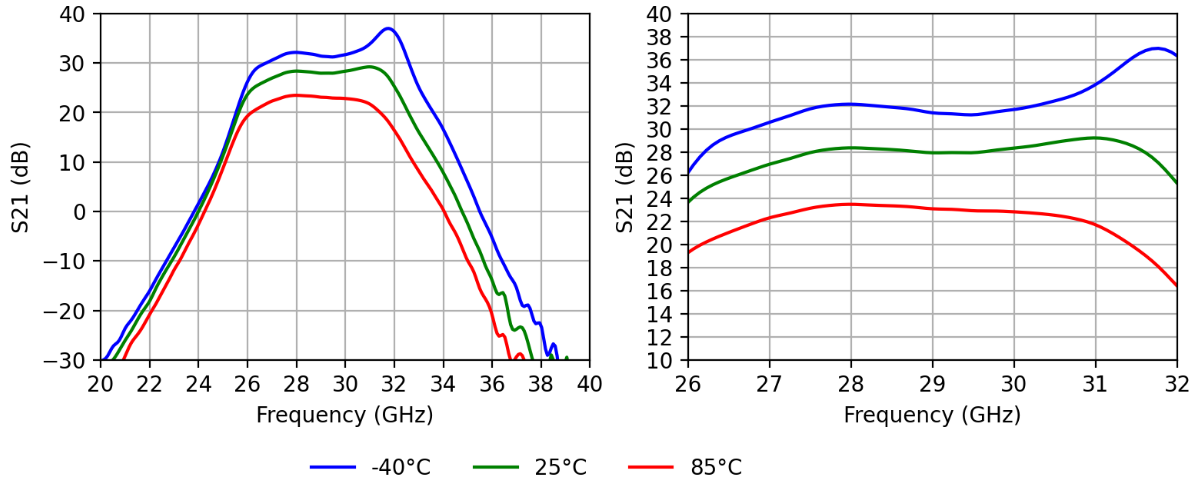
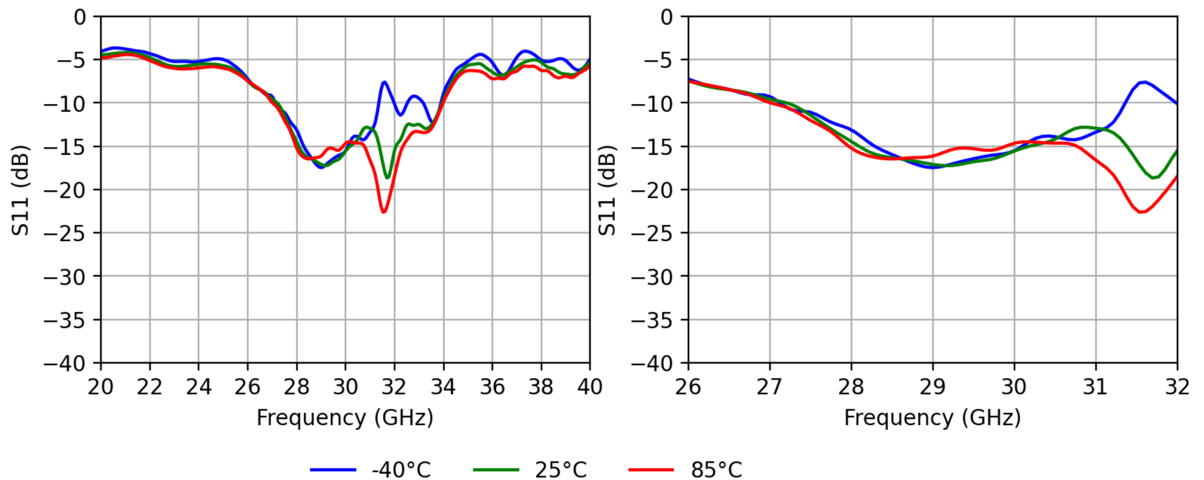
Typical Board Measurements : S-Parameters

Test conditions : CW, Vd = +25V, Idq = 70mA, T_{case} = -40°C / 25°C / 85°C

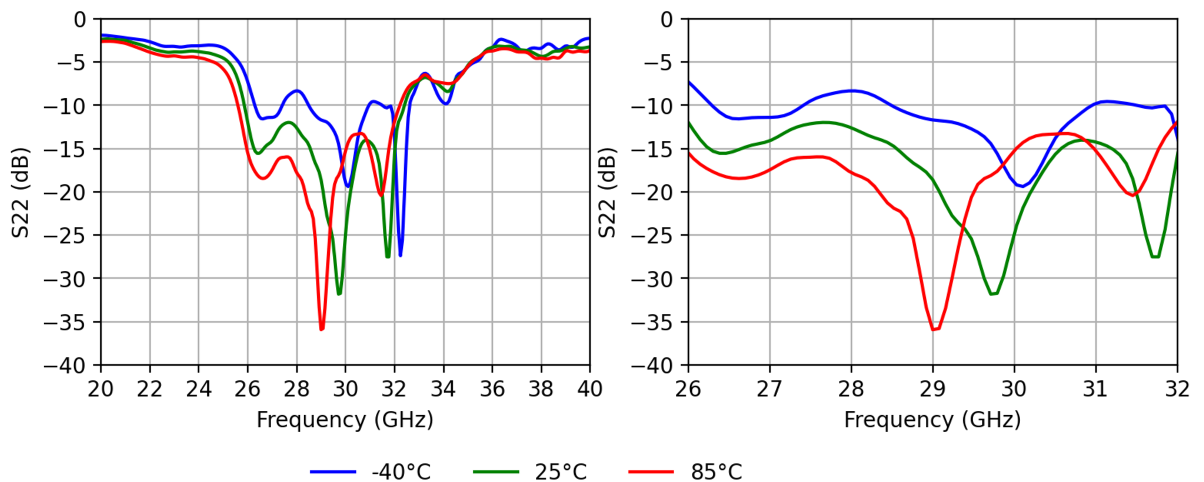
Linear Gain versus Frequency



Input Return Loss versus Frequency



Output Return Loss versus Frequency



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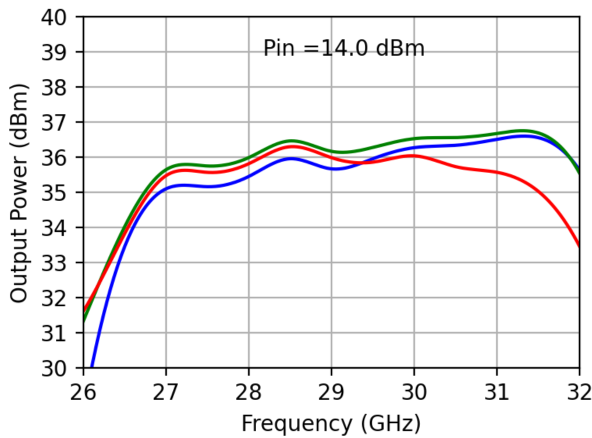
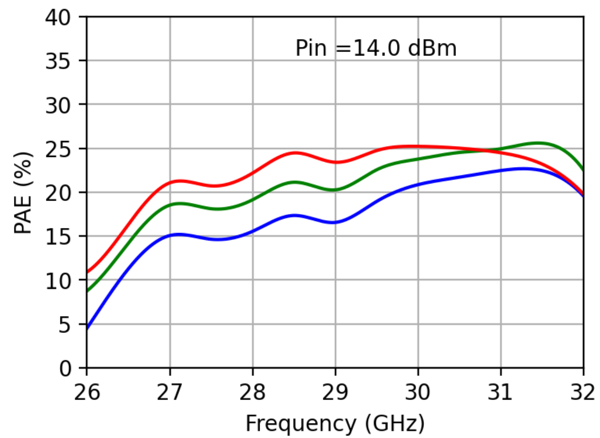
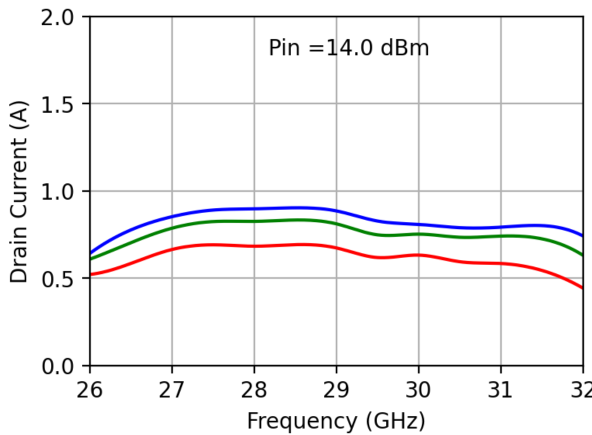
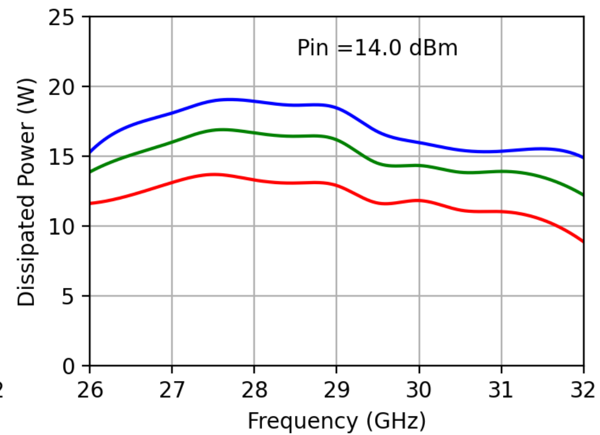
Typical Board Measurements : Large Signal

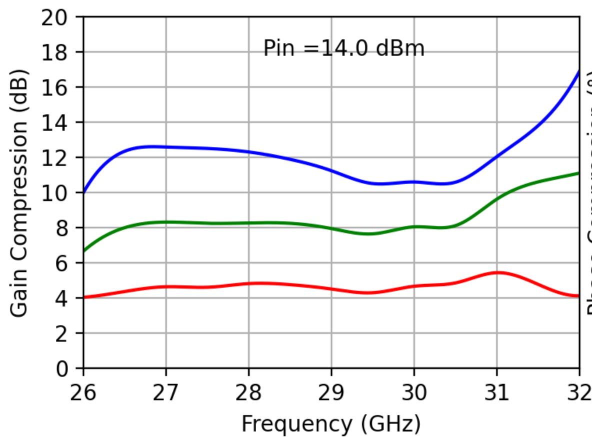
Test conditions : CW, Vd = +25V, Idq = 70mA, T_{case} = -20°C / 25°C / 85°C

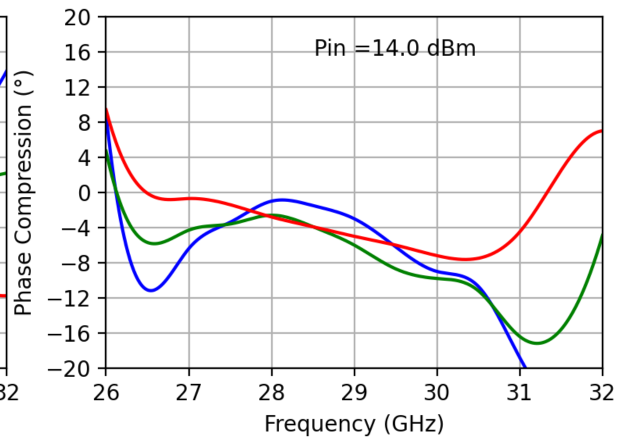












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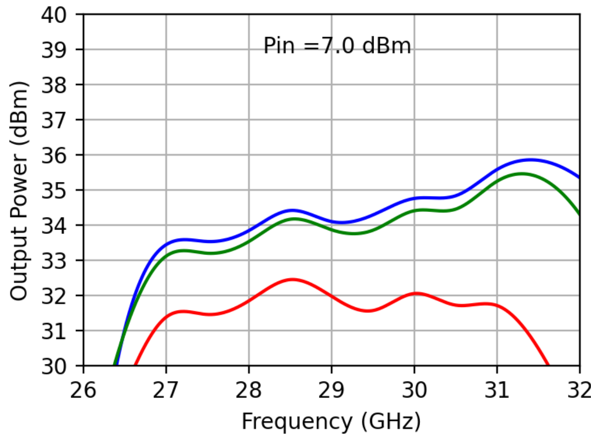
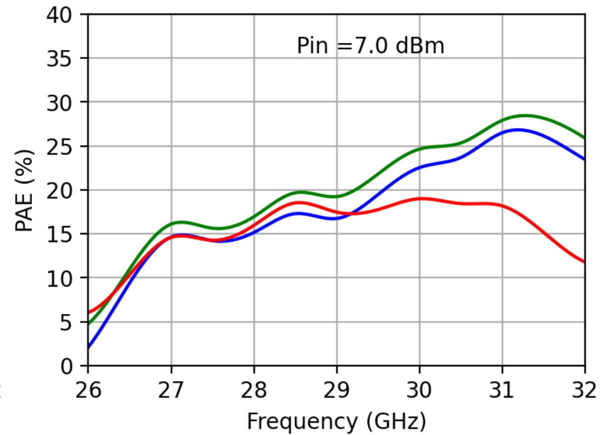
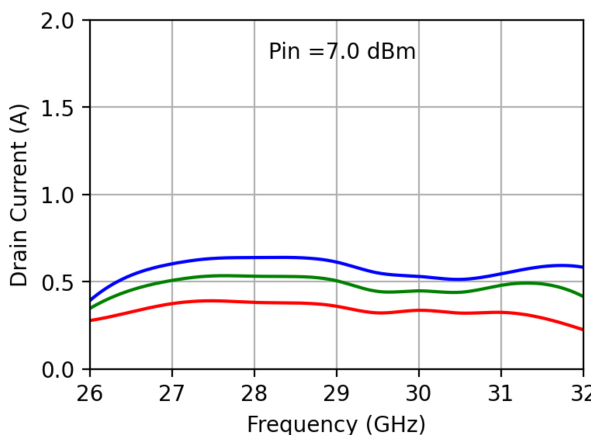
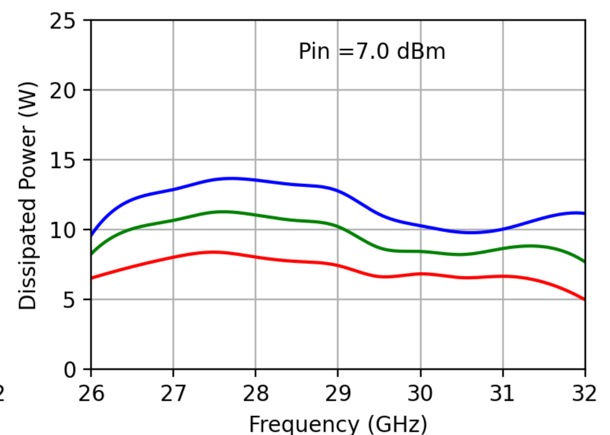
Typical Board Measurements : Large Signal

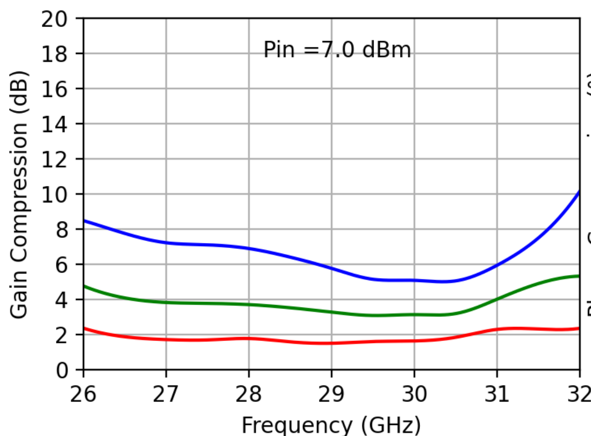
Test conditions : CW, Vd = +25V, Idq = 70mA, T_{case} = -20°C / 25°C / 85°C

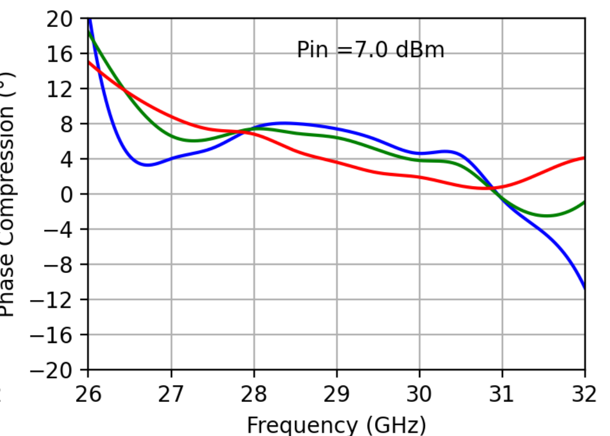












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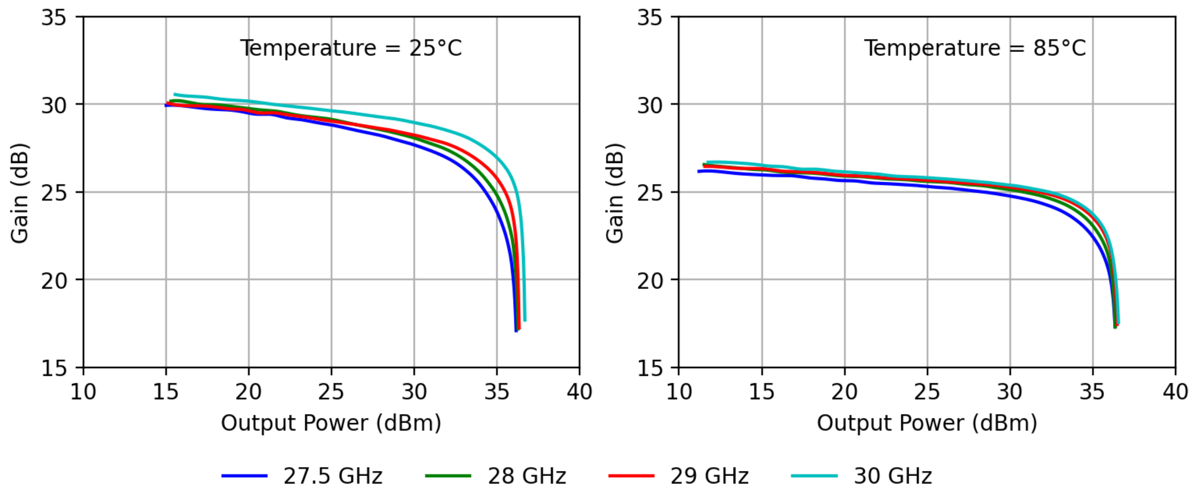
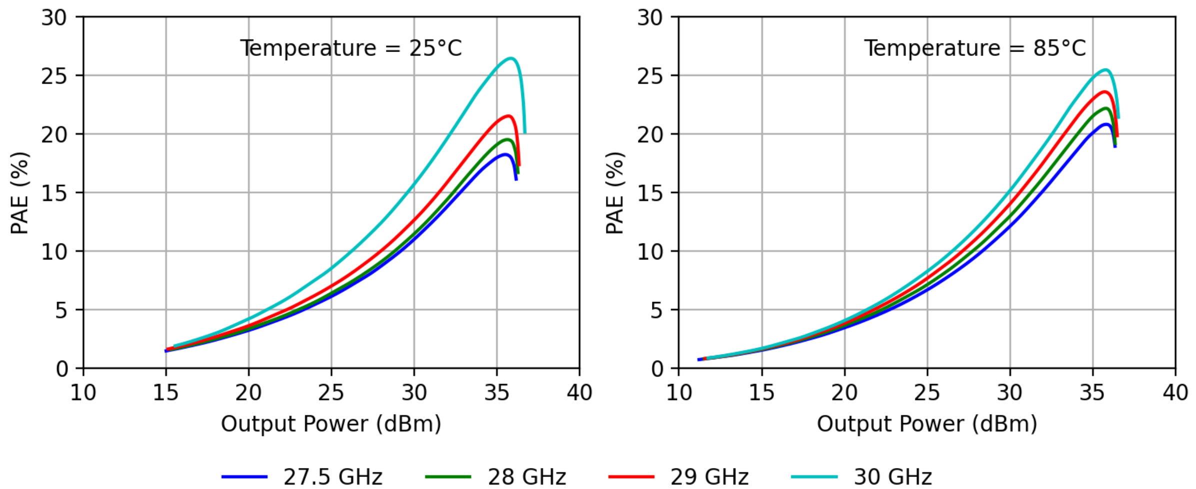
Typical Board Measurements : Large Signal

Test conditions : CW, Vd = +25V, Idq = 70mA, T_{case} = 25°C / 85 °C

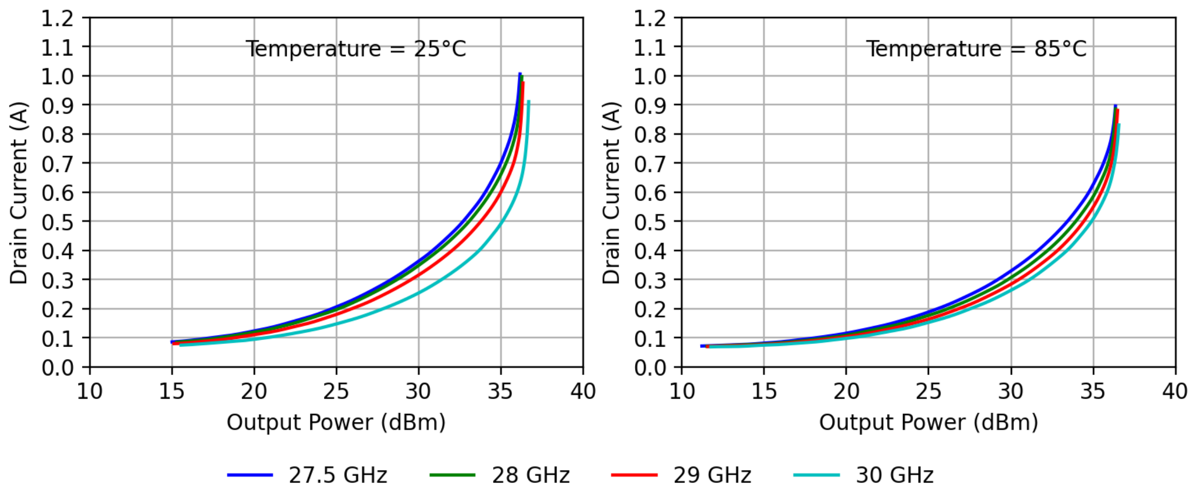
Gain versus Output Power



PAE versus Output Power



Drain Current versus Output Power



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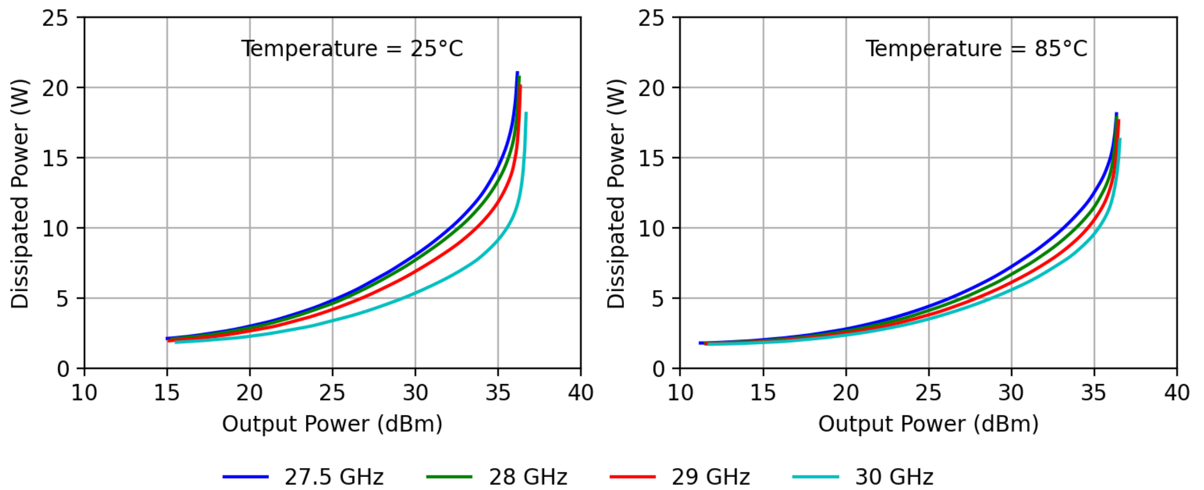
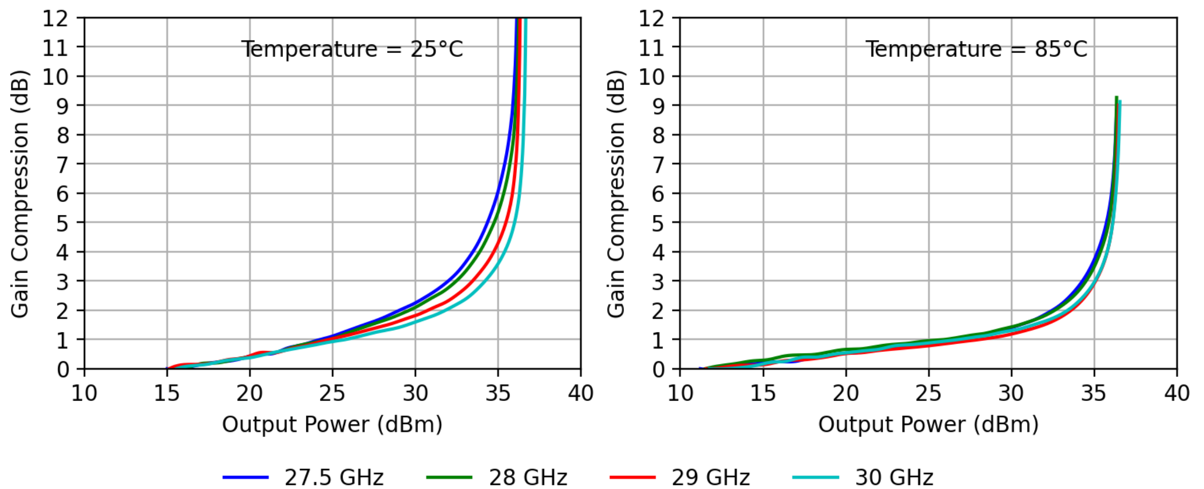
Typical Board Measurements : Large Signal

Test conditions : CW, Vd = +25V, Idq = 70mA, T_{case} = 25°C / 85 °C

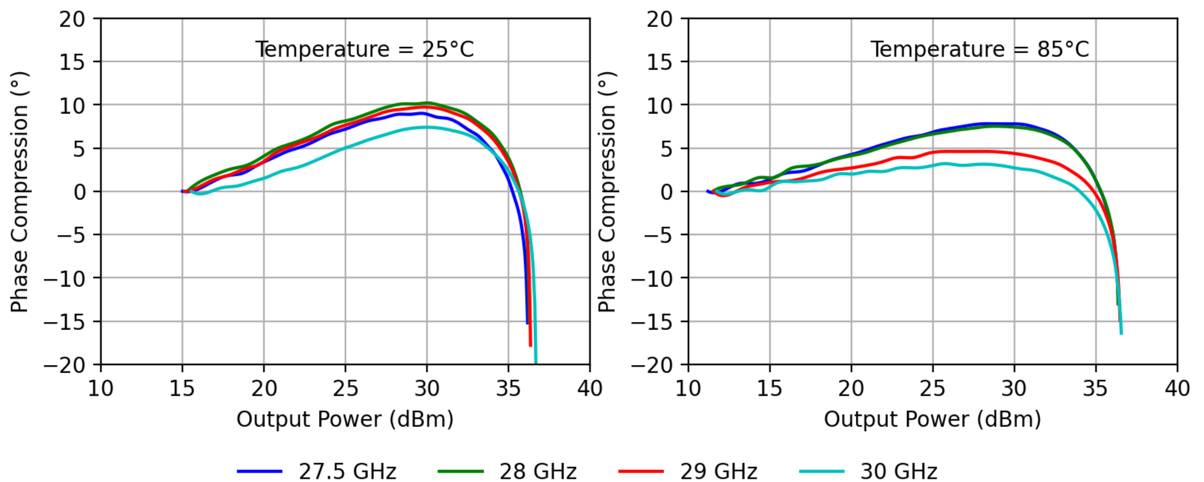
Dissipated Power versus Output Power



Gain Compression versus Output Power



Phase Compression versus Output Power



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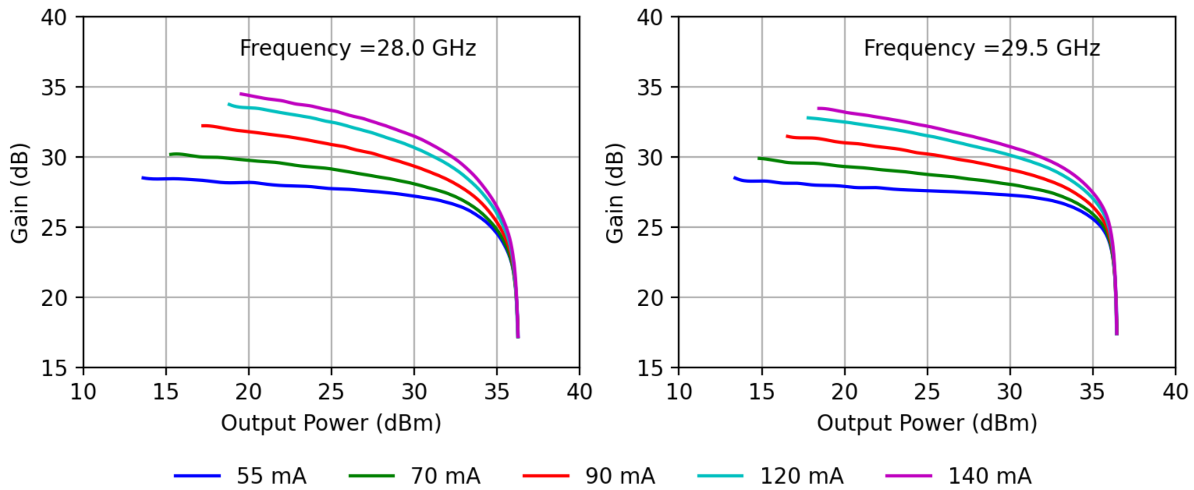
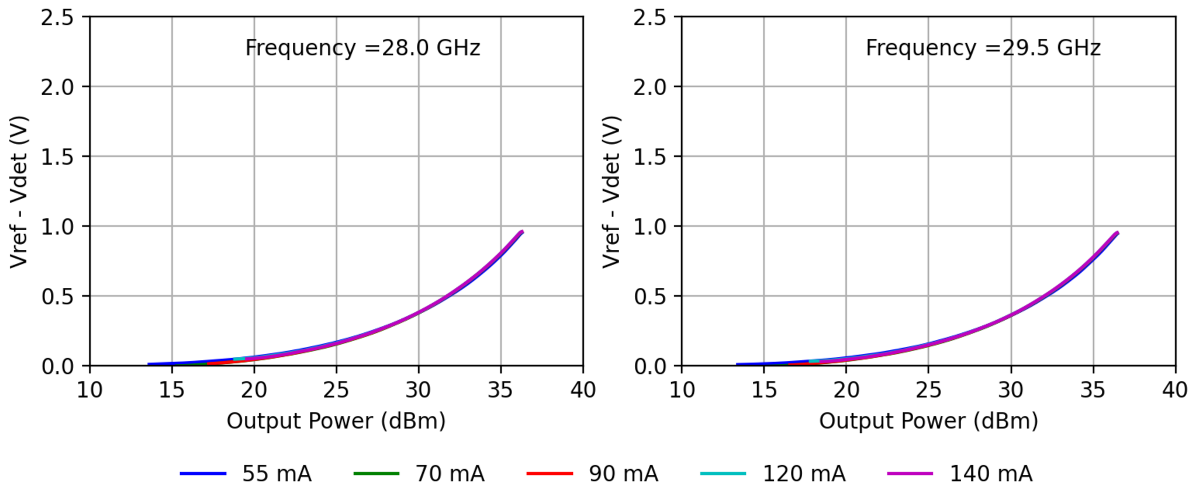
Typical Board Measurements : Large Signal

Test conditions : CW, Vd = +25V, Idq = 70mA, T_{case} = 25°C

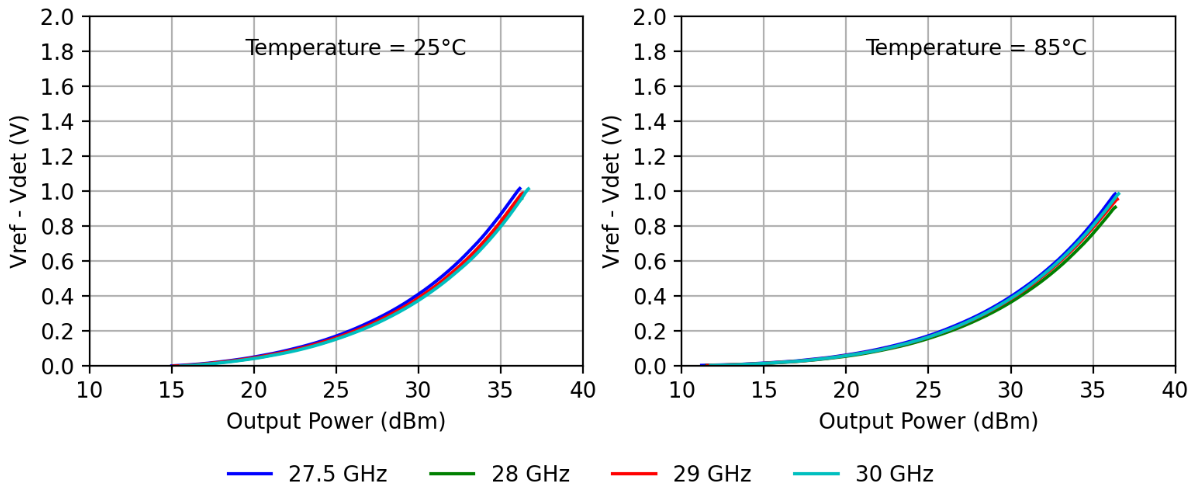
Gain versus Output Power and Quiescent Current



Power Detector versus Ouput Power and Quiescent Current



Power Detector versus Output Power and Frequency



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Typical Board Measurements : Linearity

Test conditions : CW, Vd = +25V, Idq = 70mA, T_{case} = 25°C, Carrier Frequency = 28.25 GHz
Modulation : 8PSK, Channel Spacing = 125 MHz, Roll-off = 0.2

Gain versus Output Power

Gain (dB) vs Output Power (dBm)

PAE versus Output Power

PAE (%) vs Output Power (dBm)

55 mA — 70 mA — 90 mA — 120 mA — 140 mA

EVM versus Output Power

EVM (dB) vs Output Power (dBm)

ACPR versus Output Power

ACPR (dBc) vs Output Power (dBm)

____ ACPR High
...... ACPR Low

55 mA — 70 mA — 90 mA — 120 mA — 140 mA

DC power versus Output Power

DC Power Consumption (W) vs Output Power (dBm)

Dissipated Power versus Output Power

Dissipated Power (W) vs Output Power (dBm)

55 mA — 70 mA — 90 mA — 120 mA — 140 mA

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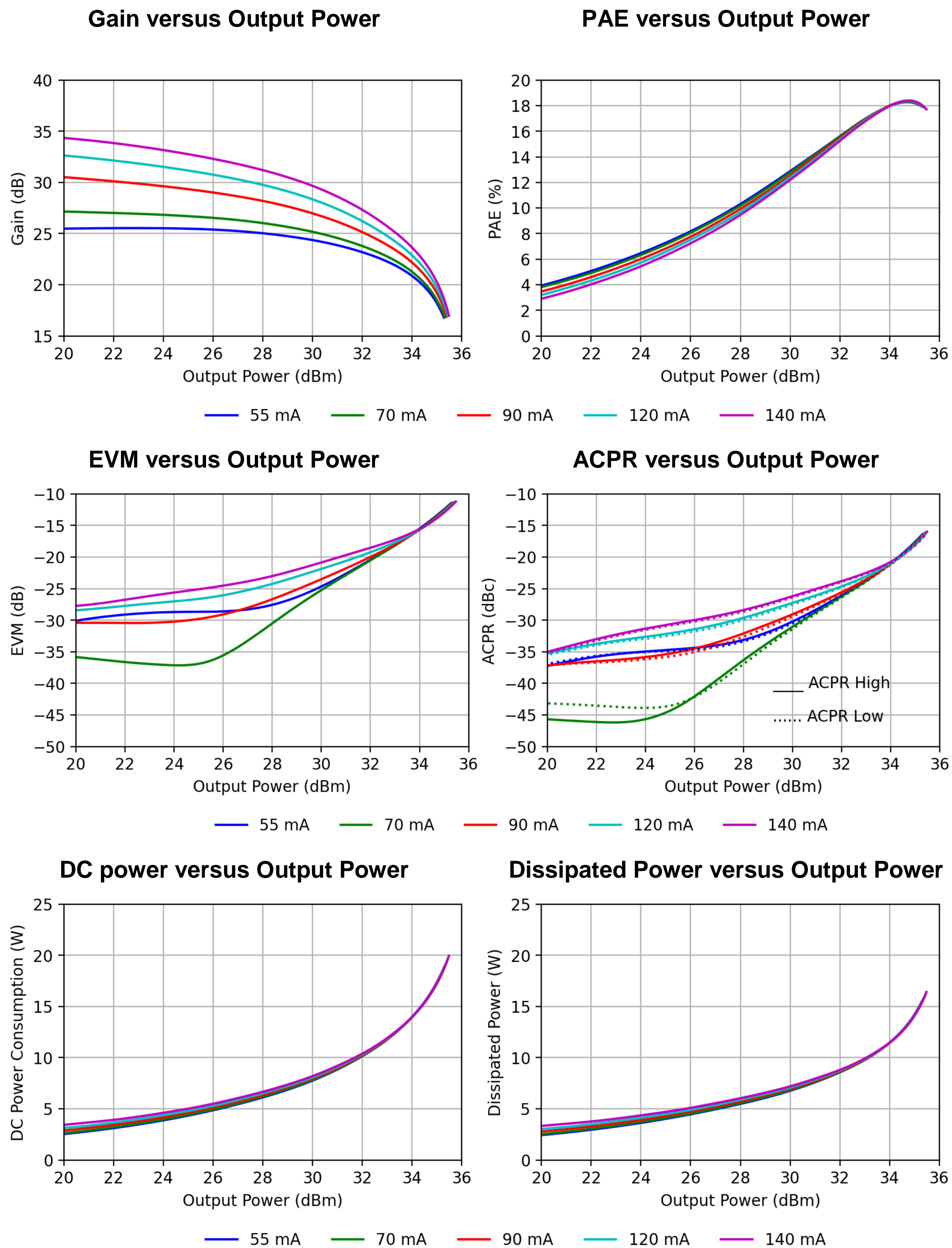
Typical Board Measurements : Linearity

Test conditions : CW, Vd = +25V, Idq = 70mA, T_{case} = 25°C, Carrier Frequency = 28.25 GHz
Modulation : 1024QAM, Channel Spacing = 50 MHz, Roll-off = 0.2



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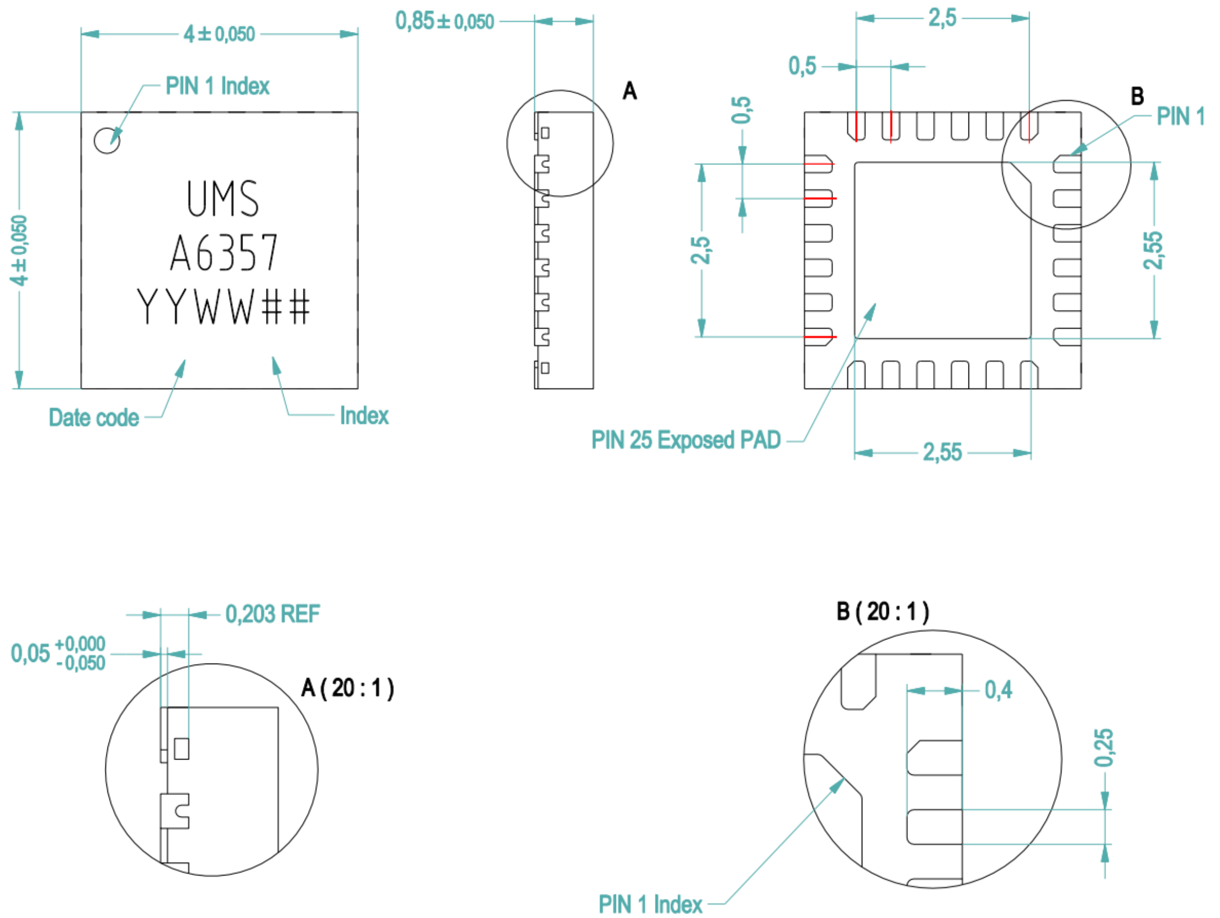
Package outline



Ni-Pd-Au-Ag Lead free	(Green)	1-	Nc	10-	G3S	19-	DET
Units :	mm	2-	Nc	11-	GND(1)	20-	VC
From the standard :	JEDEC MO-220	3-	GND(1)	12-	D3	21-	REF
		4-	IN	13-	Nc	22-	G3N
		5-	GND(1)	14-	GND(1)	23-	D2N
		6-	Nc	15-	OUT	24-	D1
		7-	G1	16-	GND(1)	25-	GND(1)
		8-	G2	17-	Nc		
		9-	D2S	18-	Nc		

(1) It is strongly recommended to ground all pins marked “GND” through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

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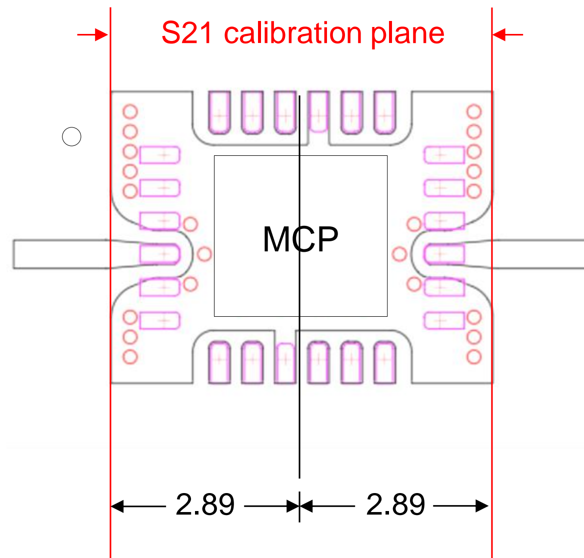
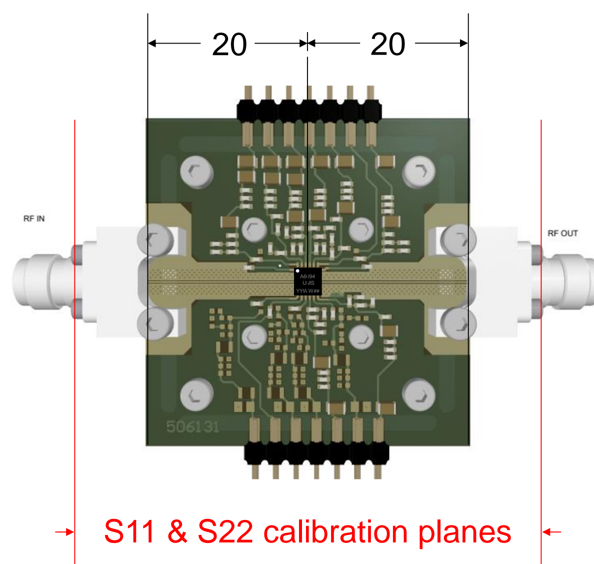
Definition of the Sij reference planes

The reference planes used for S21 measurements are symmetrical from the central axis of the package (see drawing beside). The input and output reference planes are located at 2.89mm offset from the central axis. The S21 parameter measurements include this given PCB pattern (see paragraph "Evaluation board").



Definition of the Sii reference planes

The reference planes used for S11 and S22 measurements are symmetrical from the central axis of the package (see drawing beside). The input and output reference planes are located at 20mm offset from the central axis. The S11 and S22 measurements include this given PCB patter, the RF lines of the evaluation board and the RF connectors.



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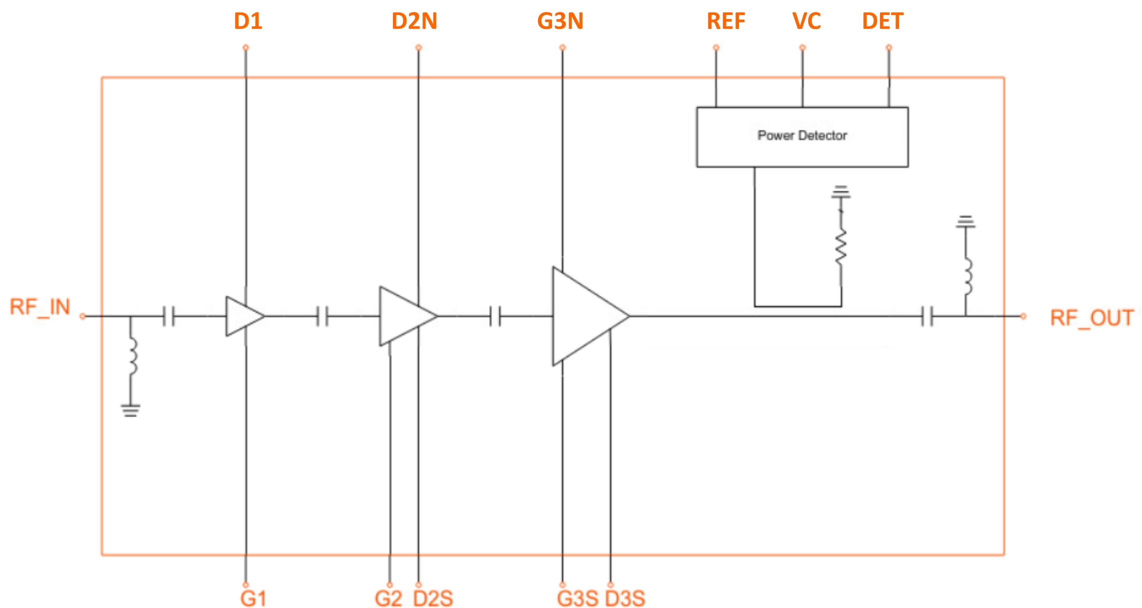
ESD sensitivity

Parameter	Classification	Standard
Human Body Model (HBM)	1A	ANSI/ESDA/JEDEC - JS-001

Package Information

Parameter	Value
Package body material	RoHS-compliant
	Low stress Injection Molded Plastic
Lead finish	100% Ni-Pd-Au-Ag
MSL Rating	MSL3

DC Schematic



Notes

Due to ESD protection circuits on RF input and output, an external capacitance might be requested to isolate the product from external voltage that could be present on the RF accesses.

The DC connections do not include any decoupling capacitor in package, therefore it is mandatory to provide a good external DC decoupling (120pF, 10nF) on the PC board, as close as possible to the package.

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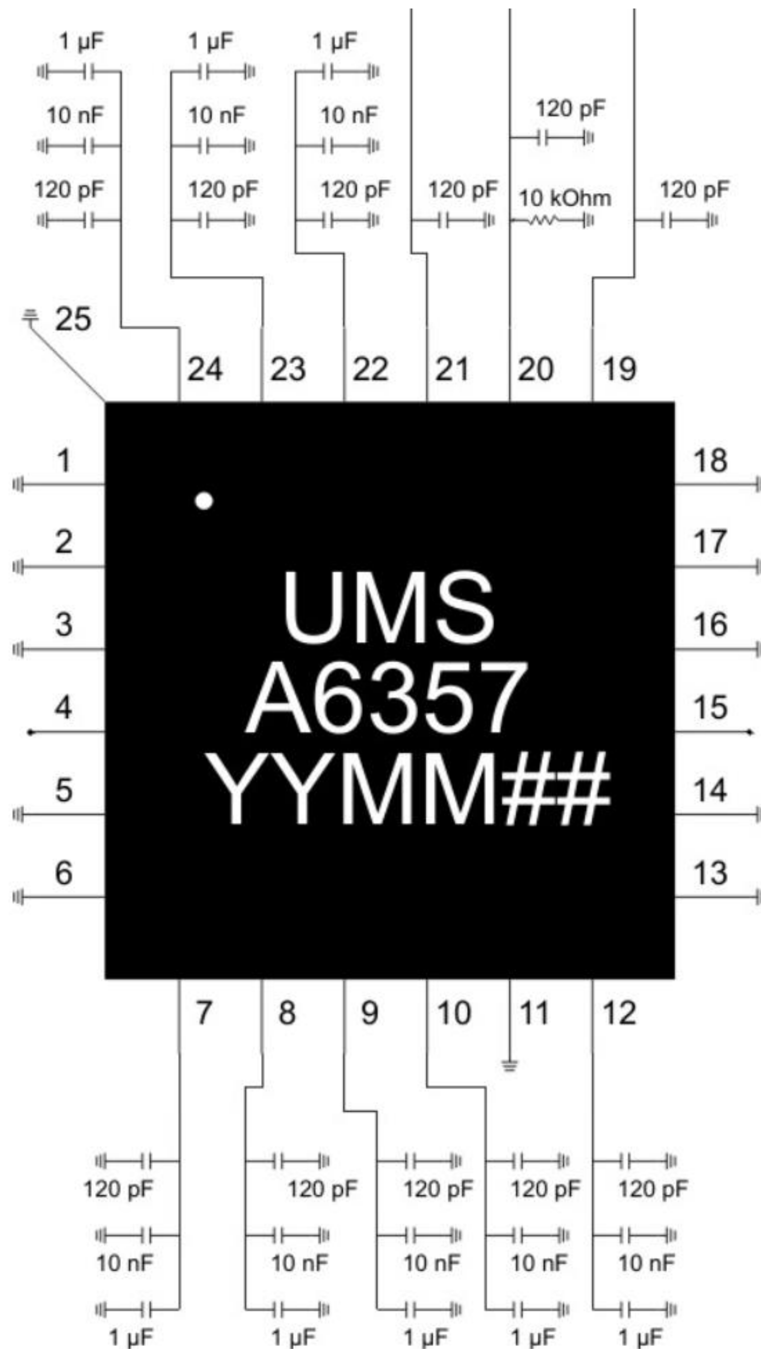
Recommended assembly plan



Recommended circuit bonding table

Label	Pin	Type	Decoupling	Comment
D1, D2S, D2N, D3	24, 9, 23, 12	Vd	120pF, 10nF & 1µF	Drain Supply
G1, G2, G3S, G3N	7, 8, 10, 22	Vg	120pF, 10nF & 1µF	Gate Supply
VC	20	Vc	10kΩ & 120pF	Detector Supply
DET, REF	19, 21	Vdet, Vref	120pF	Detection voltages

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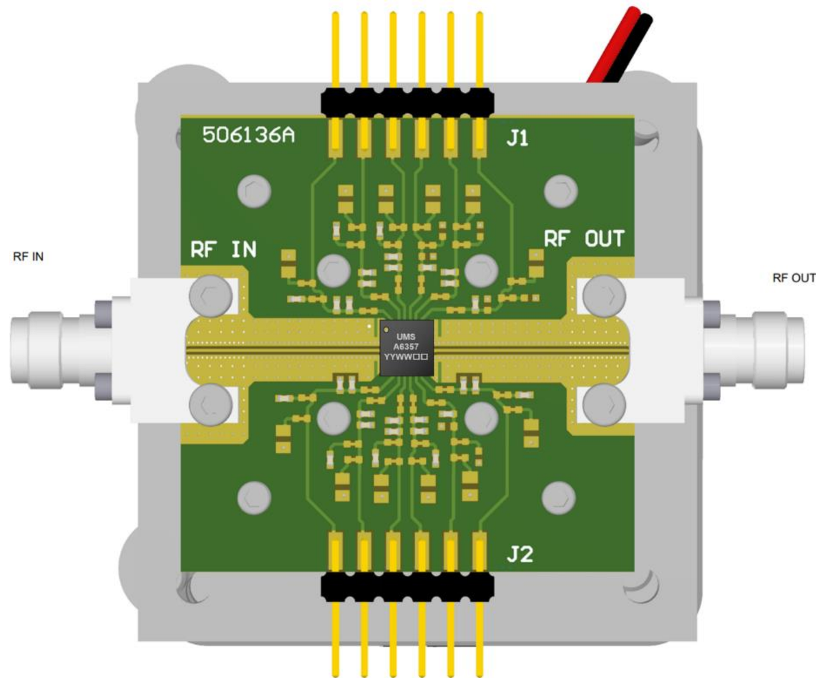
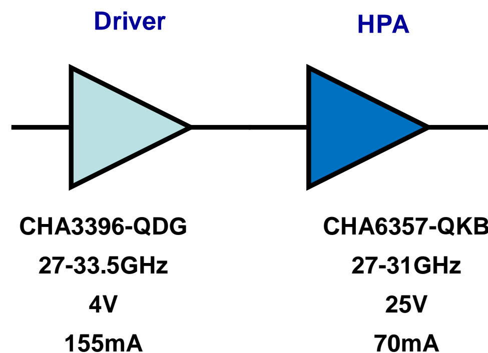
Evaluation board

■ Compatible with the proposed footprint.
■ Based on typically Ro4003 / 8mils or equivalent.
■ Using a micro-strip to coplanar transition to access the package.
■ Recommended for the implementation of this product on a module board.
■ Decoupling capacitors of 120pF, 10nF and 1µF ±10% are recommended for all DC pins.
■ See application note AN0017 for details.
■ To ensure safe operation, all measurements must be performed using **shielded cables, even for DC bias.**



Recommended UMS Power chain

The CHA6357-QKB is recommended with the CHA3396-QDG.
For more information about the CHA3396-QDG, see our web site www.ums-rf.com



CHA3396-QDG	CHA6357-QKB
27-33.5GHz	27-31GHz
4V	25V
155mA	70mA

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Recommended package footprint

Refer to the application note AN0017 available at https://www.ums-rf.com for package foot print recommendations.

SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017 at https://www.ums-rf.com.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at https://www.ums-rf.com.

Recommended ESD management

Refer to the application note AN0020 available at https://www.ums-rf.com for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

QFN 4x4 package:	CHA6357-QKB/XY	
	Stick: XY = 20	Tape & reel: XY = 21

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