United Monolithic Semiconductors

CHA6354-QQA

27.5 - 30GHz 4W HPA with SPDT

GaN Monolithic Microwave IC in QFN package

Description

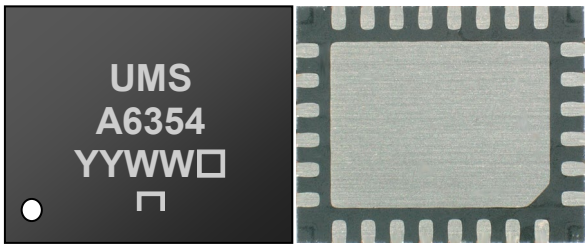
The CHA6354-QQA is a three stage monolithic GaN High Power Amplifier reaching 4W output power over 27.5-30GHz bandwidth. It includes a SPDT switch at the output.

The CHA6354-QQA provides high linearity with low consumption.

It is well suited for SatCom uplink and 5G communication applications.

The circuit is manufactured on a robust GaN-on-SiC HEMT technology. The input and output are internally matched to 50Ohms and integrate ESD RF protection.

It is available in standard surface mount 28 Leads QFN 5x4. It is supplied in RoHS compliant SMD package.

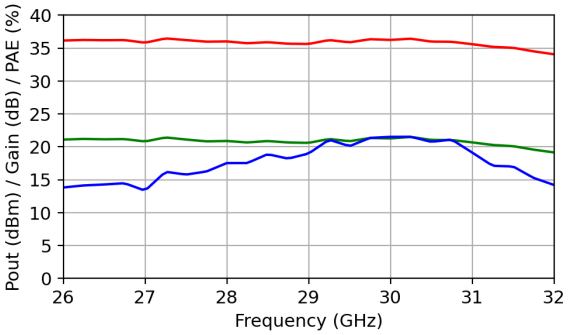


Main Features

- Broadband performances: 27.5 – 30GHz
- Pout = 36dBm @ Pin = 15dBm
- ACPR(1) = -34dBc @ Pavg = 33dBm (3dB OBO)
- DC bias: Vd=25V @ Id = 120mA
- 28 Leads QFN 5x4
- MSL3

(1) 30MHz modulation bandwidth, 8PSK

Output Power / **Gain** / **PAE** versus Frequency **@Pin = 15dBm**



Main Electrical Characteristics

Tcase = +25°C (Tcase: QFN backside temperature)

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	27.5		30	GHz
Gain	Linear Gain		27		dB
ACPR	ACPR @ Pavg = 33dBm (3dB OBO) with 8PSK modulation (BW=30MHz)		-34		dBc
Psat	Saturated Output Power		36		dB
Sw_Iso	Switch Issolation		40		dB

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Bât. Charmille - Parc Mosaic - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
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Specifications

Tcase = +25°C, Vd = +25V

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	27.5		30	GHz
Gain	Linear Gain		27		dB
Psat	Saturated Output Power		36		dBm
PAE	Power Added Efficiency		17		%
ACPR	ACPR @ Pavg = 33dBm (3dB OBO) with 8PSK modulation (BW=30MHz)		-34		dBc
ACPR	ACPR at 35dBm output power with 8PSK modulation (BW=30MHz)		-28		dBc
S11	Input return loss		-9		dB
S22	Output return loss		-15		dB
Sw_Iso	Switch Isolation		40		dB

These values are representative of on-board measurements as defined on the drawing in paragraph "Evaluation board".

Absolute Maximum Ratings (1)

Tcase = +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	27	V
Id	Quiescent Drain bias current	400	mA
Vg	Gate bias voltage	-6 to -1	V
Pin	Maximum input power	20	dBm

(1) Operation of this device above anyone of these parameters may cause permanent damage.

Recommended Operating Range (3), (4)

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	25	V
Id	Quiescent Drain bias current	120 - 260	mA
Pin	Maximum input power	18	dBm
Tj	Maximum Junction temperature (2)	200	°C

(2) See Device thermal performances section
(3) Electrical performances are defined for specified test conditions
(4) Electrical performances are not guaranteed over all recommended operating conditions

Temperature Range

Tcase	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +150	°C

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Typical Bias Conditions

Tcase=+25°C

Symbol	Pad N°	Parameter	Values	Unit
G1	1	Stage 1 Gate Supply	-5 to -2	V
G2	2	Stage 2 Gate Supply	-5 to -2	V
G3S	5	Stage 3 South Gate Supply	-5 to -2	V
G3N	21	Stage 3 North Gate Supply	-5 to -2	V
D1	24	Stage 1 Drain Supply	20 to 25	V
D2S	3	Stage 2 South Drain Supply	20 to 25	V
D2N	22	Stage 2 North Drain Supply	20 to 25	V
D3	20	Stage 3 Drain Supply	20 to 25	V
SWN	15	North Switch gate Voltage	0 / 25	V
SWS	8	South Switch gate Voltage	0 / 25	V

“Power ON” sequence

1. Ground the device
2. Set the Gate voltage Vg to -5V
3. Set 25 V to SWN and 0 V to SWS to activate north path or set 0 V to SWN and 25V to SWS to activate south path
4. Set the Drain voltage Vd to 25V
5. Increase the gate voltage up to quiescent bias drain current Id
6. Apply RF signal

“Power OFF” sequence

1. Turn off RF signal
2. Decrease the Gate voltage Vg to -5V
3. Decrease the Drain voltage Vd to 0V
4. Set SWN, SWS voltage to 0V
5. Turn off Vg supply

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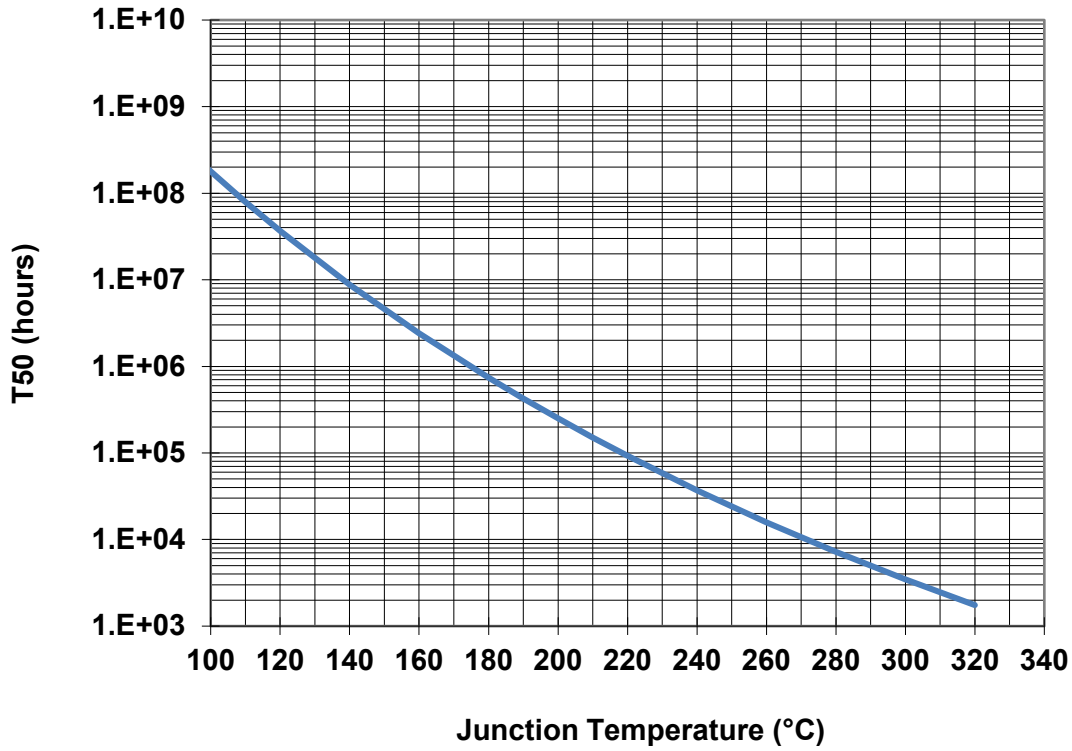
Device thermal performances

All the figures given in this section are obtained assuming that the QFN device is only cooled down by conduction through the package thermal pad (no convection mode considered).
The temperature is monitored at the package back-side interface (Tcase).
The system maximum temperature must be adjusted in order to guarantee that Tjunction remains below the maximum value specified in the Absolute Maximum Ratings table.
So, the system PCB must be designed to comply with this requirement.

Parameter	Biasing conditions	Tjunction (°C)	RTH (°C/W)	T50 (hours)
RTH (1) Thermal Resistance (Junction to QFN Backside)	Vd=25V Pout=35dBm Pdiss=15.9W	194	6.85	3.5E+5

[1] Assuming 85°C Tcase



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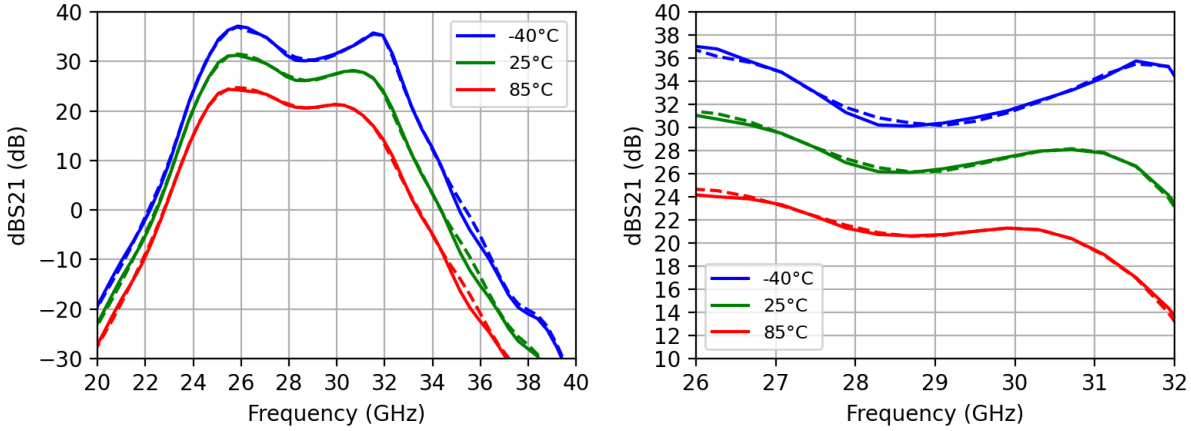
Typical Board Measurements : S-Parameters

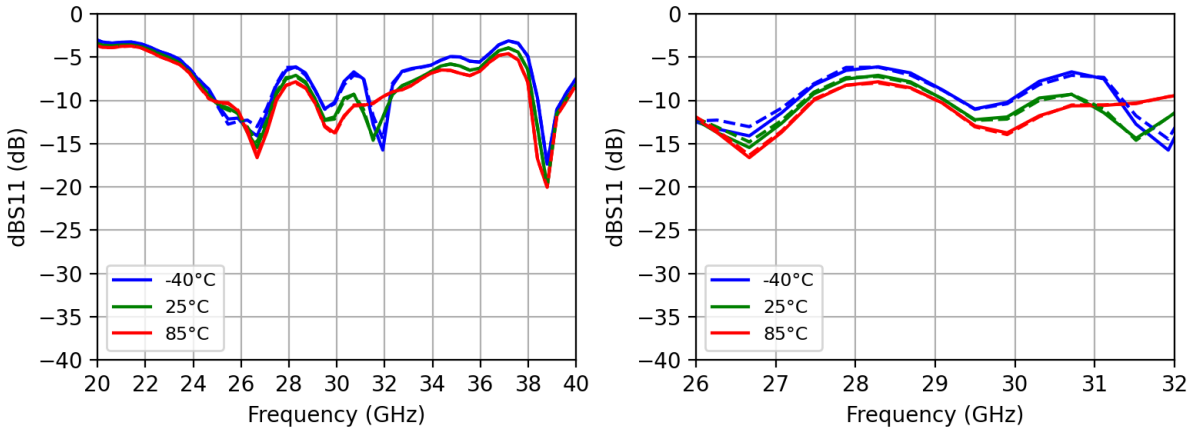
Test conditions : CW, Vd = +25V, **Id = 120mA**, T_{case} = -40°C / 25°C / 85°C

Linear Gain versus Frequency



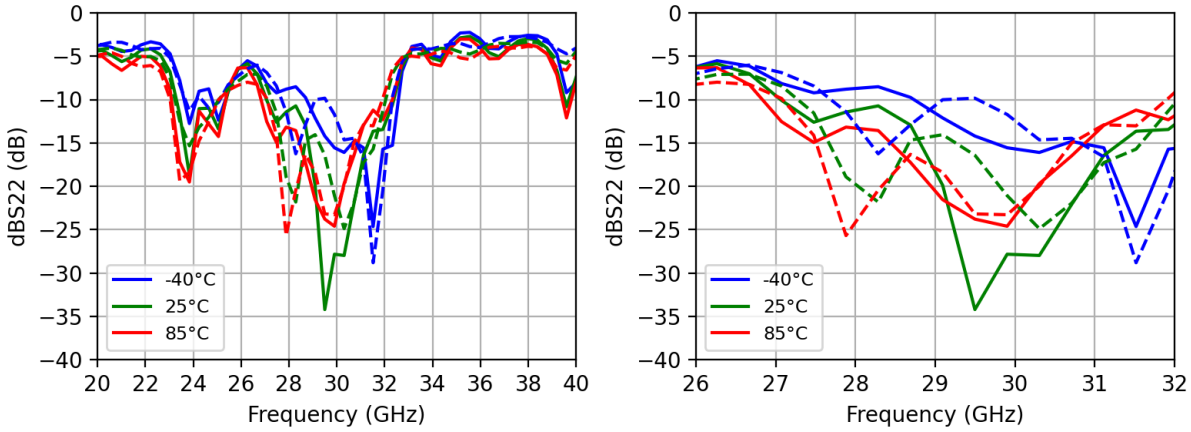
Line : North Path / Dot : South Path

Input Return Loss versus Frequency



Line : North Path / Dot : South Path

Output Return Loss versus Frequency



Line : North Path / Dot : South Path

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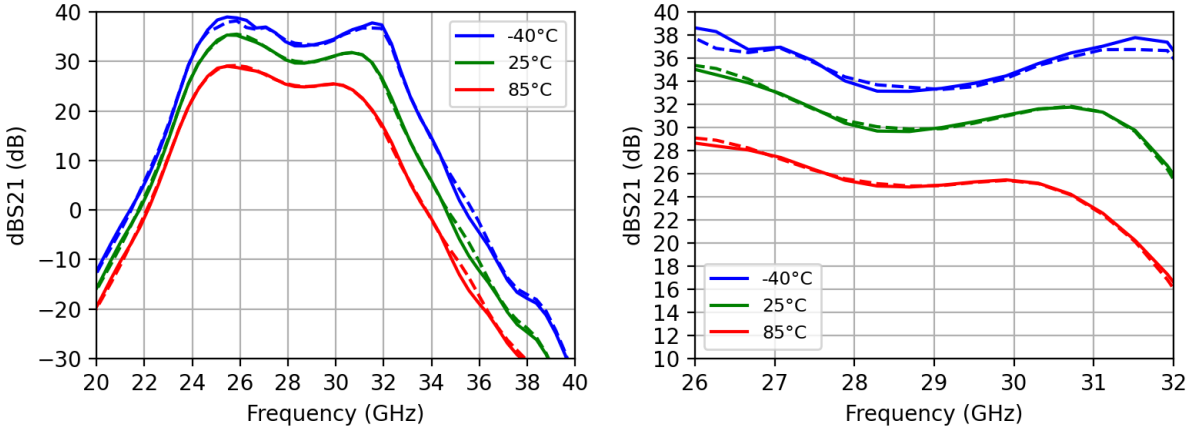
Typical Board Measurements : S-Parameters

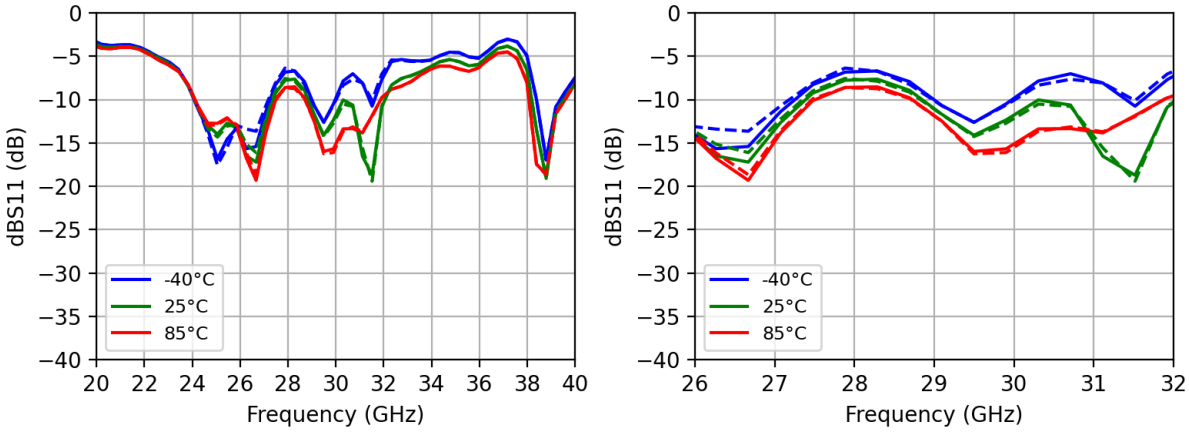
Test conditions : CW, Vd = +25V, **Id = 260mA**, T_{case} = -40°C / 25°C / 85°C

Linear Gain versus Frequency



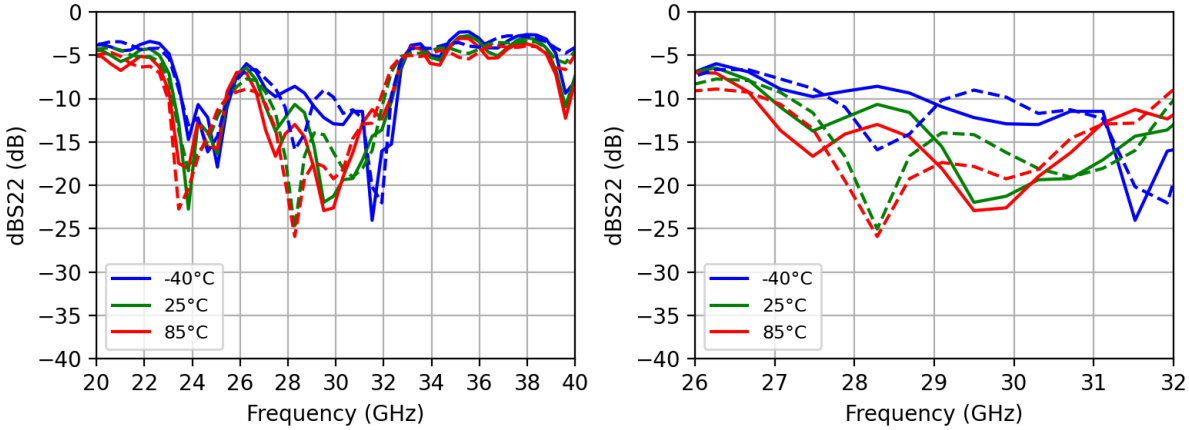
Line : North Path / Dot : South Path

Input Return Loss versus Frequency



Line : North Path / Dot : South Path

Output Return Loss versus Frequency



Line : North Path / Dot : South Path

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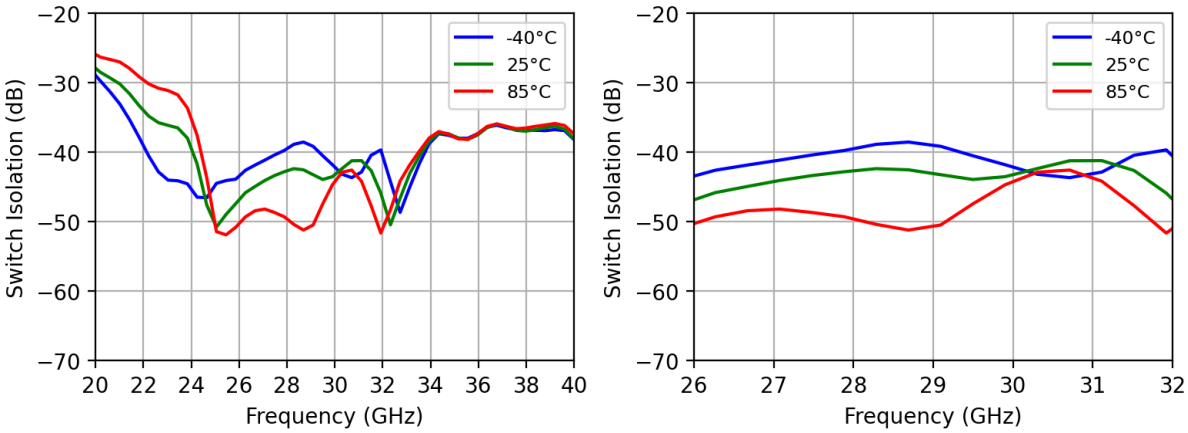
Typical Board Measurements : S-Parameters

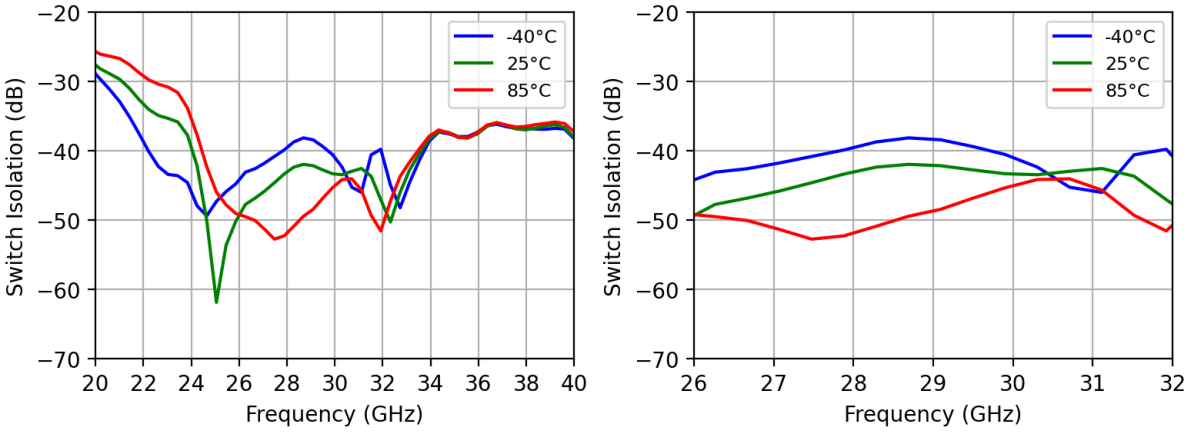
Test conditions : CW, Vd = +25V, **Id = 120mA**, T_{case} = -40°C / 25°C / 85°C

Switch isolation versus Frequency



Test conditions : CW, Vd = +25 V, **Id = 260 mA**, T_{case} = -40 °C / 25 °C / 85 °C

Switch isolation versus Frequency



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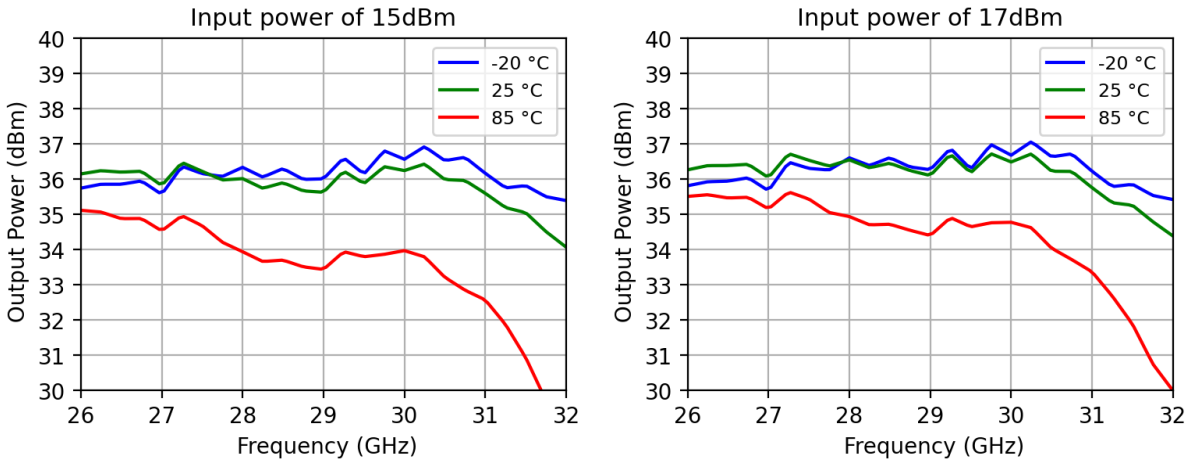
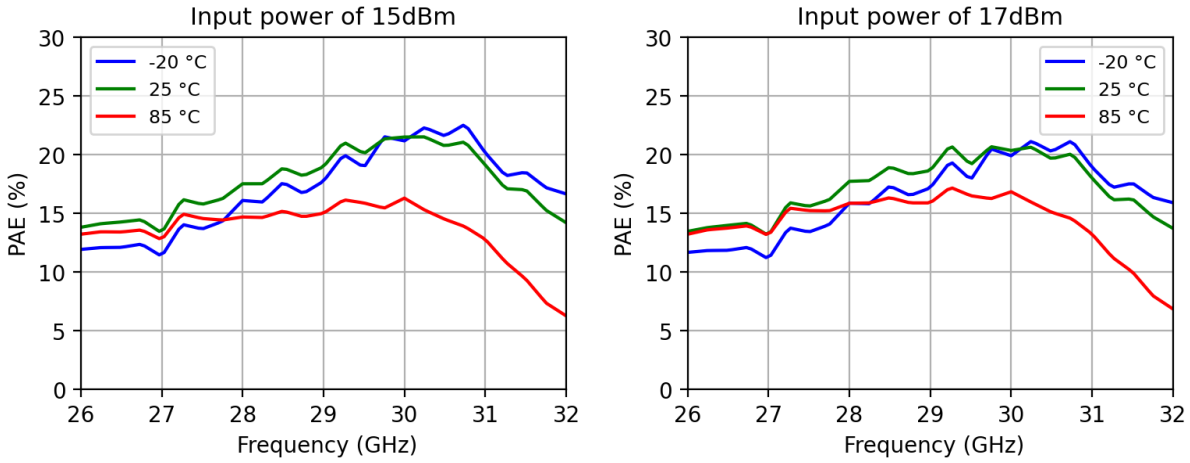
Typical Board Measurements : Large Signal

Test conditions : CW, Vd = +25V, **Id = 120mA**, T_{case} = -20°C / 25°C / 85°C, North Path

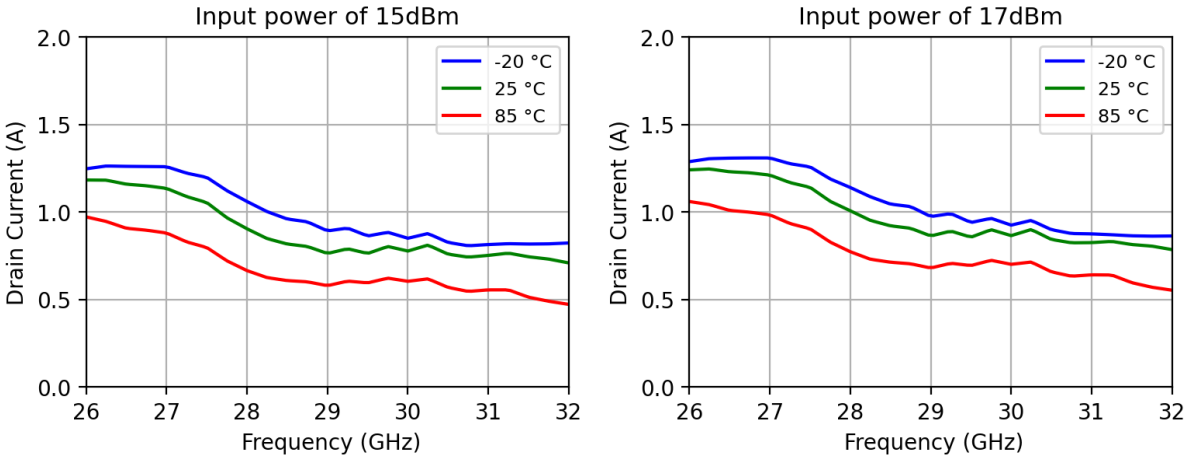
Output Power versus Frequency



PAE versus Frequency



Drain Current versus Frequency



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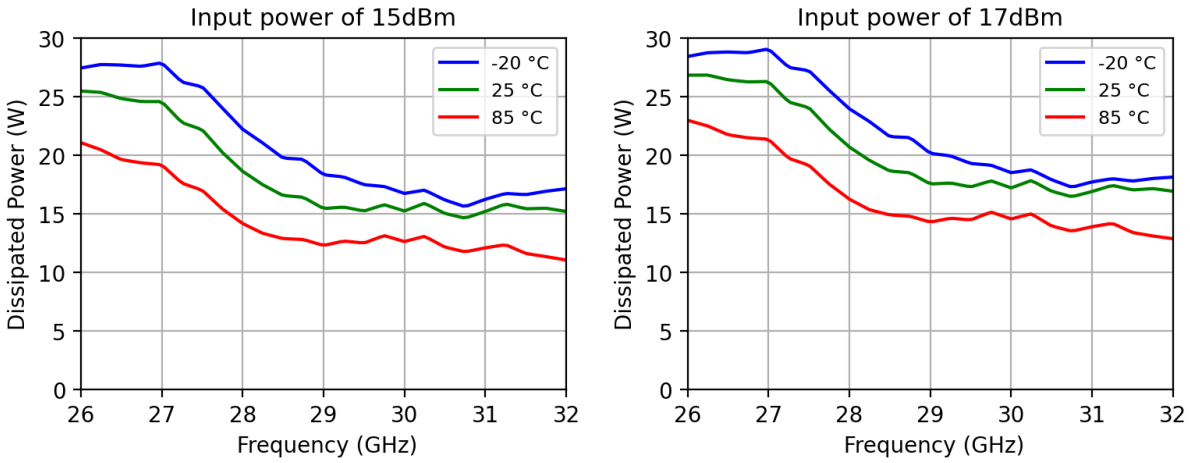
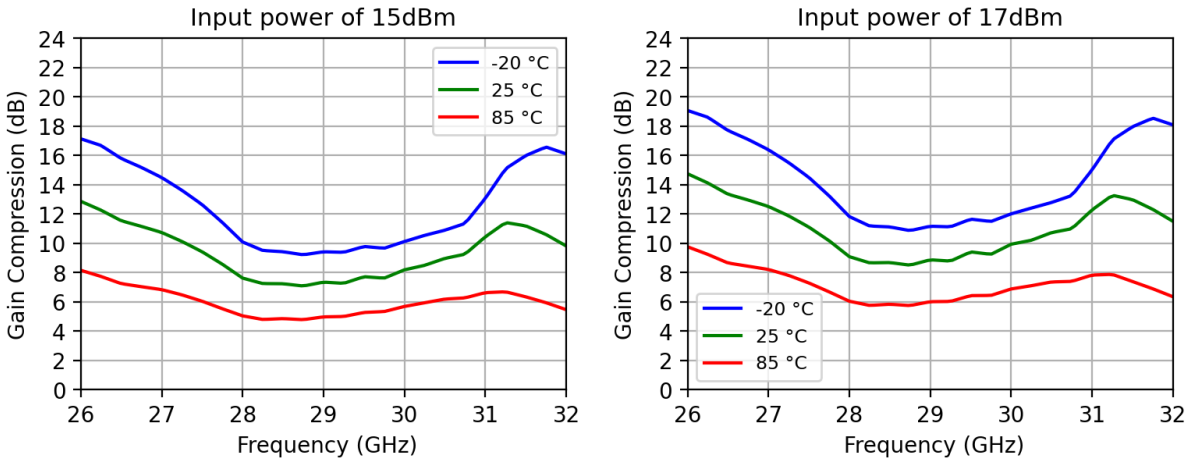
Typical Board Measurements : Large Signal

Test conditions : CW, Vd = +25V, **Id = 120mA**, T_{case} = -20°C / 25°C / 85°C, North Path

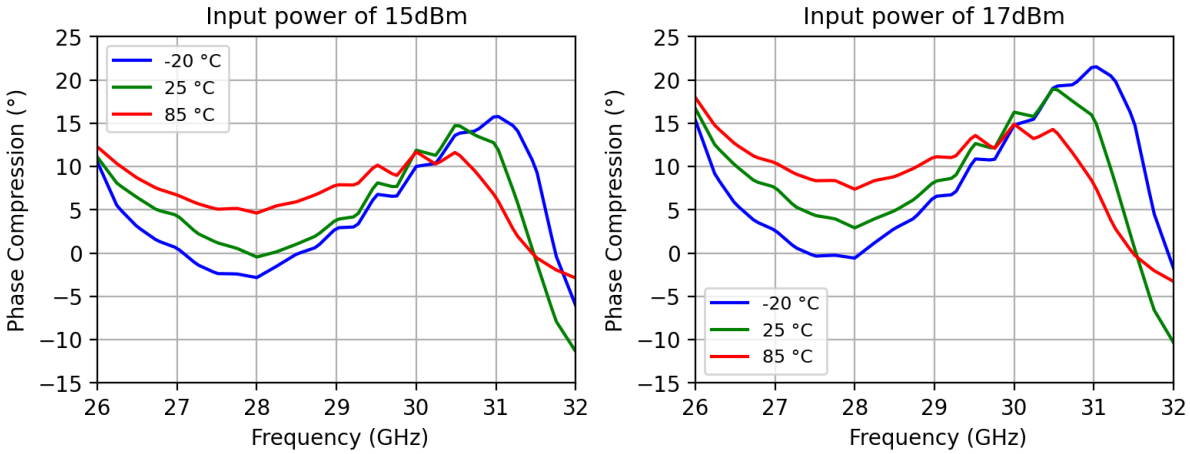
Dissipated Power versus Frequency



Gain Compression versus Frequency



Phase Compression versus Frequency



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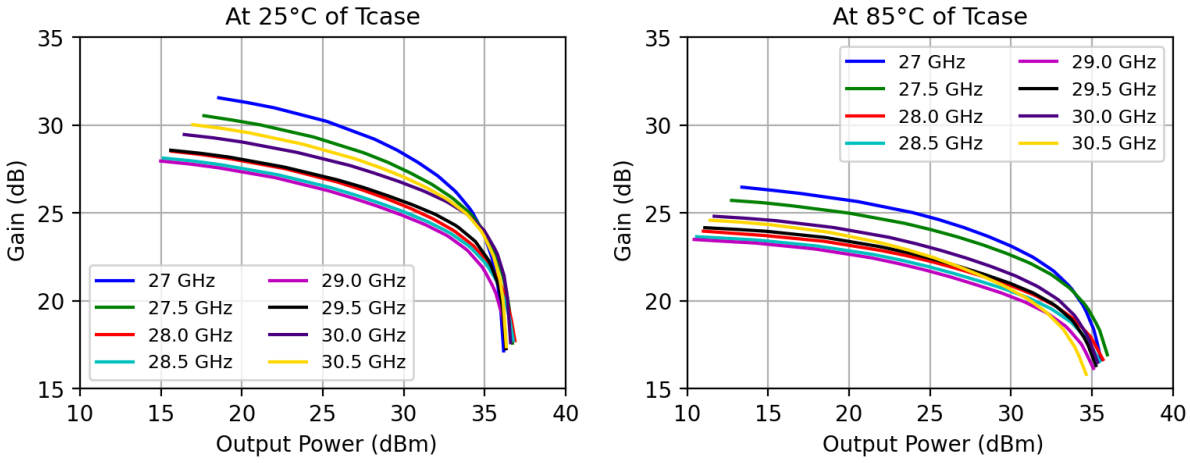
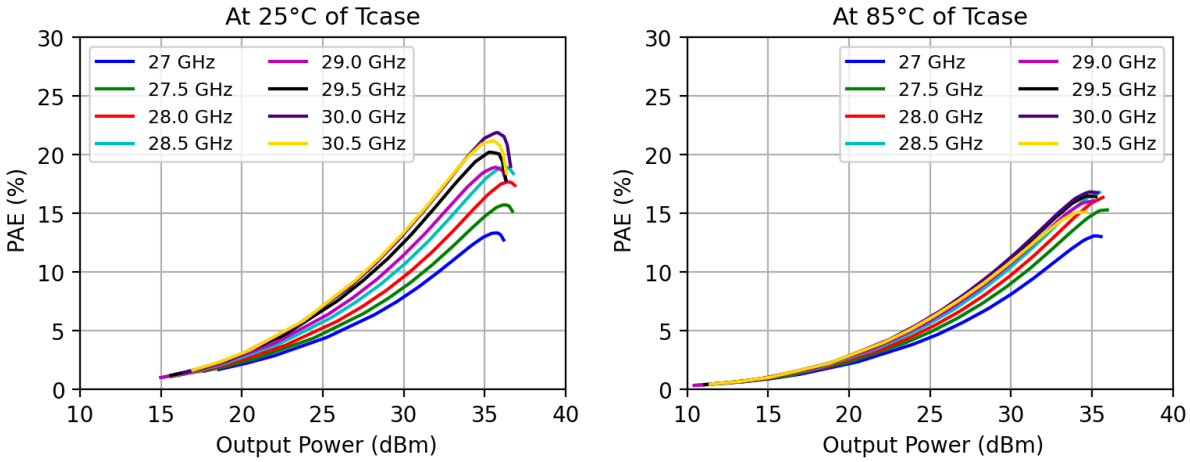
Typical Board Measurements : Large Signal

Test conditions : CW, Vd = +25V, **Id = 120mA**, T_{case} = 25°C / 85°C, North Path

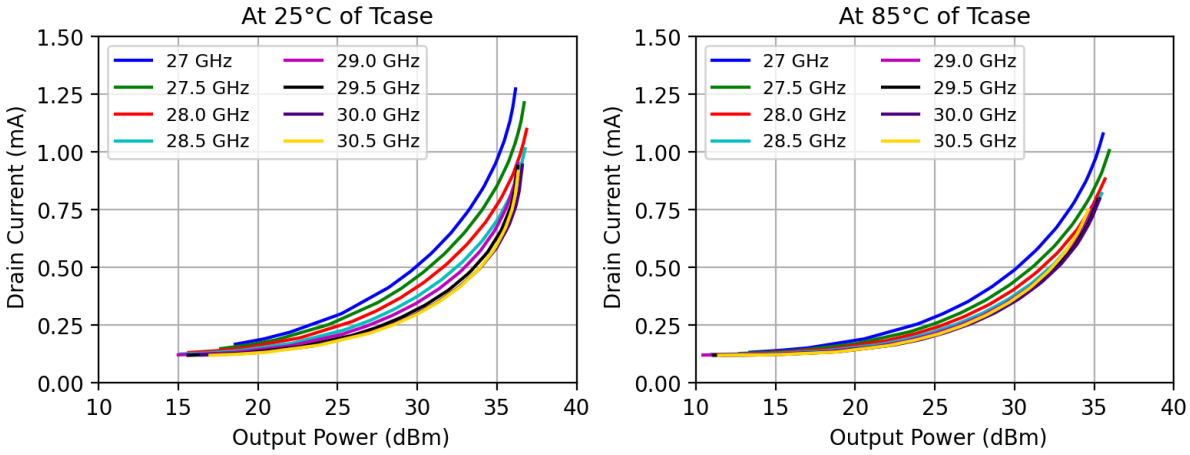
Gain versus Output Power



PAE versus Output Power



Drain Current versus Output Power



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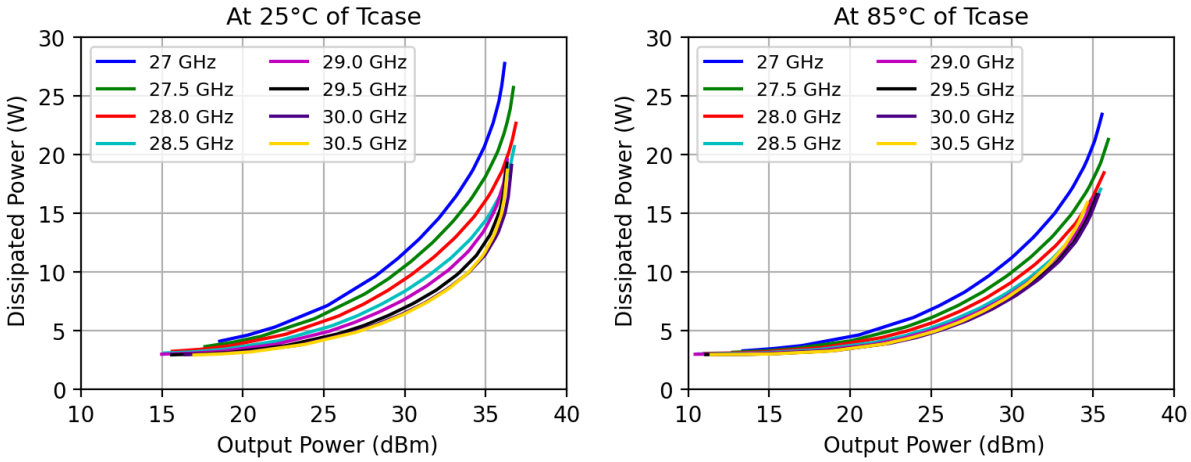
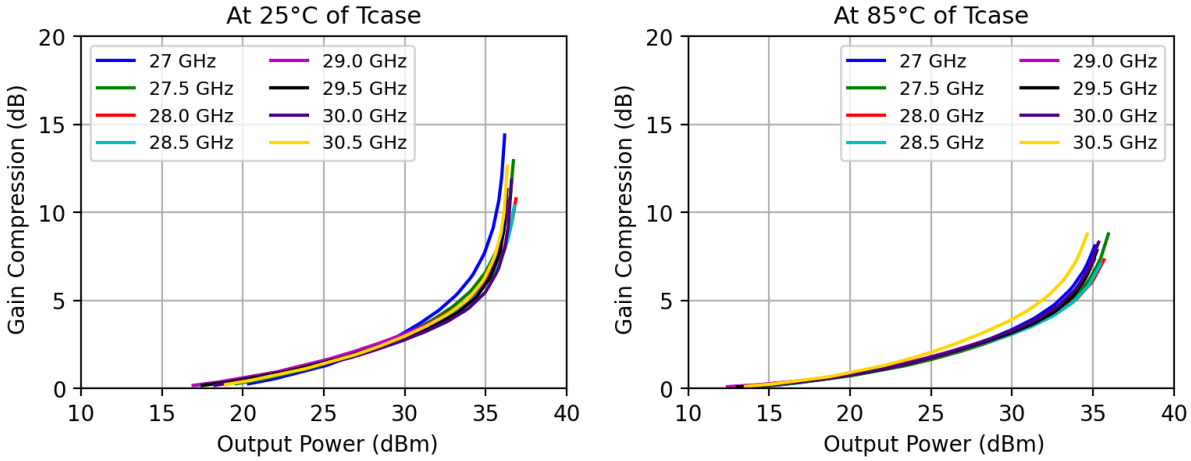
Typical Board Measurements : Large Signal

Test conditions : CW, Vd = +25V, **Id = 120mA**, T_{case} = 25°C / 85°C, North Path

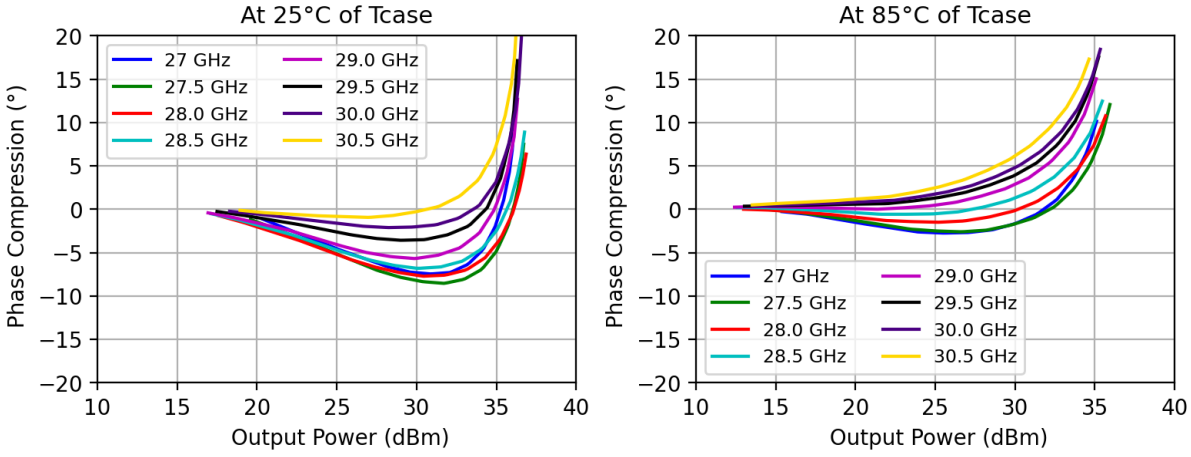
Dissipated Power versus Output Power



Gain Compression versus Output Power



Phase Compression versus Output Power



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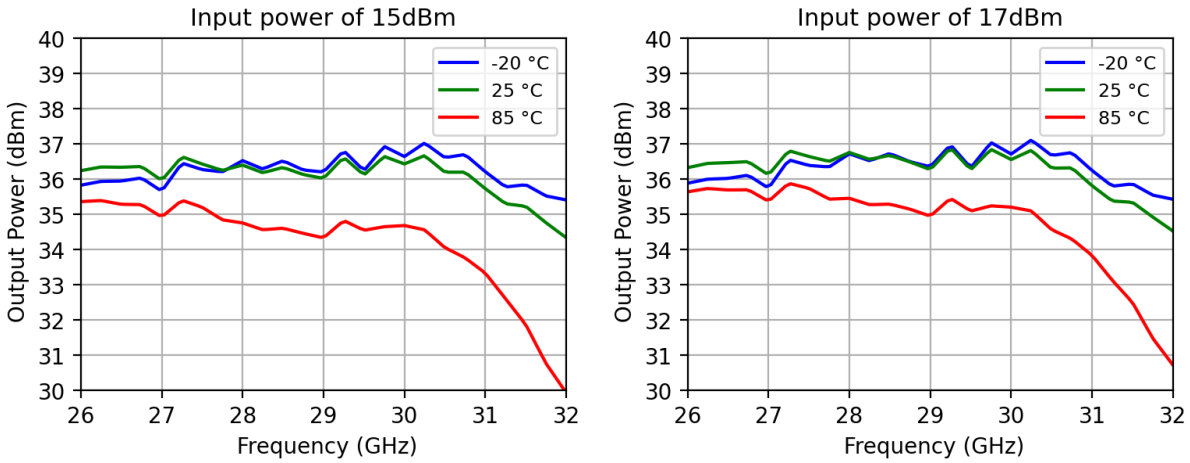
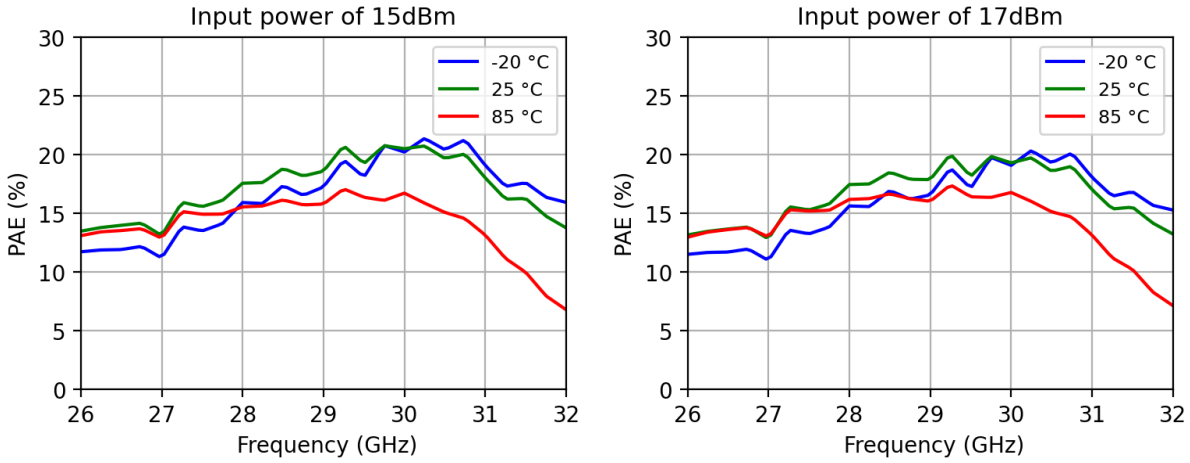
Typical Board Measurements : Large Signal

Test conditions : CW, Vd = +25V, **Id = 260mA**, T_{case} = -20°C / 25°C / 85°C, North Path

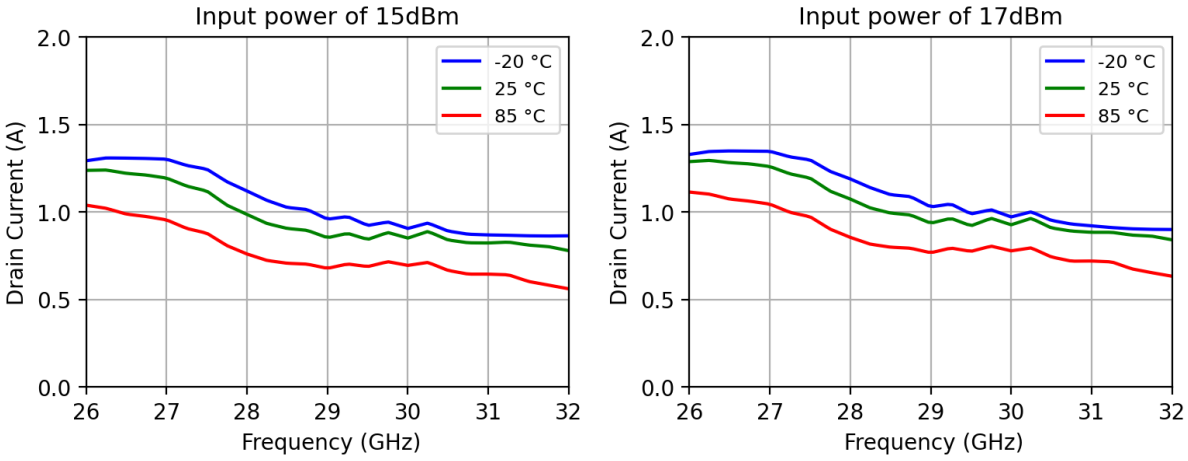
Output Power versus Frequency



PAE versus Frequency



Drain Current versus Frequency



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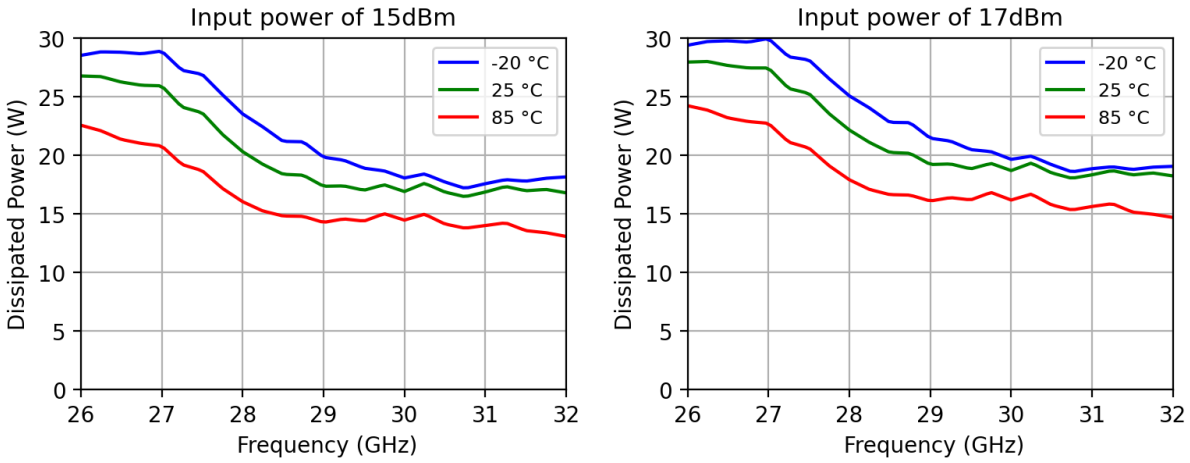
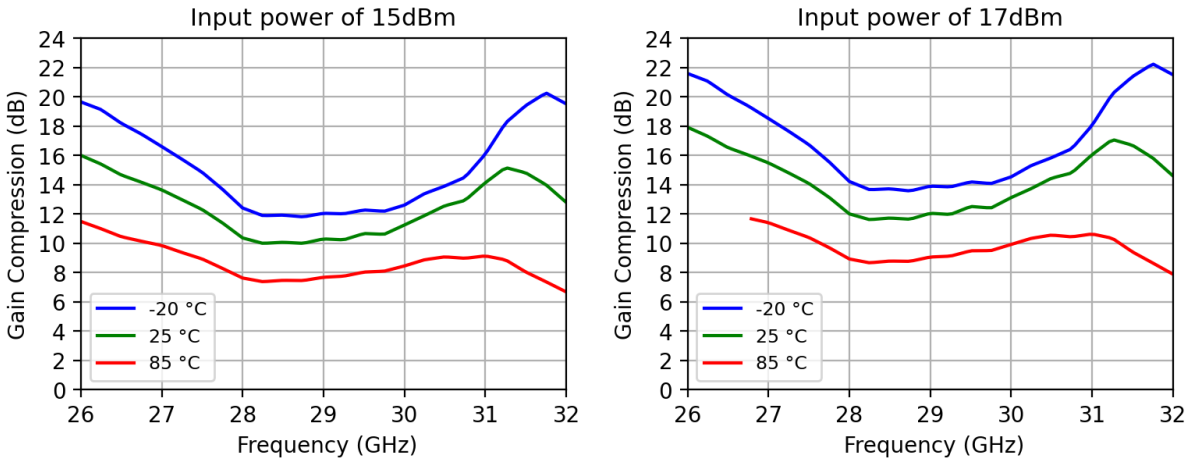
Typical Board Measurements : Large Signal

Test conditions : CW, Vd = +25V, **Id = 260mA**, T_{case} = -20°C / 25°C / 85°C, North Path

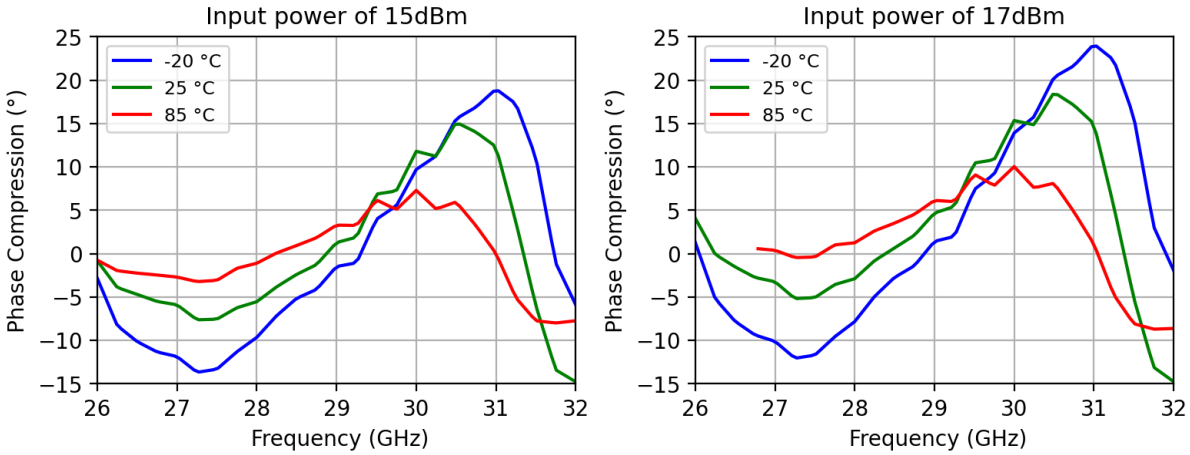
Dissipated Power versus Frequency



Gain Compression versus Frequency



Phase Compression versus Frequency



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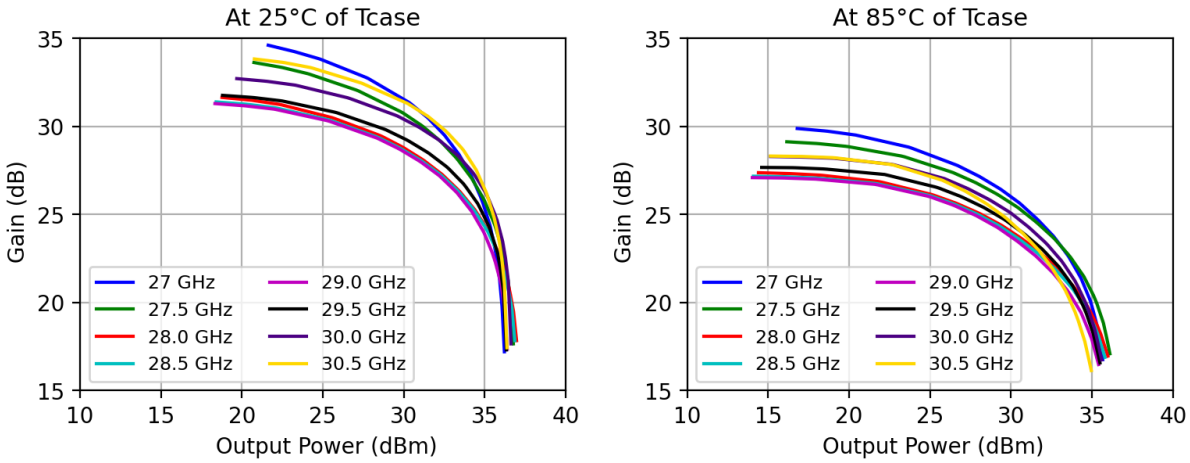
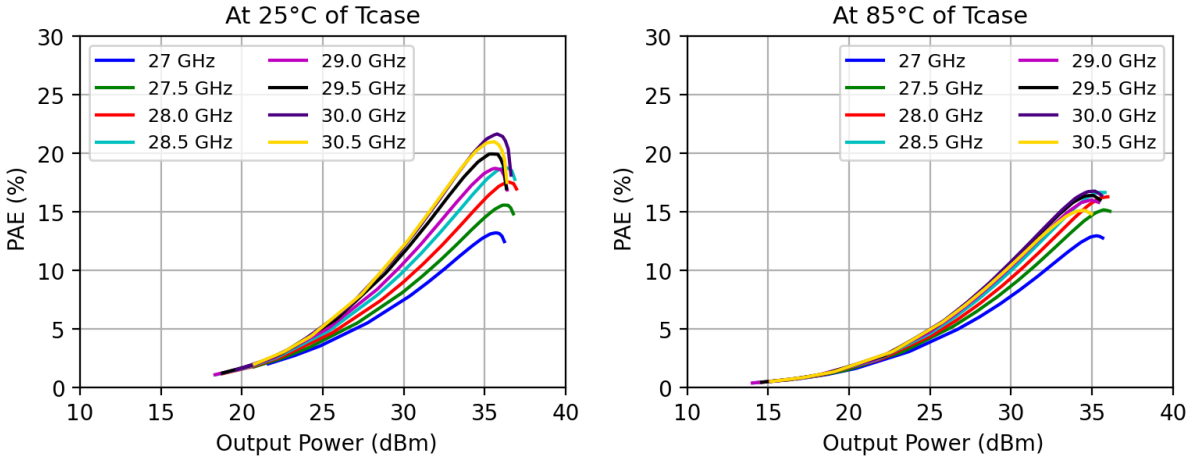
Typical Board Measurements : Large Signal

Test conditions : CW, Vd = +25V, **Id = 260mA**, T_{case} = 25°C / 85°C, North Path

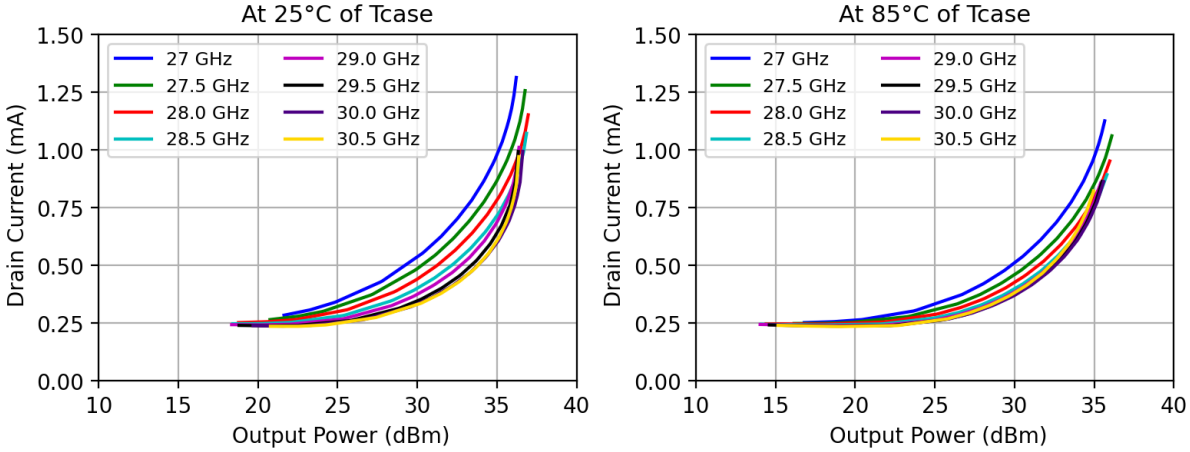
Gain versus Output Power



PAE versus Output Power



Drain Current versus Output Power



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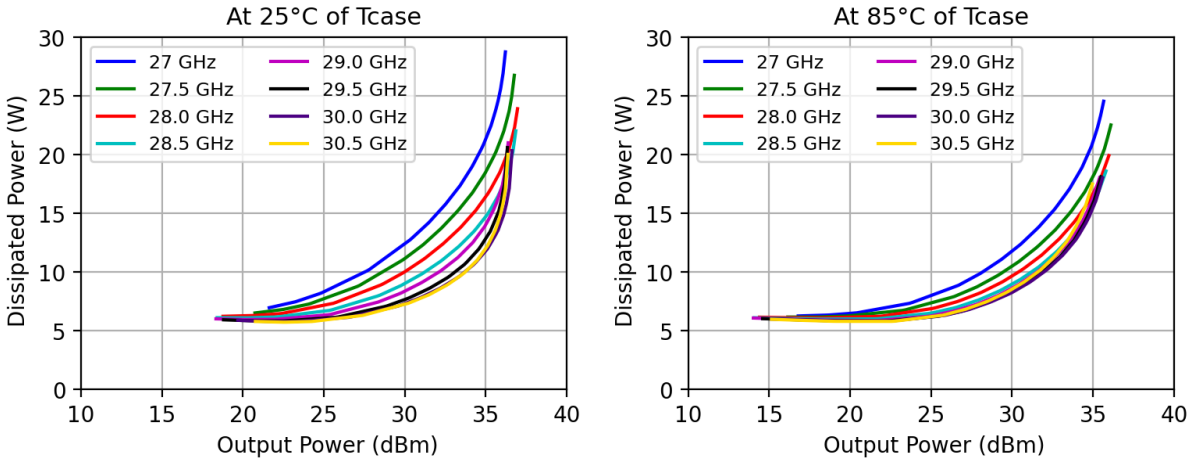
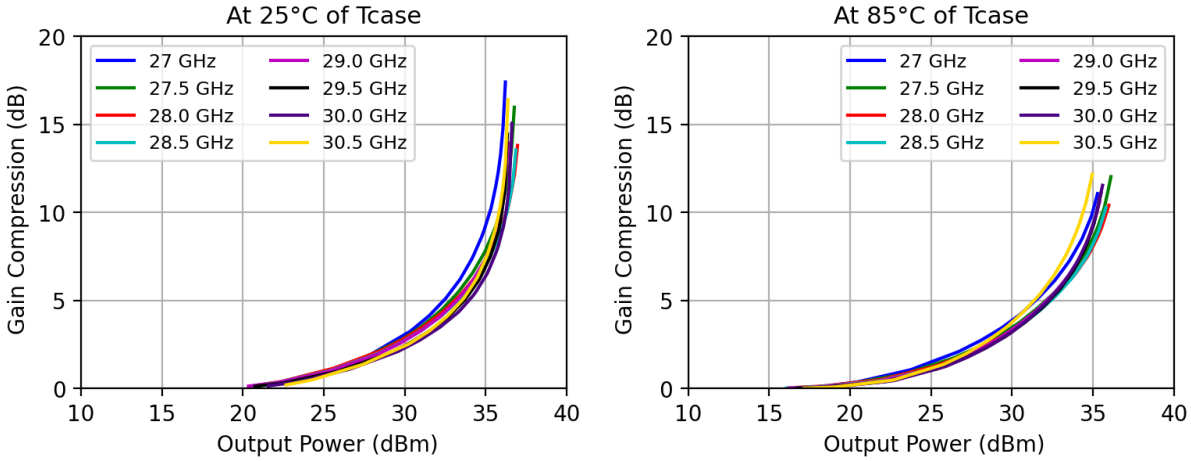
Typical Board Measurements : Large Signal

Test conditions : CW, Vd = +25V, **Id = 260mA**, T_{case} = 25°C / 85°C, North Path

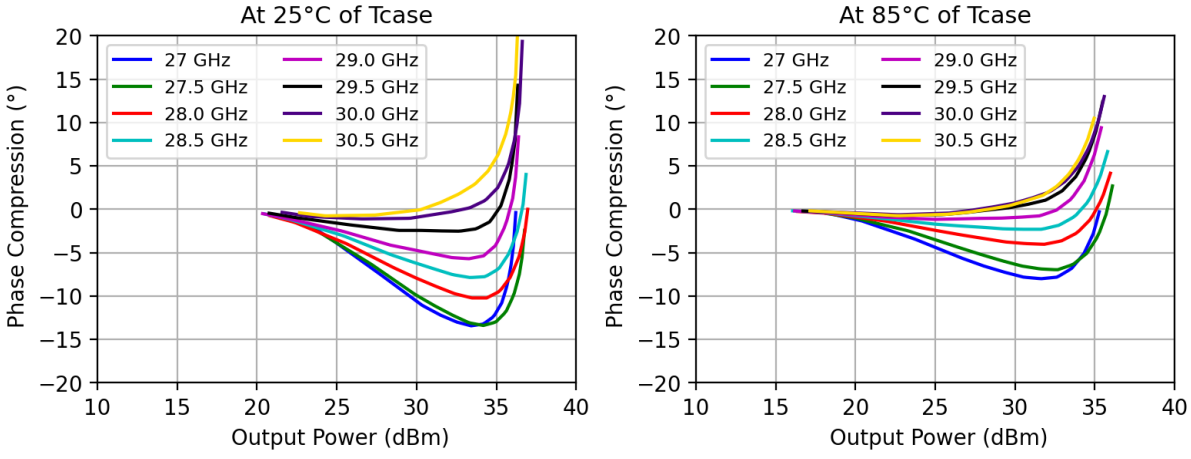
Dissipated Power versus Output Power



Gain Compression versus Output Power



Phase Compression versus Output Power



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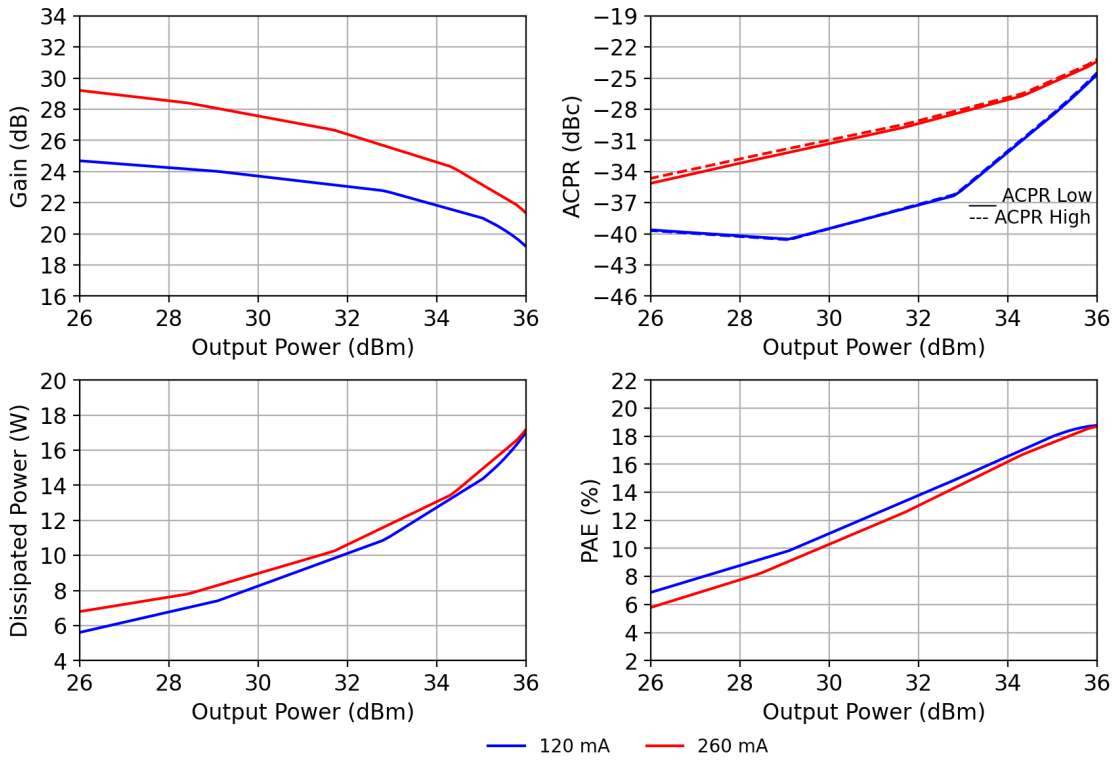
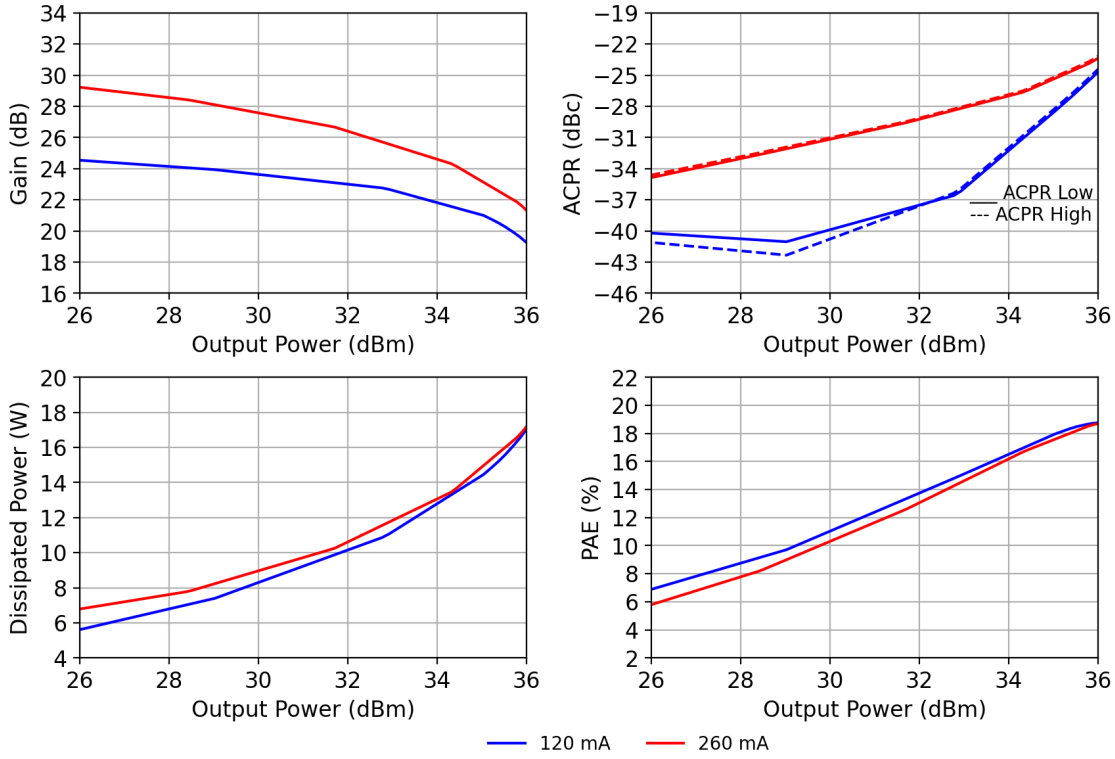
Typical Board Measurements : Linearity

Test conditions : 8PSK / BW = 15MHz / Roll off = 0.2 / **Fc=28.75GHz**
Vd = +25V, Id = 120mA and 260mA, **Tcase = 25°C**



Test conditions : 8PSK / BW = 30 MHz / Roll off = 0.2 / **Fc=28.75GHz**
Vd = +25V, Id = 120mA and 260mA, **Tcase = 25°C**



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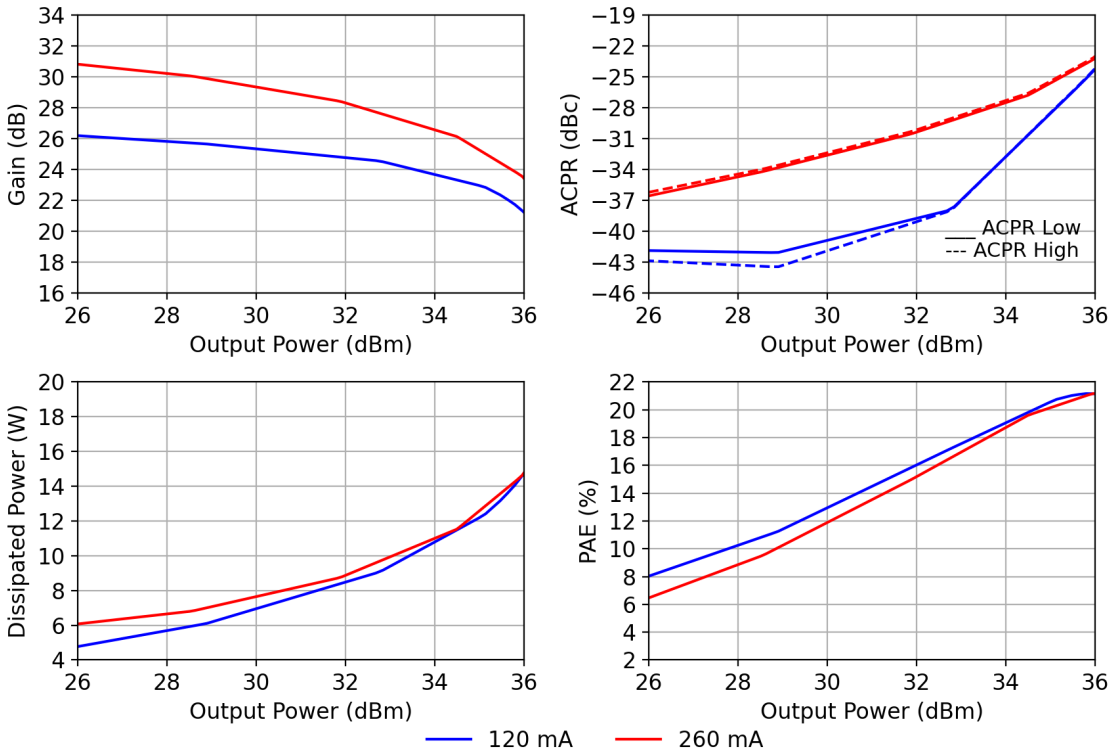
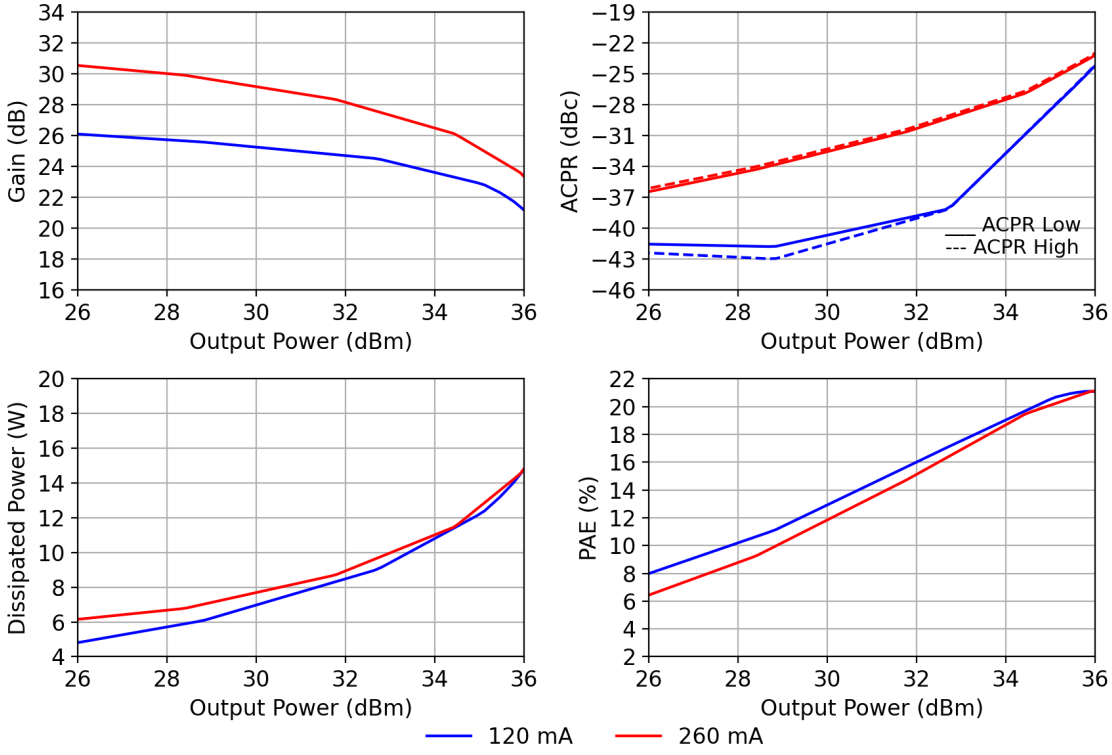
Typical Board Measurements : Linearity

Test conditions : 8PSK / BW = 15MHz / Roll off = 0.2 / **Fc=29.75GHz**
Vd = +25V, Id = 120mA and 260mA, **Tcase = 25°C**



Test conditions : 8PSK / BW = 30MHz / Roll off = 0.2 / **Fc=29.75GHz**
Vd = +25V, Id = 120mA and 260mA, **Tcase = 25°C**



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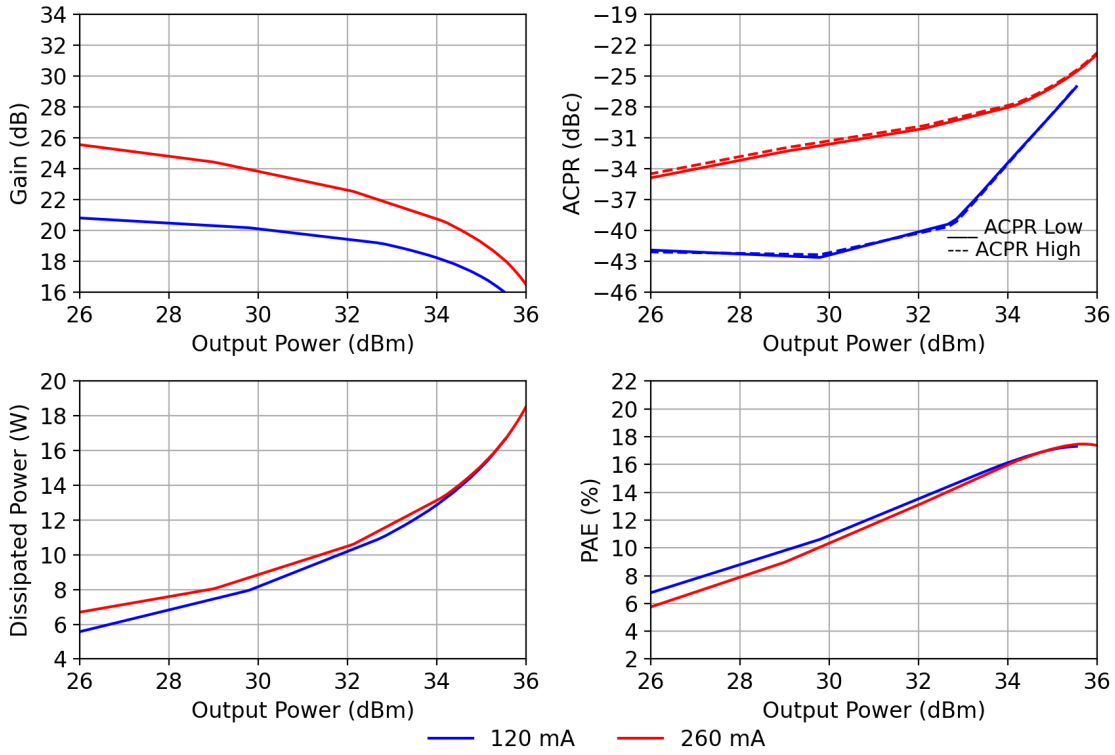
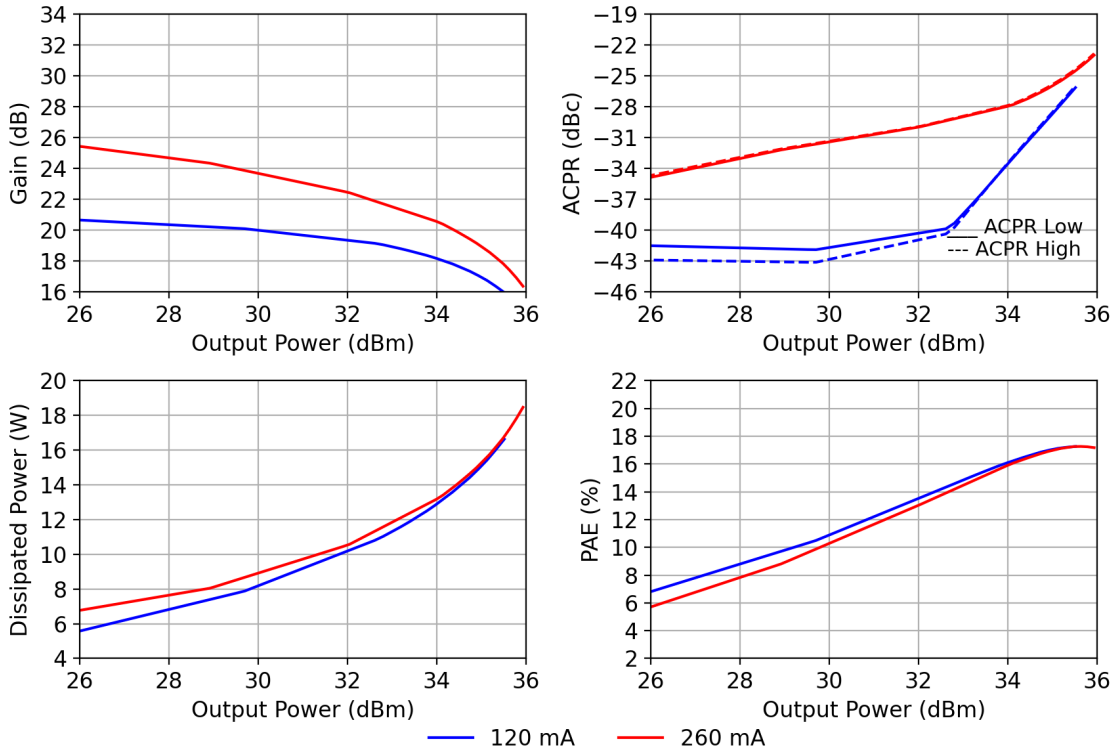
Typical Board Measurements : Linearity

Test conditions : 8PSK / 15MHz / Roll off = 0.2 / **Fc=28.75GHz**
Vd = +25V, Id = 120mA and 260mA, **Tcase = 85°C**



Test conditions : 8PSK / BW = 30MHz / Roll off = 0.2 / **Fc=28.75GHz**
Vd = +25V, Id = 120mA and 260mA, **Tcase = 85°C**



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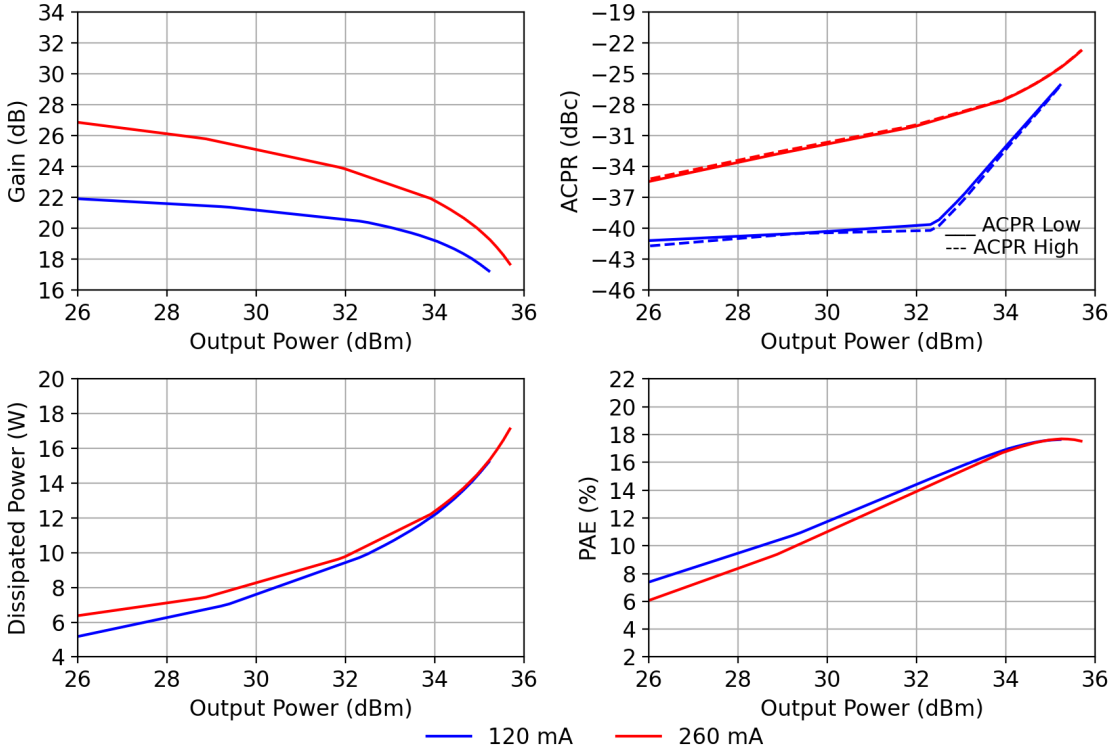
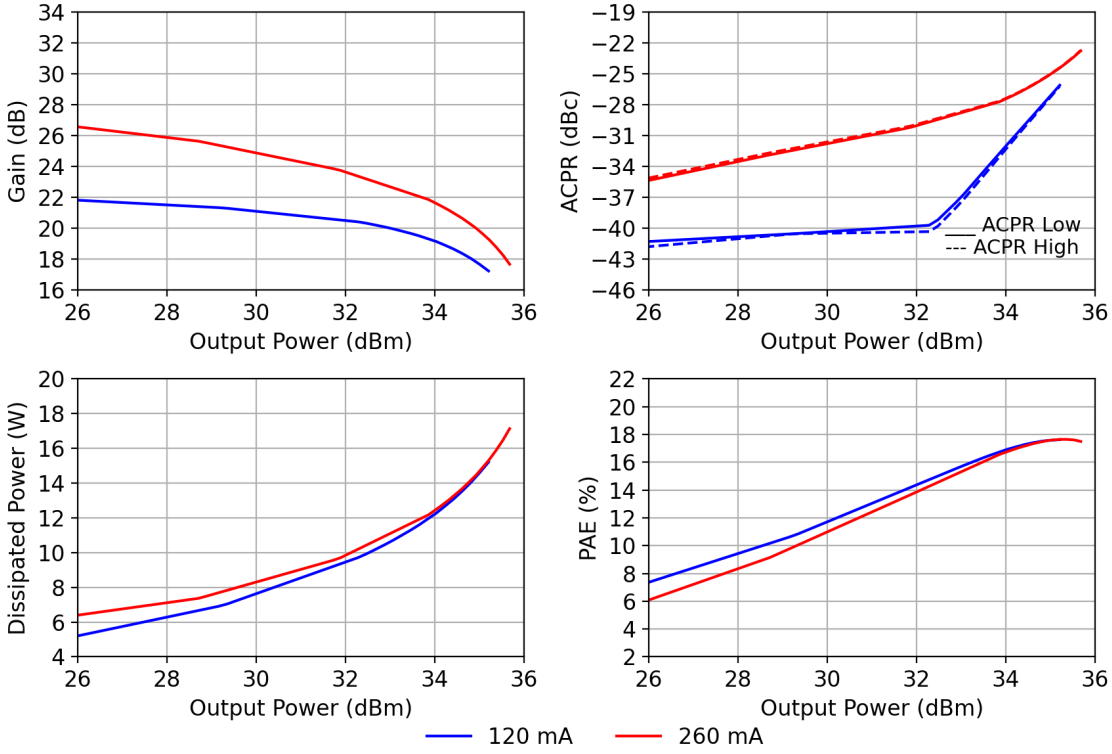
Typical Board Measurements : Linearity

Test conditions : 8PSK / BW = 15MHz / Roll off = 0.2 / **Fc=29.75GHz**
Vd = +25V, Id = 120mA and 260mA, **Tcase = 85°C**



Test conditions : 8PSK / BW = 30MHz / Roll off = 0.2 / **Fc=29.75GHz**
Vd = +25V, Id = 120mA and 260mA, **Tcase = 85°C**



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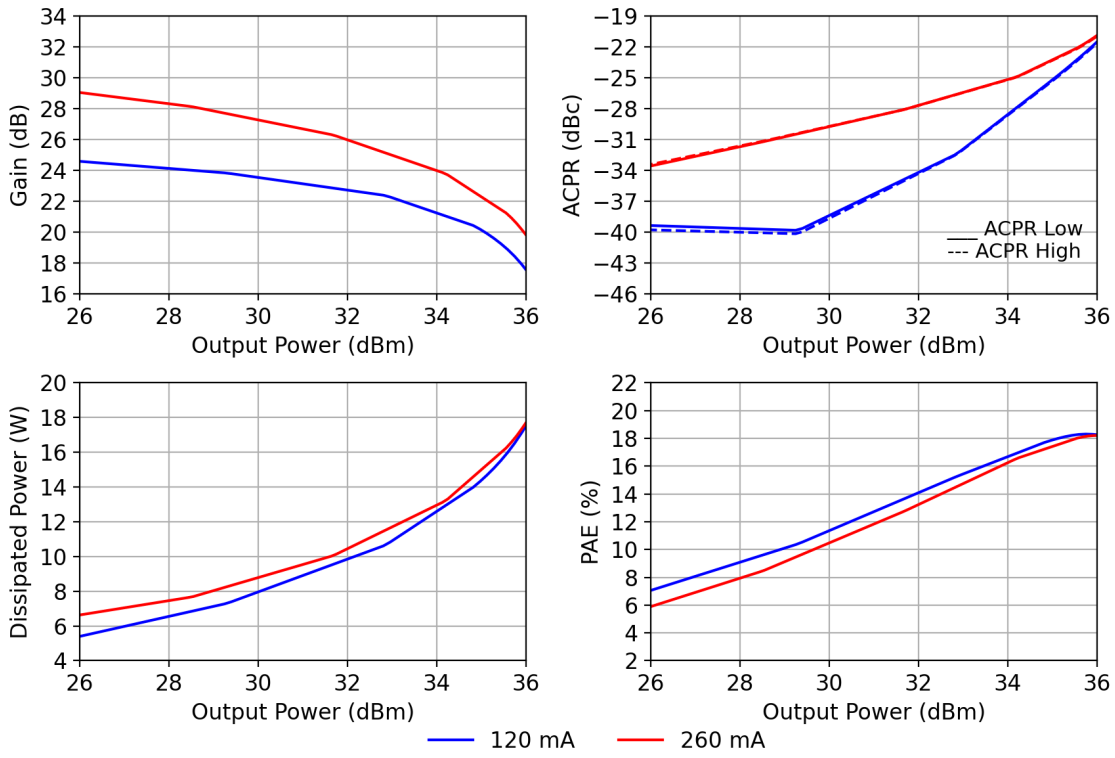
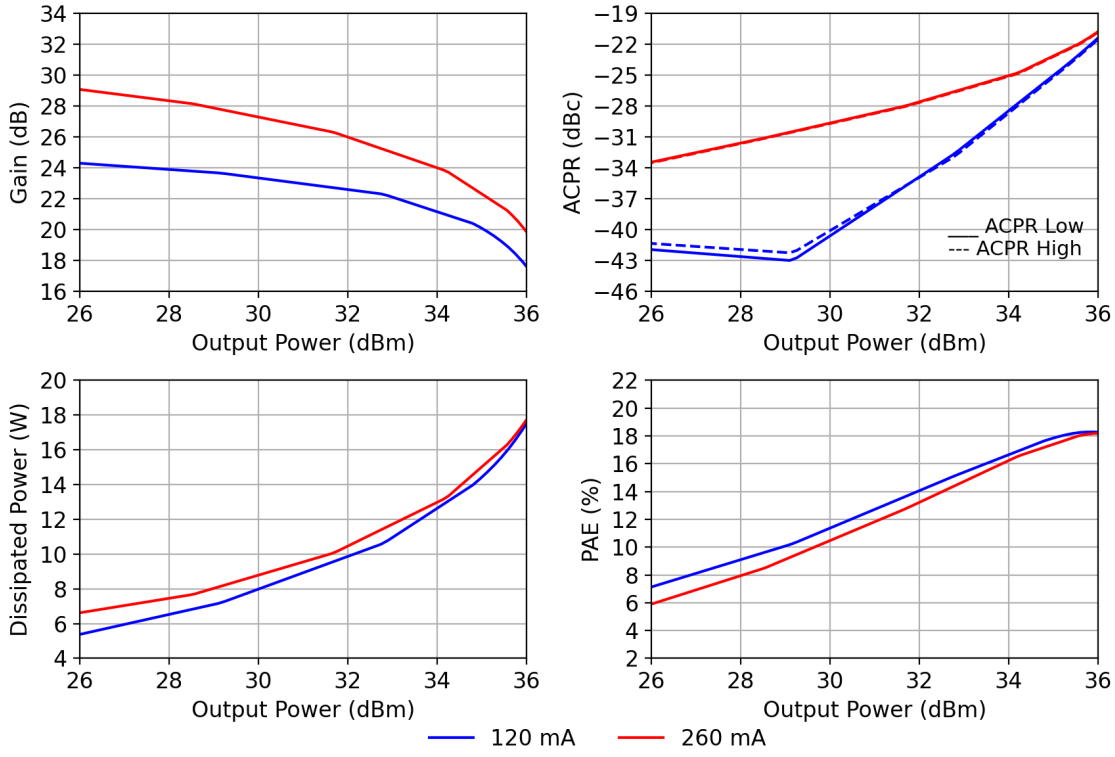
Typical Board Measurements : Linearity

Test conditions : 16QAM / BW = 15MHz / Roll off = 0.2 / **Fc=28.75GHz**
Vd = +25V, Id = 120mA and 260mA, **Tcase = 25°C**



Test conditions : 16QAM / BW = 1.9MHz / Roll off = 0.2 / Fc=28.75GHz,
Vd = +25V, Id = 120mA and 260mA, **Tcase = 25°C**



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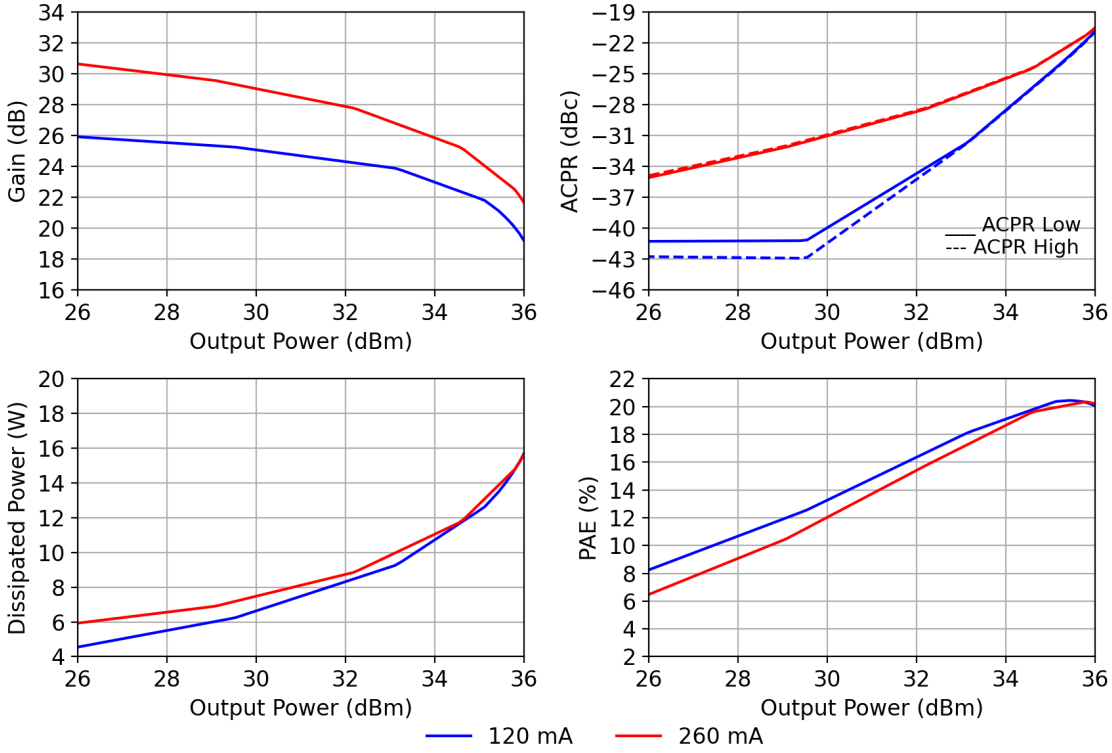
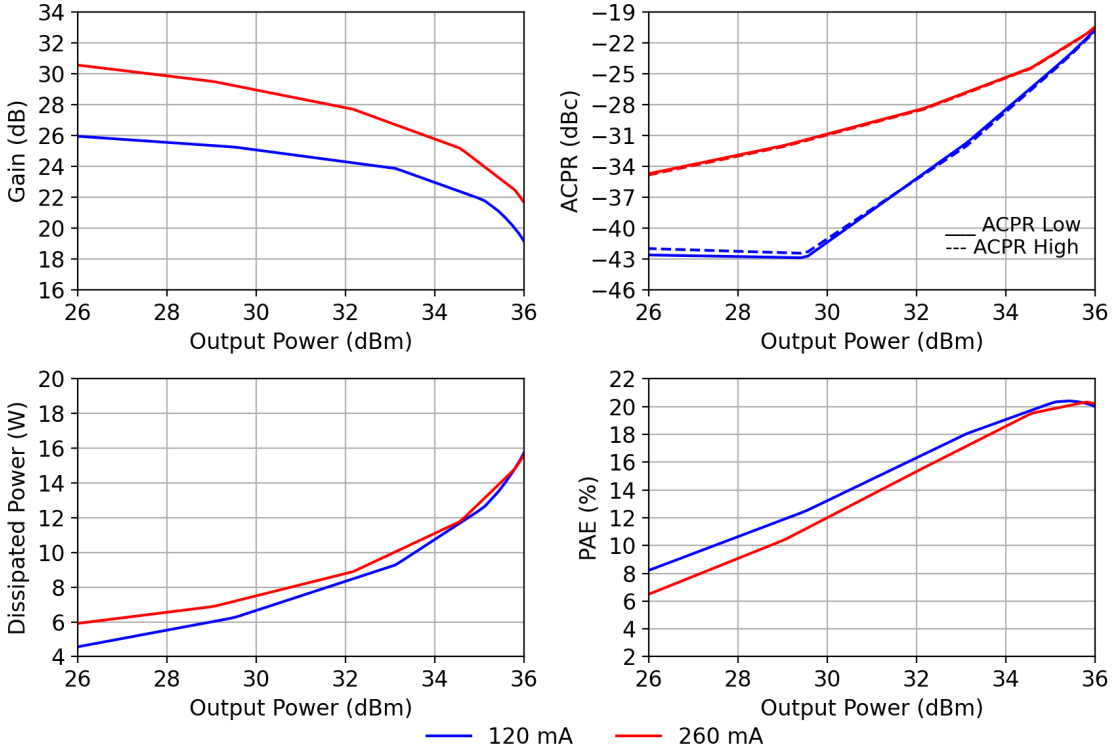
Typical Board Measurements : Linearity

Test conditions : 16QAM / BW = 15MHz / Roll off = 0.2 / **Fc=29.75GHz**
Vd = +25V, Id = 120mA and 260mA, **Tcase = 25°C**



Test conditions : 16QAM / BW = 1.9MHz / Roll off = 0.2 / **Fc=29.75GHz**
Vd = +25V, Id = 120mA and 260mA, **Tcase = 25°C**



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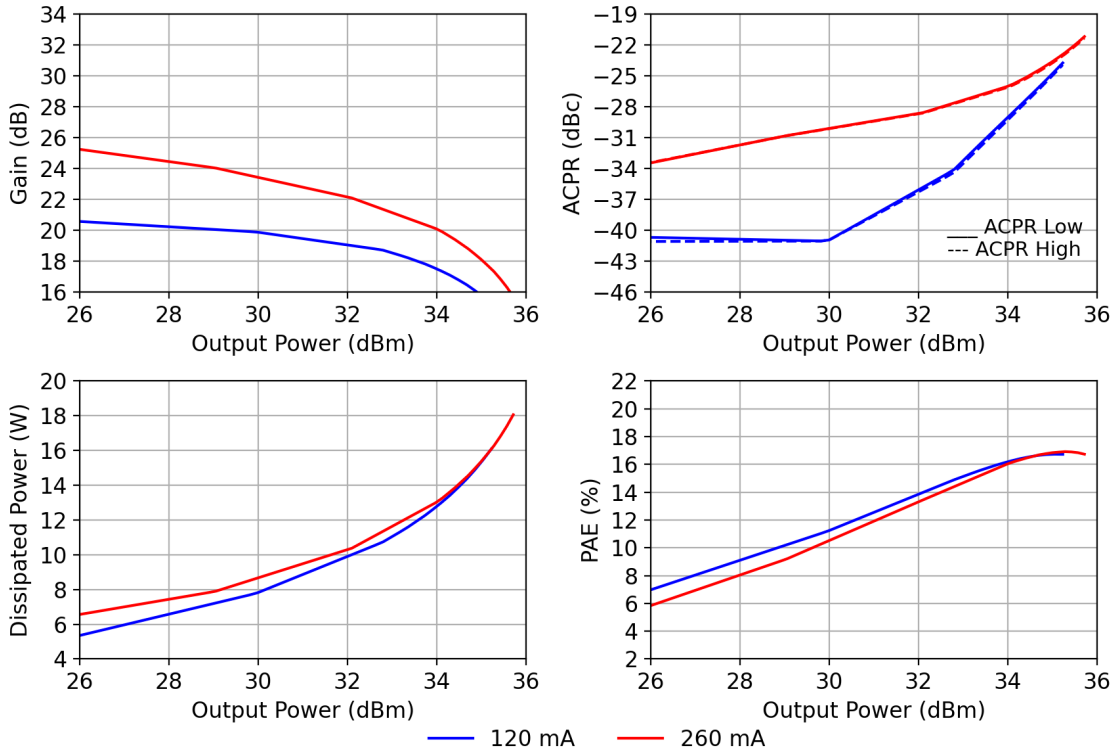
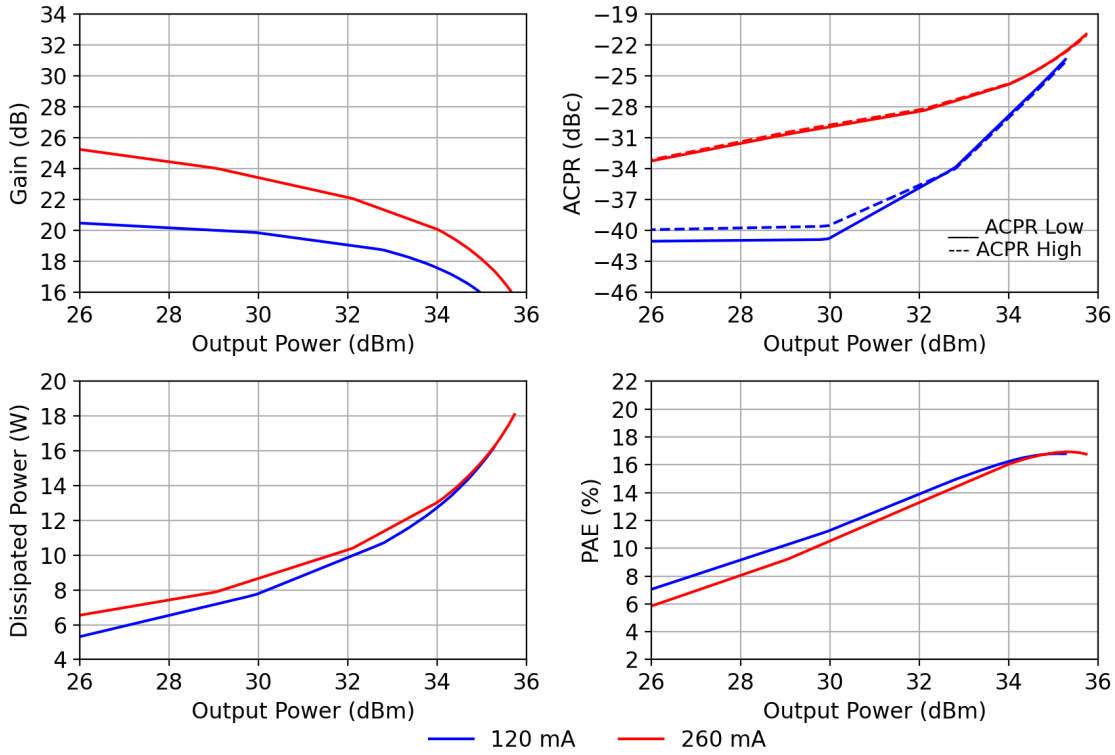
Typical Board Measurements : Linearity

Test conditions : 16QAM / BW = 15MHz / Roll off = 0.2 / **Fc=28.75GHz**
Vd = +25V, Id = 120mA and 260mA, **Tcase = 85°C**



Test conditions : 16QAM / BW = 1.9MHz / Roll off = 0.2 / **Fc=28.75GHz**
Vd = +25V, Id = 120mA and 260mA, **Tcase = 85°C**



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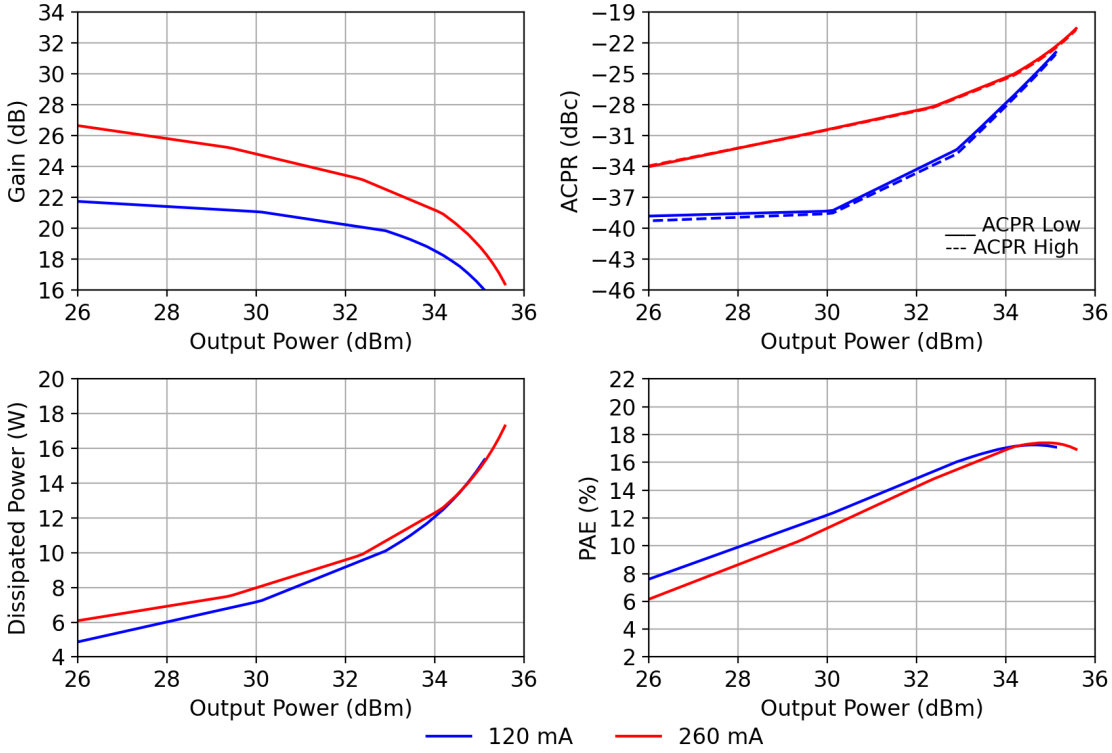
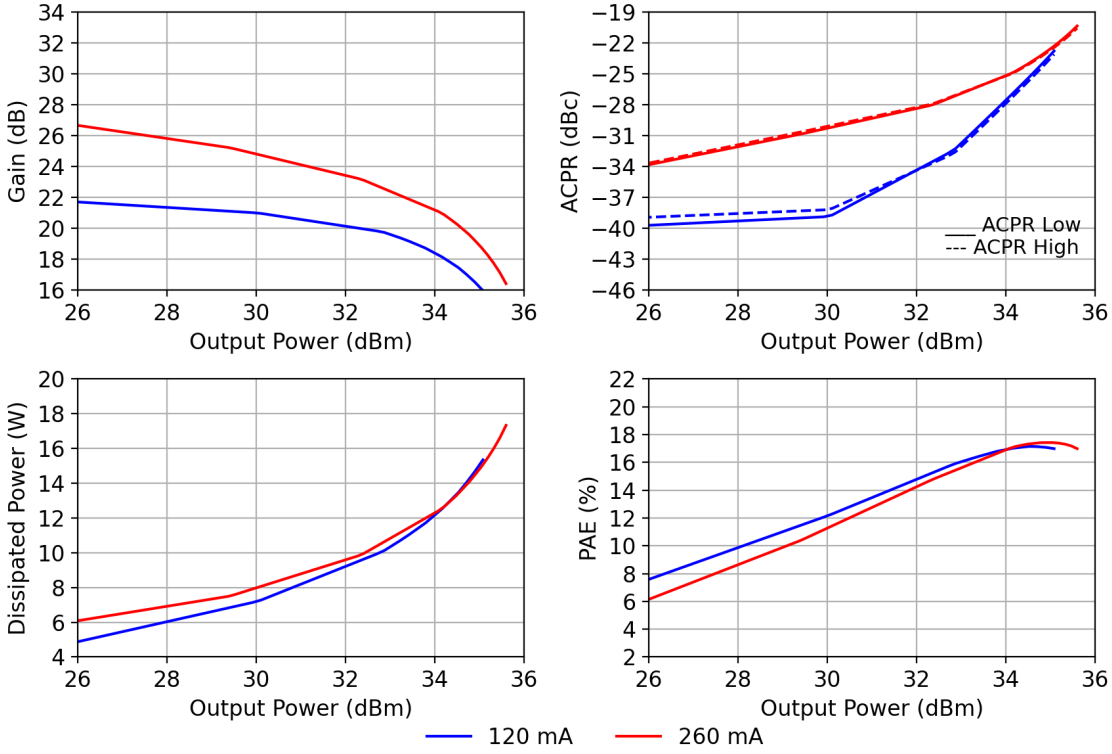
Typical Board Measurements : Linearity

Test conditions : 16QAM / BW = 15MHz / Roll off = 0.2 / **Fc=29.75GHz**
Vd = +25V, Id = 120mA and 260mA, **Tcase = 85°C**



Test conditions : 16QAM / BW = 1.9MHz / Roll off = 0.2 / **Fc=29.75GHz**
Vd = +25V, Id = 120mA and 260mA, **Tcase = 85°C**



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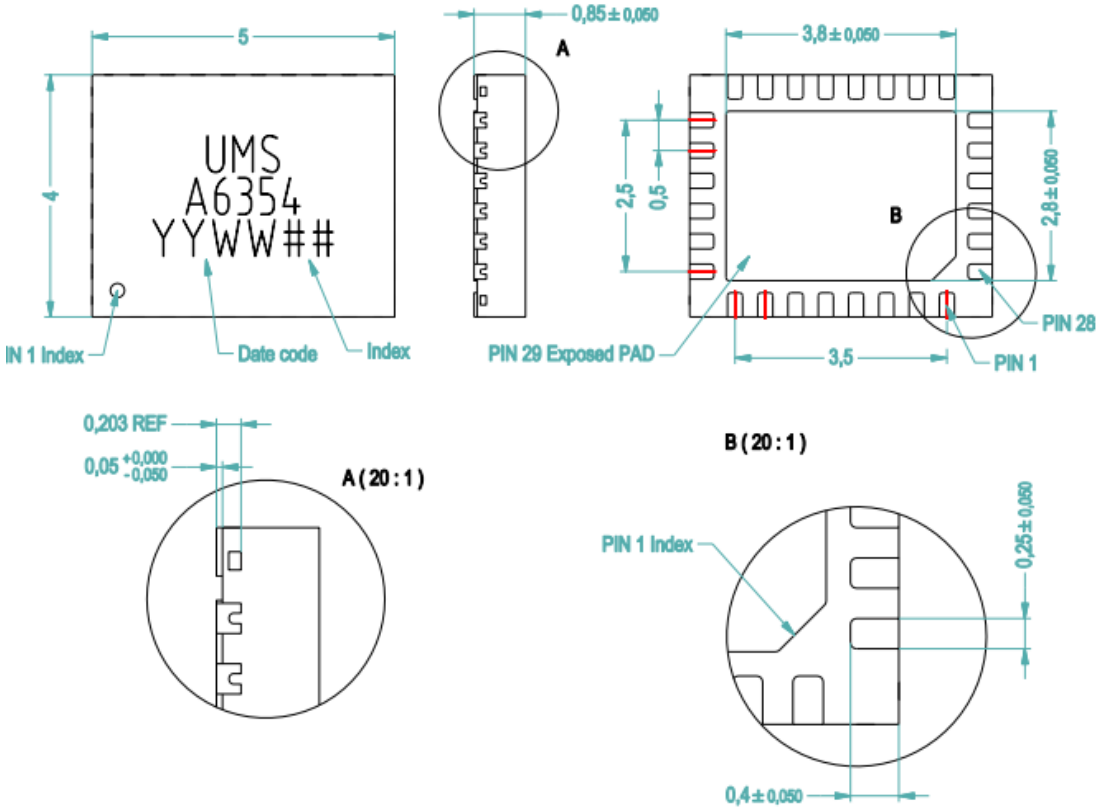
Package outline (1)



Matte tin, Lead Free	(Green)	1- G1	11- GND(2)	21- G3N
Units :	mm	2- G2S	12- GND(2)	22- D2N
From the standard :	JEDEC MO-220	3- D2S	13- OUT1	23- NC
	(VGGD)	4- NC	14- GND(2)	24- D1
		5- G3S	15- SWN	25- NC
		6- D3S	16- NC	26- GND(2)
		7- GND(2)	17- NC	27- IN
		8- SWS	18- NC	28- GND(2)
		9- GND(2)	19- NC	29- GND(2)
		10- OUT2	20- D3N	

(1) Refer to the application note AN0017 (https://www.ums-rf.com) for general consideration and recommendations for Molded Plastic QFN/DFN packages.

(2) It is strongly recommended to ground all pins marked “GND” through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

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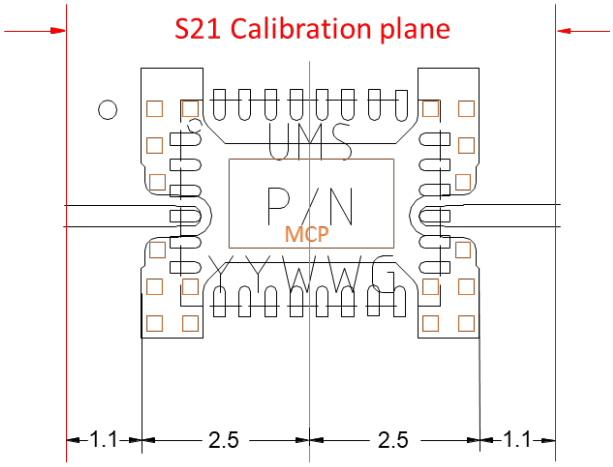
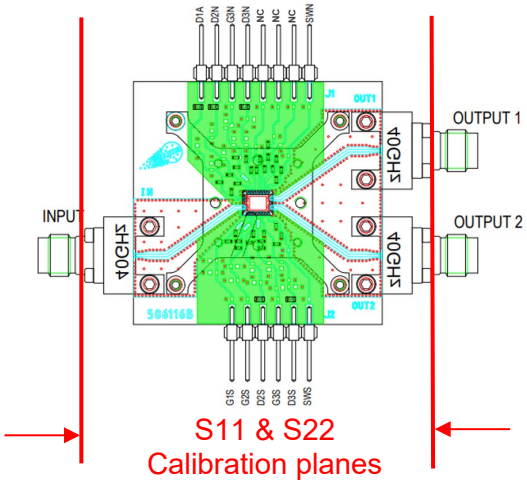
Definition of the Sij and power measurement reference planes

The reference planes used for S21 and power measurements are symmetrical from the central axis of the package (see drawing beside). The input and output reference planes are located at 3.6mm offset from the central axis. The S21 parameter measurements include this given PCB pattern (see paragraph "Evaluation board").



Definition of the Sii reference planes

The reference planes used for S11 and S22 measurements are symmetrical from the central axis of the package (see drawing beside). The input and output reference planes are located at 20mm offset from the central axis. The S11 and S22 measurements include this given PCB patter, the RF lines of the evaluation board and the RF connectors.



ESD sensitivity

Parameter	Classification	Standard
Human Body Model (HBM)	1A	ANSI/ESDA/JEDEC - JS-001

Package Information

Parameter	Value
Package body material	RoHS-compliant
	Low stress Injection Molded Plastic
Lead finish	100% Ni-Pd-Au-Ag
Moisture Sensitivity Level	MSL3

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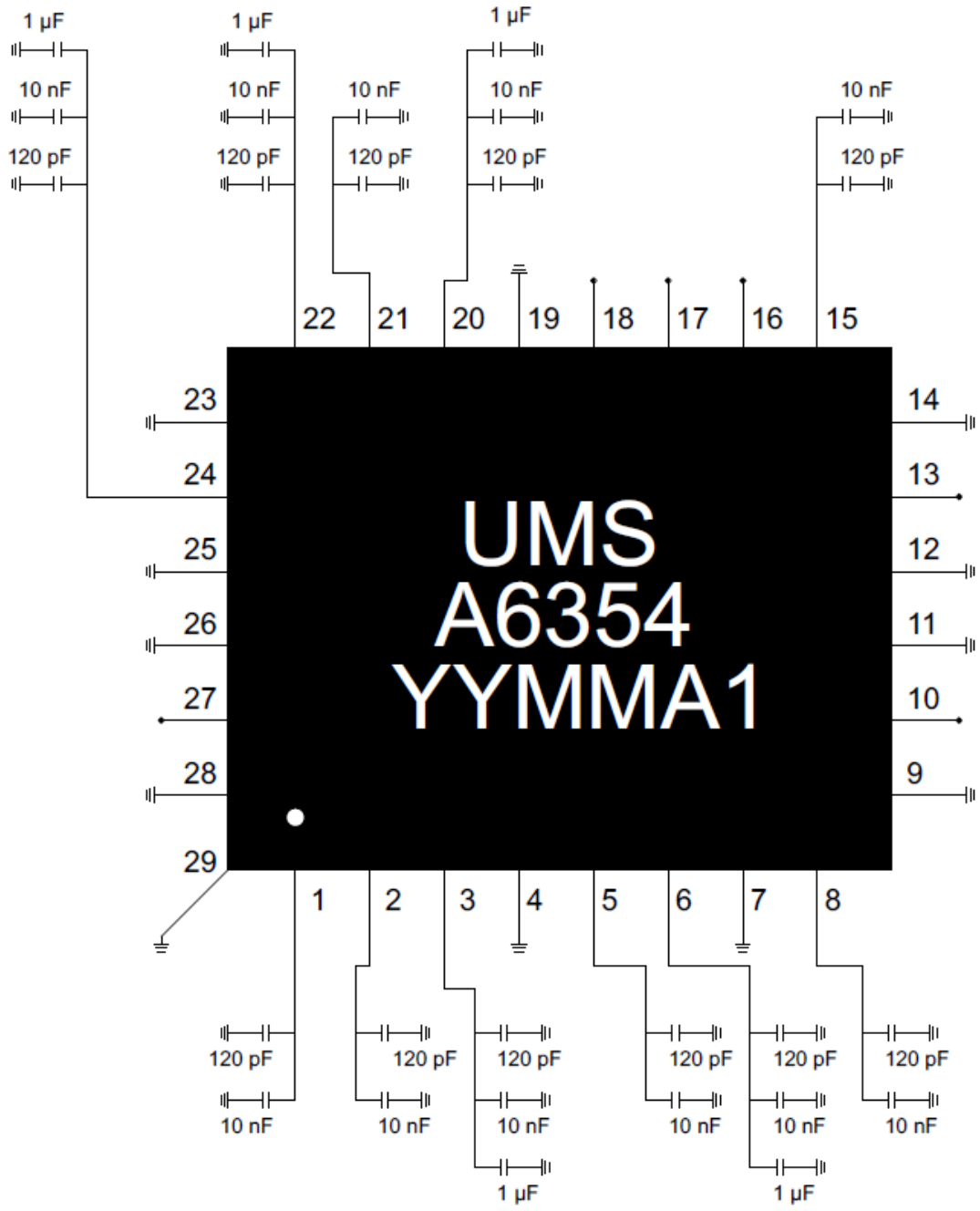
Recommended assembly plan



Recommended circuit bonding table

Label	Pin	Type	Decoupling	Comment
D1, D2S, D2N, D3	3, 6, 20, 22, 24	Vd	120pF, 10nF & 1µF	Drain Supply
G1, G2, G3S, G3N	1, 2, 5, 21	Vg	120pF, 10nF	Gate Supply
SWN, SWS	15, 8	Switch	120pF, 10nF	Switch Supply

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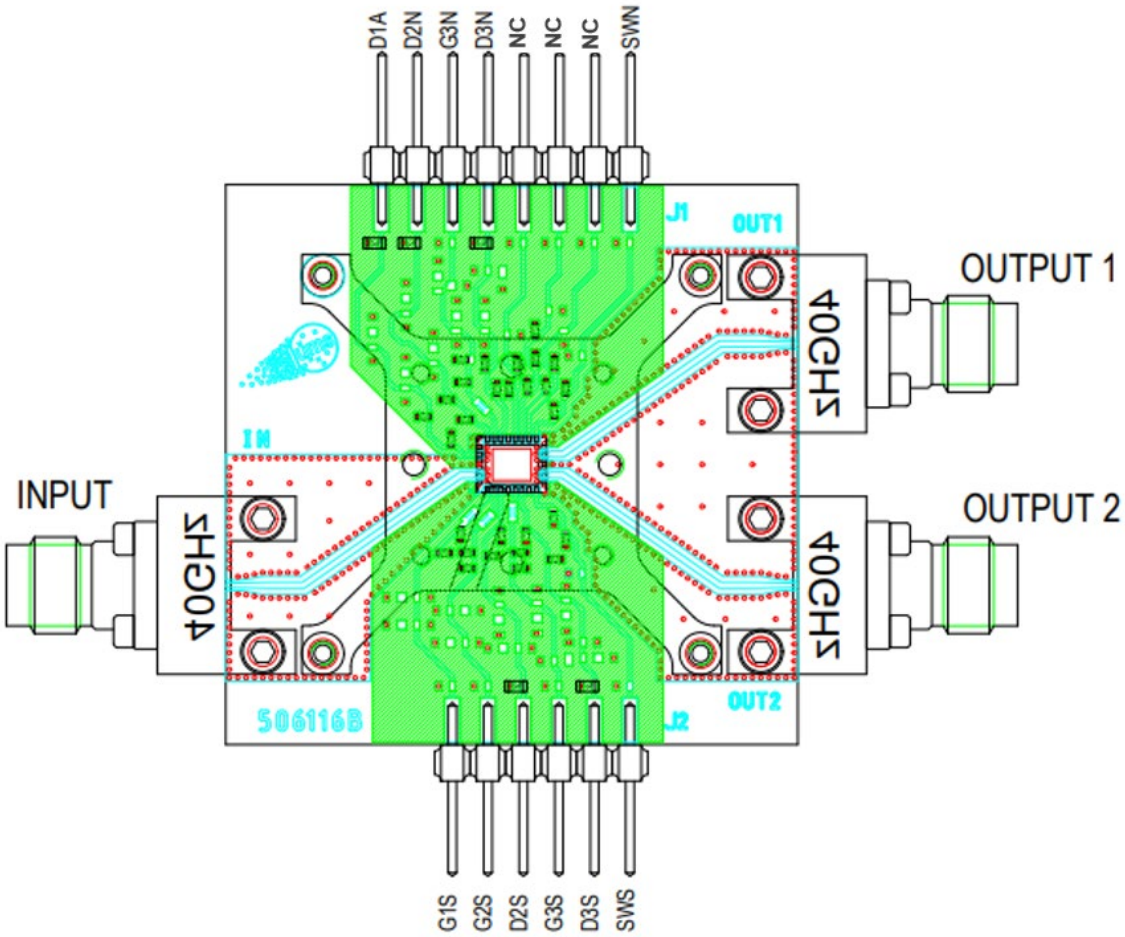
Evaluation board

- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a micro-strip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 10nF ±10 % are recommended for all DC accesses.
- See application note AN0017 for details.



Note: All board measurements are performed using shielded cables, even for DC bias, to ensure safe operation.

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Notes

Due to ESD protection circuits on RF input and output, an external capacitance might be requested to isolate the product from external voltage that could be present on the RF accesses.

ESD protections are also implemented on gate and control accesses.
The DC connections do not include any decoupling capacitor in package. Therefore, it is mandatory to provide a good external DC decoupling (120pF & 10nF) on the PC board, as close as possible to the package.

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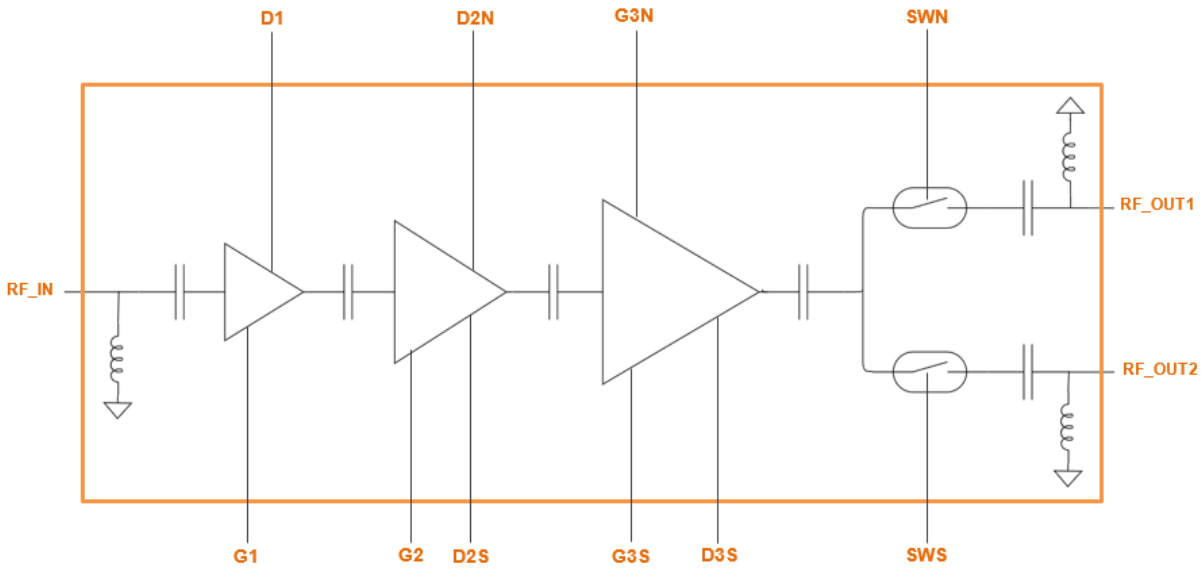
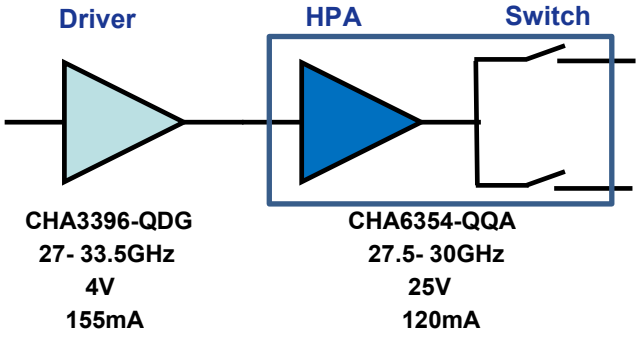
DC Schematic



Recommended UMS Power chain

The CHA6354-QQA is recommended with the CHA3396-QDG as driver.
Total Gain: 49dB
For more information about the CHA3396-QDG, see our web site www.ums-rf.com



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SMD mounting procedure

For the mounting process standard techniques, involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017 at https://www.ums-rf.com.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at https://www.ums-rf.com.

Recommended ESD management

Refer to the application note AN0020 available at https://www.ums-rf.com for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

QFN 5x4 package:	CHA6354-QQA/XY	
	Stick: XY = 20	Tape & reel: XY = 21

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