United Monolithic Semiconductors

CHA6224-98F

20 – 40 GHz 2 Watt GaN Power Amplifier

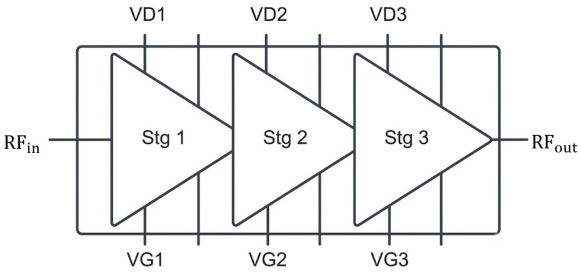
GaN Monolithic Microwave IC in bare die

Description

CHA6224-98F is a three-stage wideband power amplifier operating between 20 and 40GHz. The amplifier provides typically 2W saturated output power and 21dB linear gain. The integration of an on-chip RF ESD inductor further enhances device robustness and reliability under demanding operation conditions.

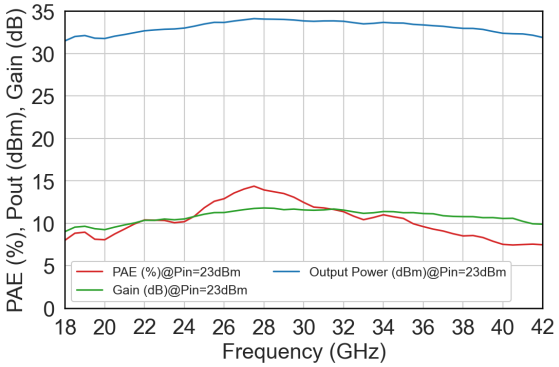
With its compact footprint and excellent RF performance, this amplifier delivers optimized mmWave power solutions to meet the stringent requirements of next-generation Satcom, 5G infrastructure, Test instrumentation and broadband electronic warfare systems.

The circuit is manufactured on a robust 0.1µm HEMT GaN-on-SiC process with top layer mechanical protection. Input and Output are 50Ω matched.



Main Features

- Broadband performance: 20-40GHz
- ~33dBm Pout for +23dBm input power
- Linear Gain: 21dB
- DC bias: Vd=15V@Id=550mA
- Chip size: 3.5 x 2.2mm²



Main Electrical Characteristics

$T_{backside}$ = +25°C ($T_{backside}$: Die backside temperature)

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	20		40	GHz
Gain	Linear Gain		21		dB
Pout	Output Power		33		dBm

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Electrical Characteristics

$T_{backside}$= +25°C, Vd = +15V, CW mode ($T_{backside}$: Die Backside temperature)

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	20		40	GHz
Gain	Linear Gain		21		dB
Pout	Output Power @Pin = 23dBm		33		dBm
PAE	Power Added Efficiency @Pin = 17dBm		11		%
Pdiss	Dissipated power @Pin = 17dBm		14		W
S11	Input Return Loss		-12		dB
S22	Output Return Loss		-10		dB
IMD3	IMD3 (Pout/tone = 23 dBm, Δf = 100MHz)		-22		dBc
Idq	Quiescent Drain bias current		550		mA
Vd	Drain voltage			15	V

These values are representative of on-board measurements as defined on the drawing in paragraph "Evaluation board".

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Absolute Maximum Ratings (1)

$T_{backside}$ = +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	19	V
Vg	Gate bias voltage	-7 to -5	V
Pin	Maximum peak input power overdrive	27	dBm

(1) Operation of this device above anyone of these parameters may cause permanent damage.

Recommended Operating Range (2), (3)

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	≤15	V
Vg	Gate bias voltage	-5 to -2.4	V
Pin	Maximum peak input power overdrive	+23	dBm
Tj	Maximum Junction temperature	200	°C

(2) Electrical performances are defined for specified test conditions

(3) Electrical performances are not guaranteed over all recommended operating conditions

Temperature Range

$T_{backside}$	Operating Temperature Range	-40 to 85	°C
T_{stg}	Storage Temperature Range	-55 to 150	°C

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Typical Bias Conditions

$T_{backside}$=+25°C

Symbol	Pad Nº	Parameter	Values	Unit
Vg	4, 7, 8	Gate voltage tuned for Idq~550mA	-2.4	V
Vd	14, 16, 18	Drain Voltage	15	V

"Power ON" sequence

1. Bias HPA gate voltage at Vg close to Vpinch-off (Vg~-5V)
2. Set Vd bias voltage to 0V: Id=0mA
3. Apply Vd bias voltage, Vd = 15V: Id=0mA
4. Increase Vg up to quiescent bias drain current Idq=550mA
5. Apply RF input Power

"Power OFF" sequence

1. Turn off RF input power
2. Bias HPA Gate voltage at Vg~-5V: Id=0mA
3. Decrease Vd bias voltage down to 0V
4. Turn Vg bias voltage to 0V

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Device thermal performance

All figures given in this section are obtained assuming the chip backside is only cooled down by the conduction through the test board (no convection mode is considered).

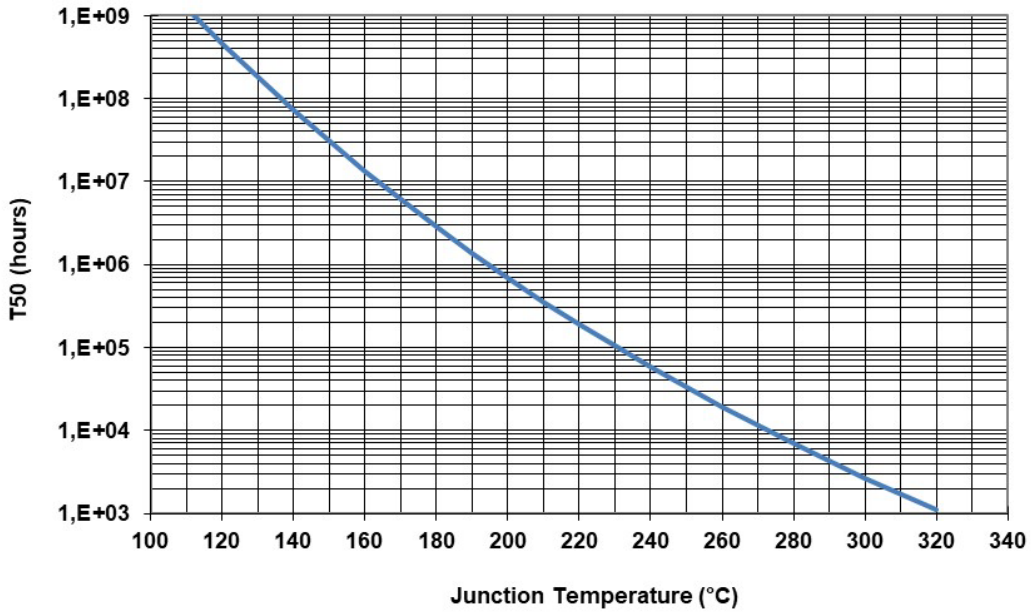
The temperature is monitored at the chip backside ($T_{backside}$).

The system maximum temperature must be adjusted in order to guarantee that the junction temperature of transistors ($T_{junction}$) remains below the maximum value specified in the Recommended Operating Range table.

The system PCB must be designed to comply with this requirement.

Parameter	Conditions	$T_{junction}$ (°C)	Rth (°C/W)	T50 (hours)
Rth(1) Thermal Resistance	Vd = 15V Idq = 550mA Pin = 23dBm Dissipated power = 16.6W	181	5.74	$6.8x10^5$

(1) Thermal resistance measured to backside of the chip with $T_{backside}$=85°C



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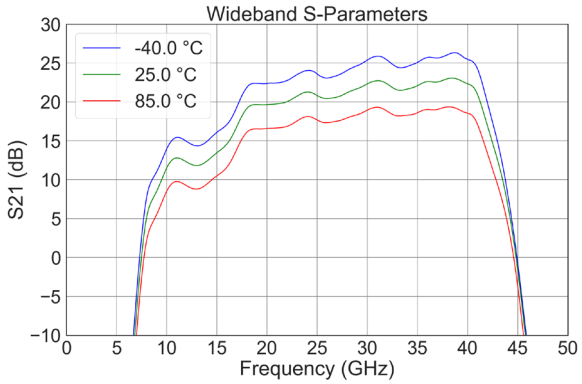
Typical Board Measurements – Small Signal Performance

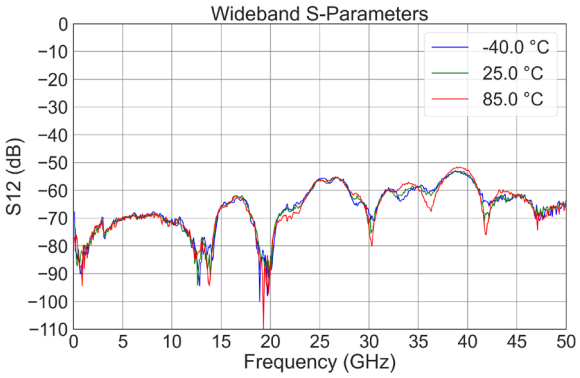
Measurement reference is at the connector plane for S11 and S22, and de-embedded at the wire-bonding plane of the RF lines for S21.

Wide-band S-Parameters vs. Frequency and Temperature
Test conditions: Vd = 15V, Idq = 550mA, $T_{backside}$ = -40°C/25°C/85°C

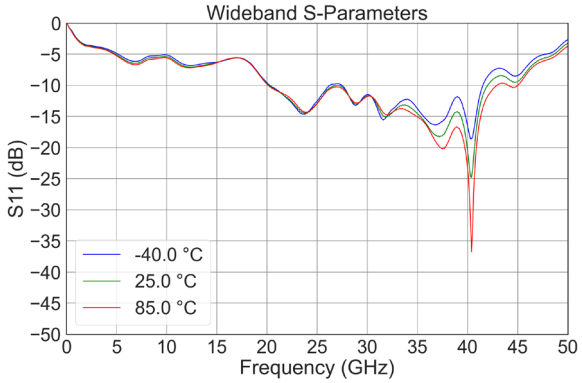
Linear gain



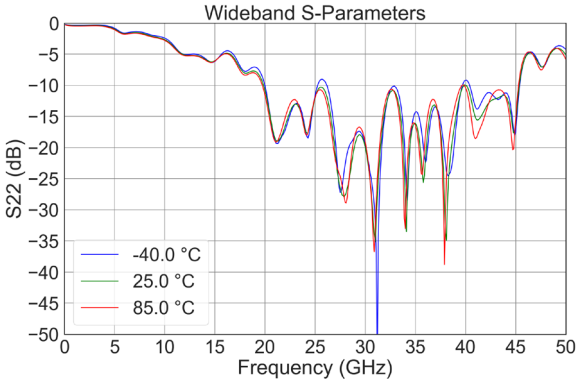
Reverse isolation



Input return loss



Output return loss



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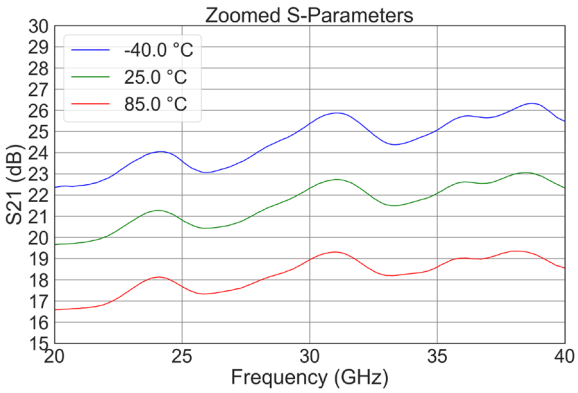
Typical Board Measurements – Small Signal Performance

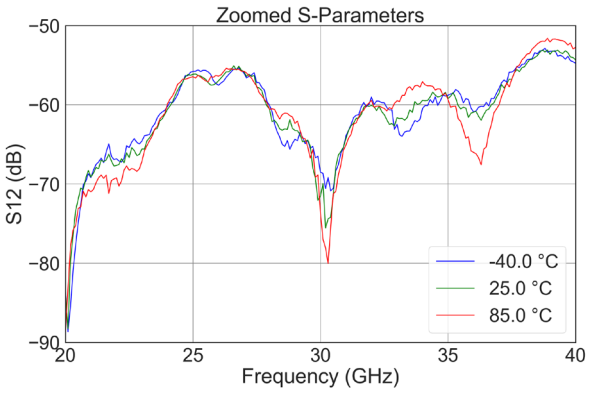
Measurement reference is at the connector plane for S11 and S22, and de-embedded at the wire-bonding plane of the RF lines for S21.

Narrow-band S-Parameters vs. Frequency and Temperature
Test conditions: Vd = 15V, Idq = 550mA, $T_{backside}$ = -40°C/25°C/85°C

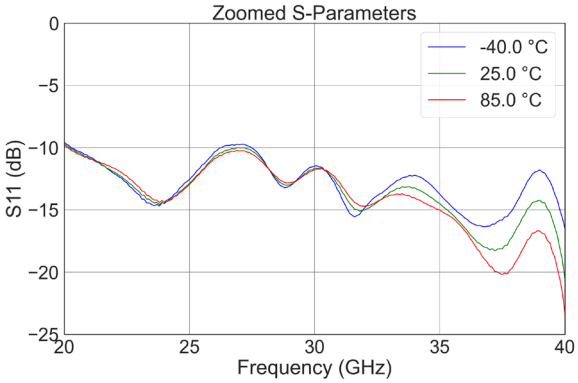
Linear gain



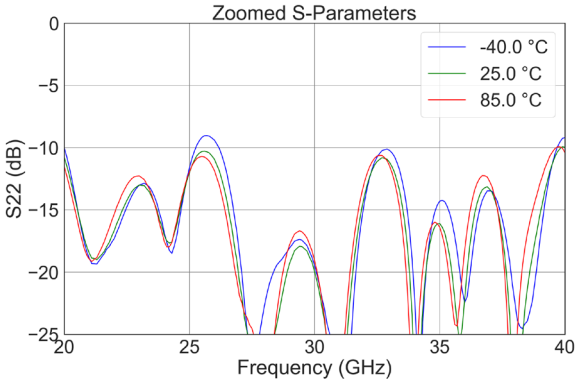
Reverse isolation



Input return loss



Output return loss



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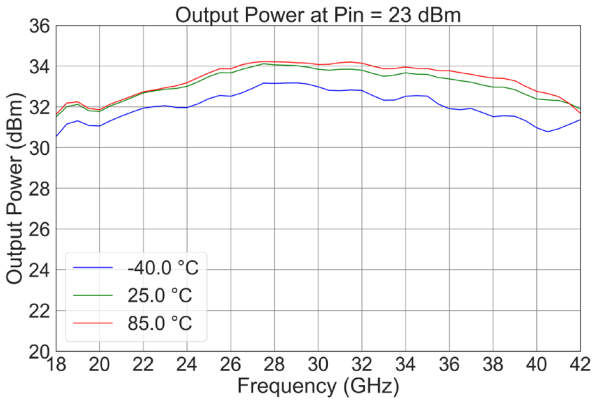
Typical Board Measurements – Large Signal Performance

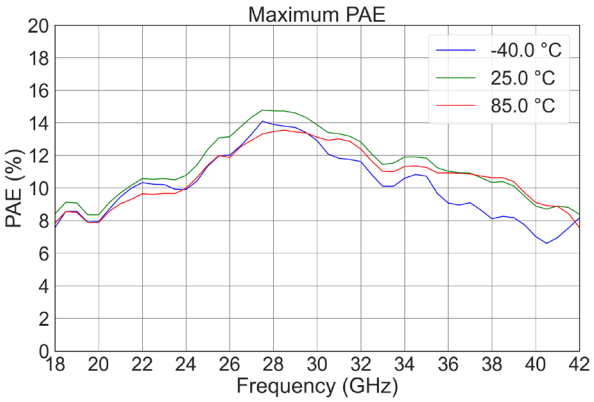
Test conditions: Vd = 15V, Idq = 550mA, $T_{backside}$ = -40°C/25°C/85°C

Measurement reference plane is de-embedded at the wire-bonding plane of the RF lines.

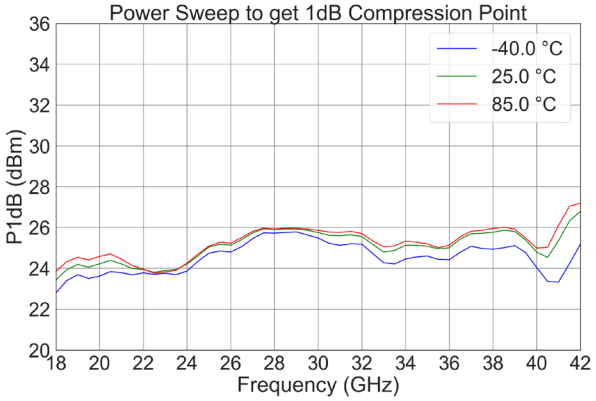
Pout vs Frequency



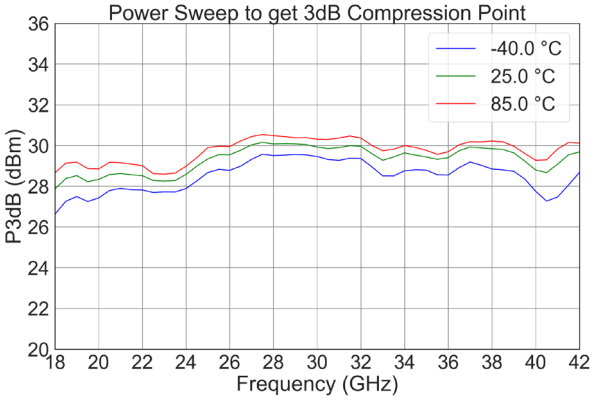
PAE vs Frequency at Pin = 17 dBm



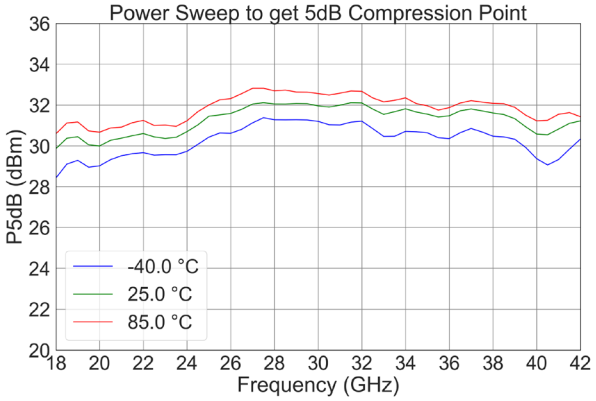
1-dB Compression Output Power



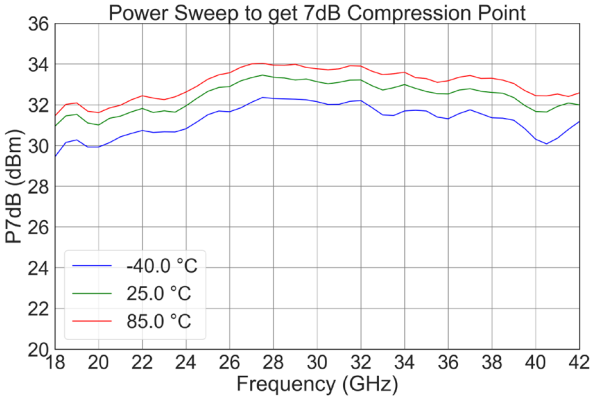
3-dB Compression Output Power



5-dB Compression Output Power



7-dB Compression Output Power



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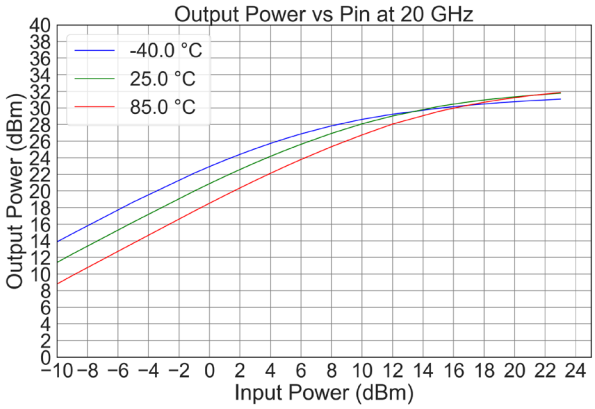
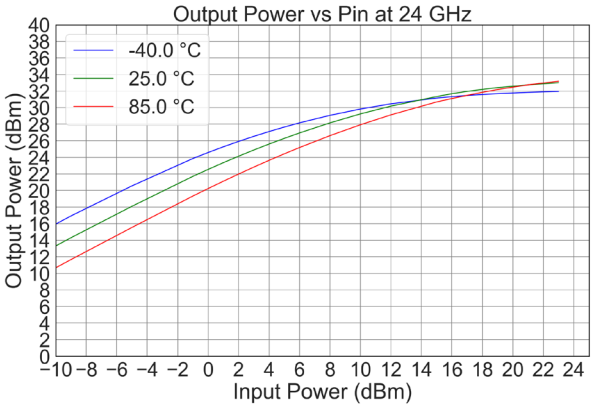
Typical Board Measurements – Large Signal Performance

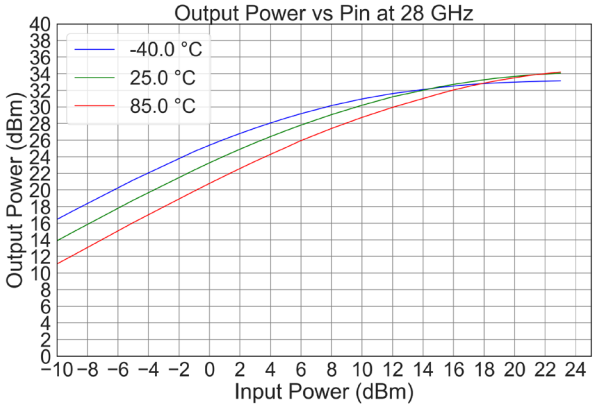
Test conditions: Vd = 15V, Idq = 550mA, $T_{backside}$ = -40°C/25°C/85°C

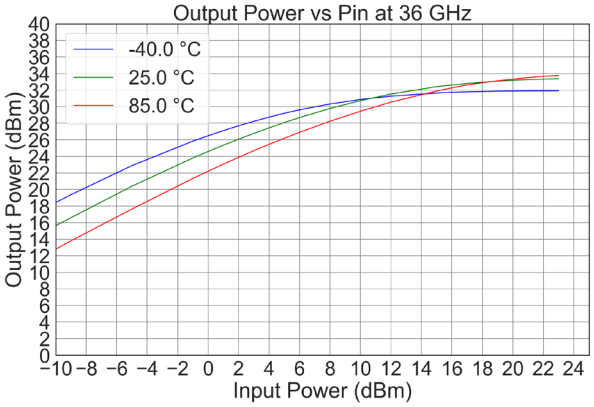
Measurement reference plane is de-embedded at the wire-bonding plane of the RF lines.

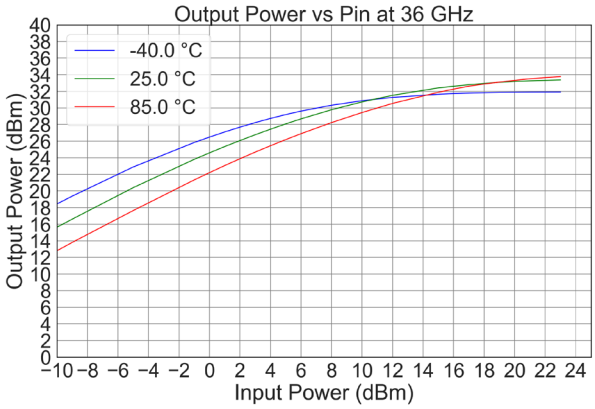
Output power vs. Input power per Frequency

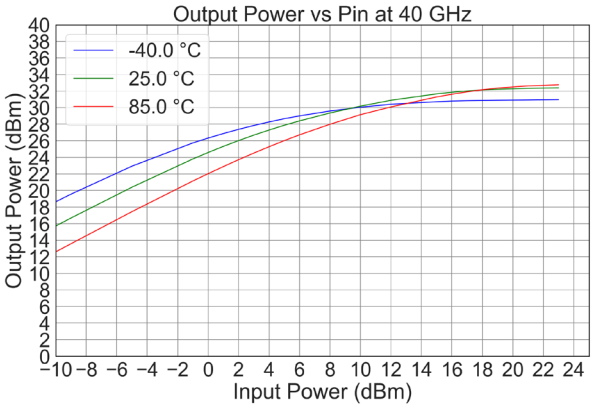












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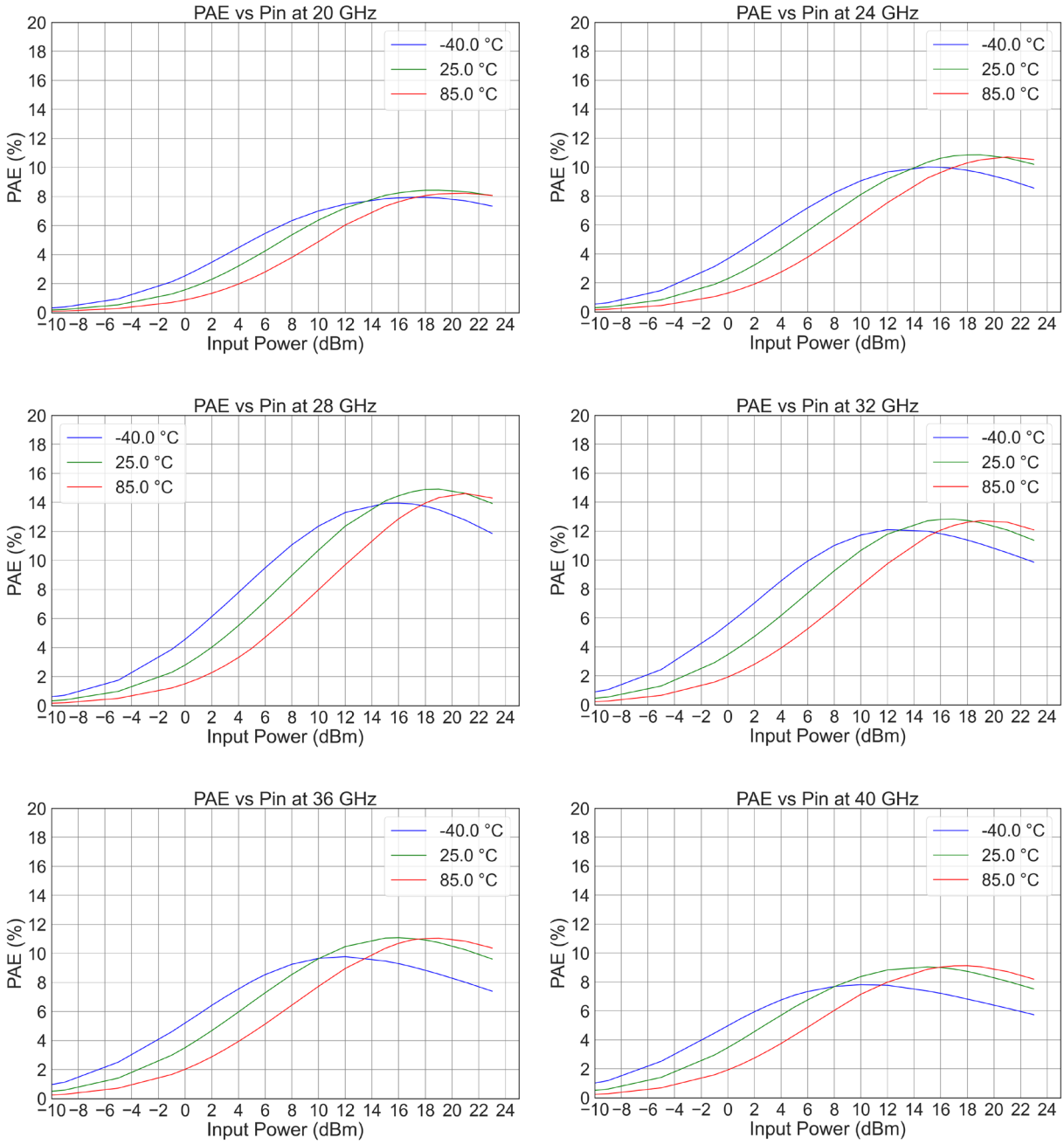
Typical Board Measurements – Large Signal Performance

Test conditions: Vd = 15V, Idq = 550mA, $T_{backside}$ = -40°C/25°C/85°C

Measurement reference plane is de-embedded at the wire-bonding plane of the RF lines.

PAE vs. input power per Frequency



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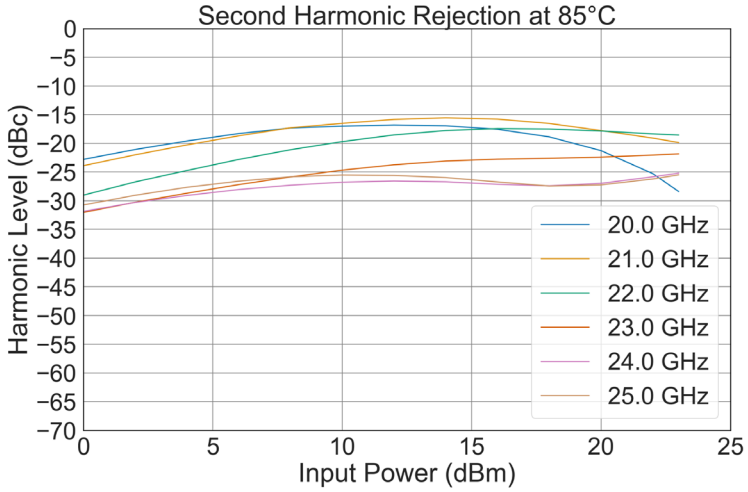
Typical Board Measurements – Harmonic Rejection

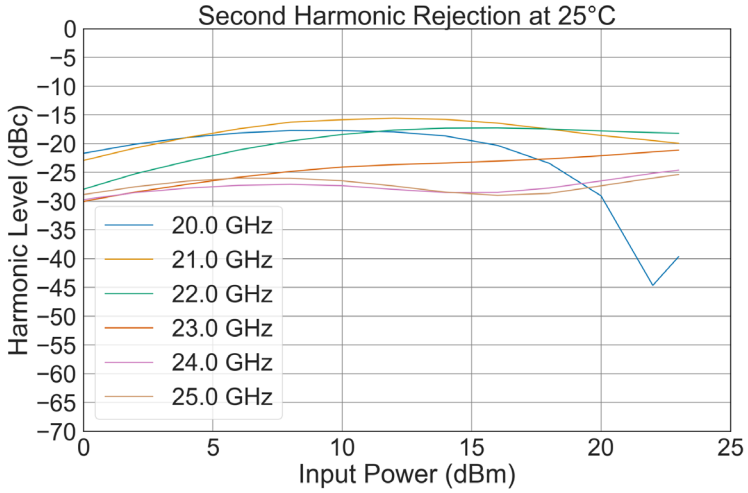
Test conditions: Vd = 15V, Idq = 550mA, $T_{backside}$ = -40°C/25°C/85°C

Measurement reference plane is de-embedded at the wire-bonding plane of the RF lines.

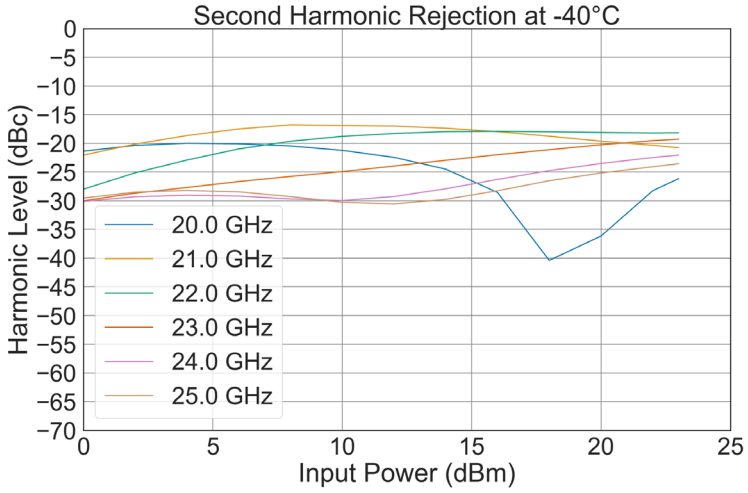
Second Harmonic Rejection vs. Input power vs. Frequency at 85°C



Second Harmonic Rejection vs. Input power vs. Frequency at 25°C



Second Harmonic Rejection vs. Input power vs. Frequency at -40°C



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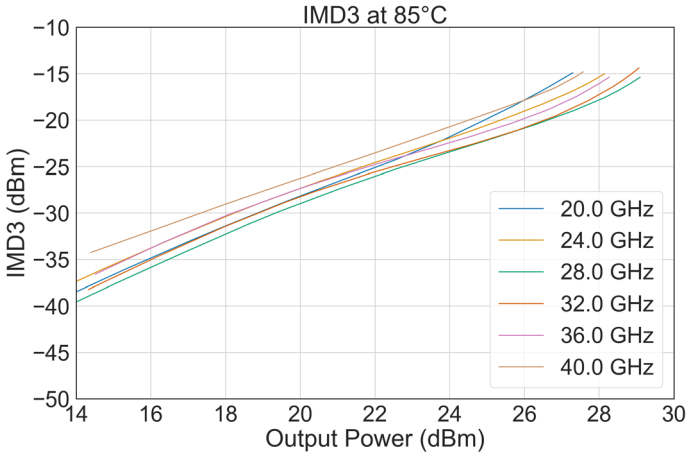
Typical Board Measurements - Two-tone Large Signal Performance

Test conditions:

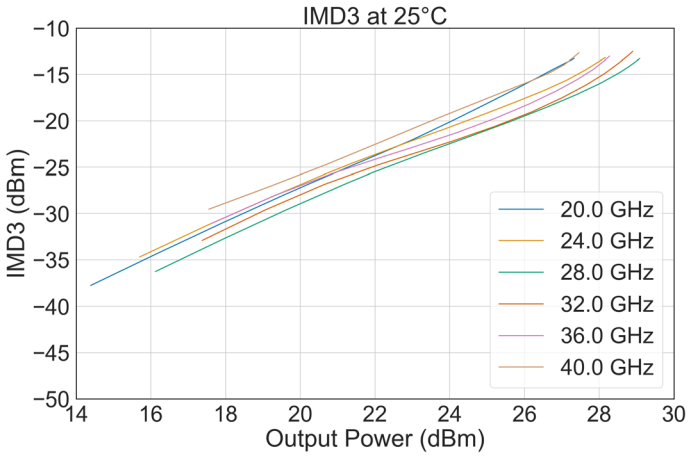
Vd = 15V, Idq = 550mA, Tone Spacing = 100MHz, $T_{backside}$ = -40°C/25°C/85°C

Measurement reference plane is de-embedded at the wire-bonding plane of the RF lines.

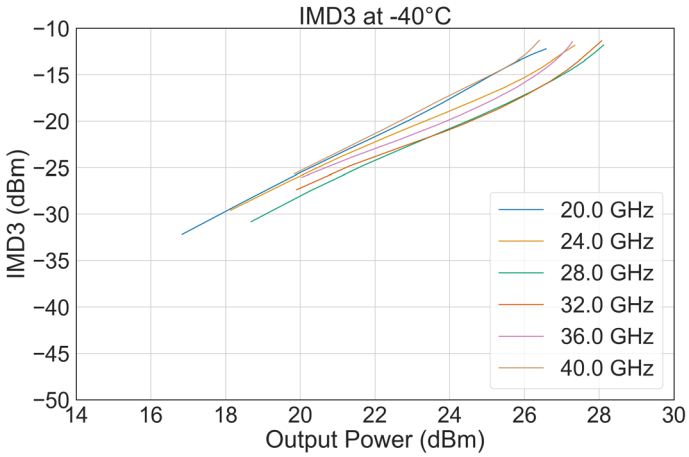
IMD3 vs Output power per Tone vs Frequency at 85°C



IMD3 vs Output power per Tone vs Frequency at 25°C



IMD3 vs Output power per Tone vs Frequency at -40°C



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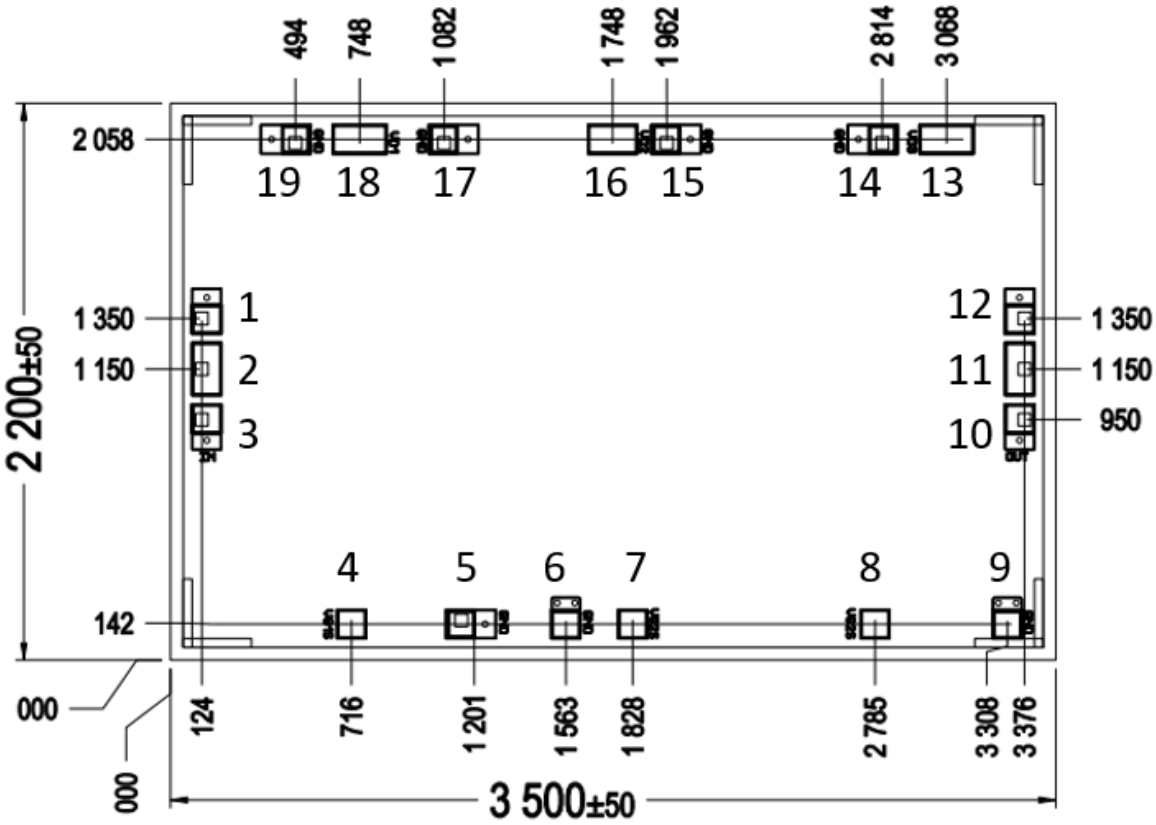
Chip mechanical data



Chip thickness: 50µm
Chip size: 3500/2200 ±50µm
All dimensions are in micrometers

1-	GND RF	8-	VG3	14-	GND
2-	RF IN	9-	GND	15-	GND
3-	GND RF	10-	GND RF	16-	VD2
4-	VG1	11-	RF OUT	17-	GND
5-	GND	12-	GND RF	18-	VD1
6-	GND	13-	VD3	19-	GND
7-	VG2				

Ensure that the PCB is designed to provide the best possible ground to the die

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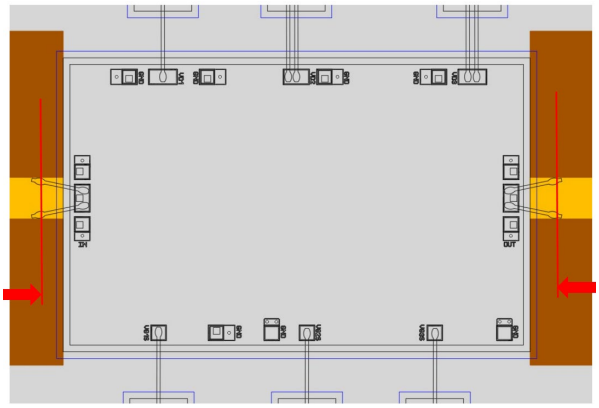
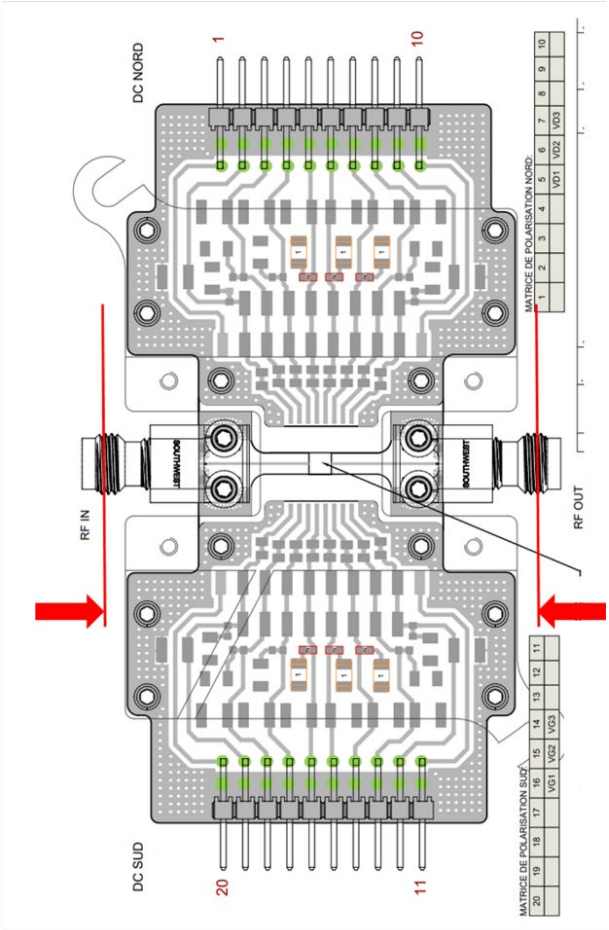
Measurement Reference Planes

The reference planes used for S21, power and linearity measurements given above are located at input and output of the MMIC as defined in the drawing



Input and Output Return Loss (S11 and S22) are given at Evaluation Board connectors reference planes as defined in the drawing



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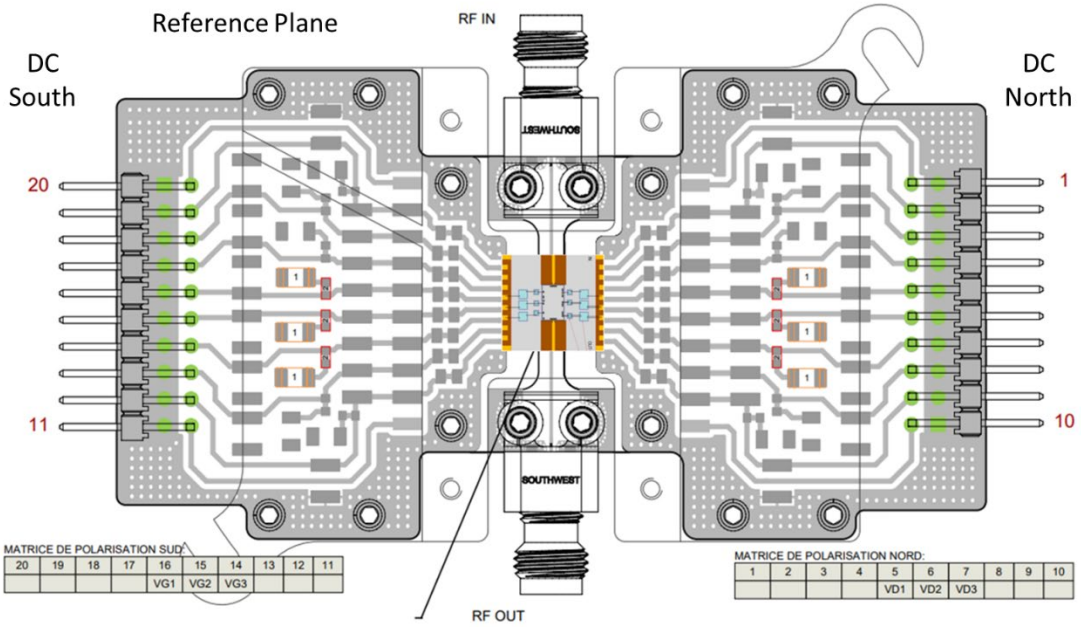
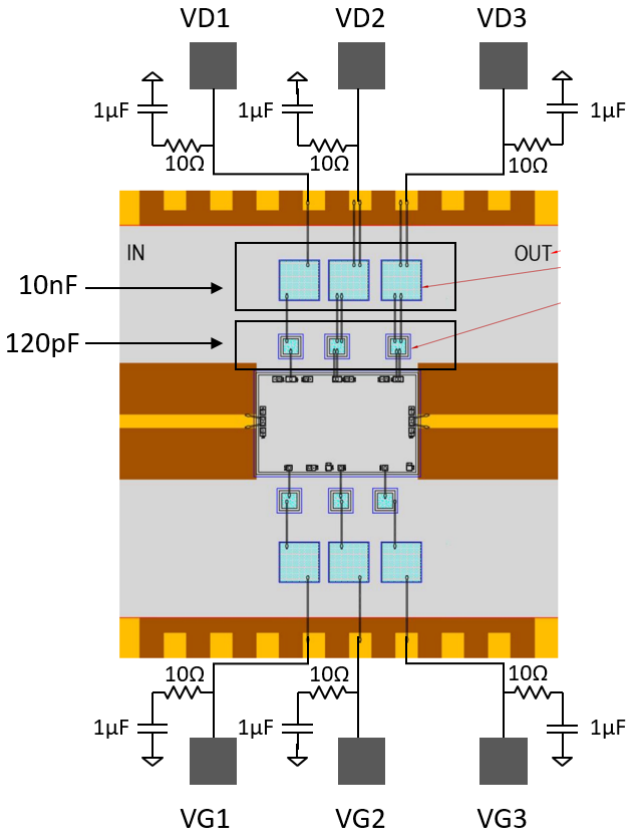
Evaluation board assembly outline



3 levels of decoupling capacitors have been used, 2 on the tab and 1 on the board. The first level is composed of 120 pF chip capacitors, the second level is composed of 10nF chip capacitors and the third level is composed of 100nF SMD 1210 capacitors in series with 10-ohm resistors. The first two levels should be as close as possible to the die.



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Recommended reflow process

Refer to the application note AN0001 available at http://www.ums-rf.com for die attach.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at http://www.ums-rf.com.

Recommended ESD management

Refer to the application note AN0020 available at https://www.ums-rf.com/application-notes/ for ESD sensitivity and handling recommendations for UMS products.

Recommended Evaluation board (EVB)

Refer to the application note AN0030 available at https://www.ums-rf.com/application-notes/

Ordering Information

Chip form:	CHA6224-98F/00
Evaluation board:	EVB-CHA6224-98F

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