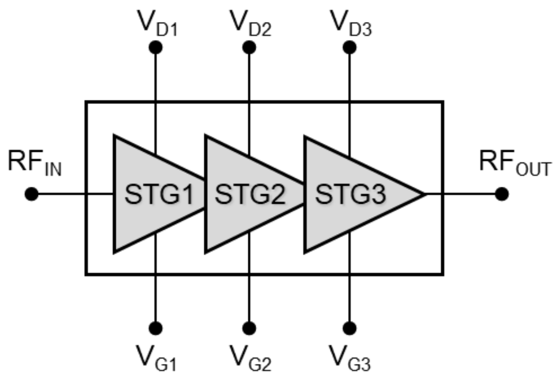
7.25-7.75GHz 3W Power Amplifier

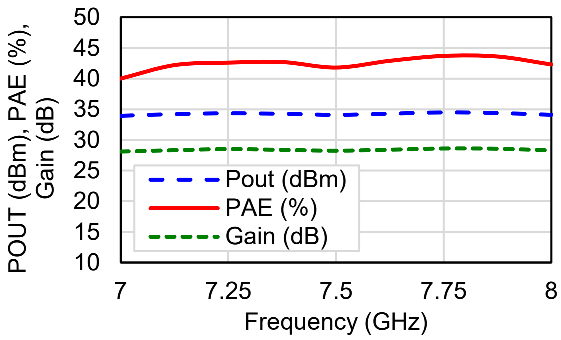
GaN Monolithic Microwave IC

Description

The CHA6154-99F is a three-stage monolithic GaN Medium Power Amplifier operating between 7.25 and 7.75GHz and typically providing 2.8W Output Power at 43% of Power Added Efficiency. This amplifier exhibits more than 1W linear Output Power associated to 17dBc NPR and 33% Power Added Efficiency. It also provides a typical small signal gain of 36.5dB. This amplifier is well suited for radar and space communications as well as telecommunications. It can be used as a Driver or a Power Amplifier.
The circuit is manufactured using a space evaluated, robust GaN-on-SiC HEMT process and is provided as a bare die for direct integration into hybrid circuits.



V_D = 28V, I_{DQ} = 70mA,
$T_{backside}$ = 25°C, P_{IN} = 5.8 dBm



Main Features

- Frequency band: 7.25-7.75GHz
- 34.5dBm P_{OUT} at 43% PAE
- 36.5dB linear gain
- NPR = 17dBc at 30.4dBm Average Pout[(1)]
- Typical DC bias: V_D = 28V@I_{DQ} = 70mA
- Physical dimensions : 4.08x1.7mm²
- Available as bare die

(1) BW= 500MHz, Notch=10%, Number of tones: 4000

Main Electrical Characteristics

$T_{backside}$ = 25°C, V_D = 28V, ($T_{backside}$: Die backside temperature)

Symbol	Parameter	Min	Typ	Max	Unit
Frequency	Frequency range	7.25		7.75	GHz
Gain	Linear Gain		36.5		dB
P_{OUT}	Output power at max PAE		34.5		dBm
PAE	Maximum Power Added Efficiency		43		%
NPR	Noise Power Ratio @ Pout = 30.4dBm (BW=500MHz)		17		dBc
I_{DQ}	Quiescent Current		70		mA

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Electrical Characteristics

$T_{backside}$ = 25°C, V_D = 28V, ($T_{backside}$: Die backside temperature)

Symbol	Parameter	Min	Typ	Max	Unit
Frequency	Frequency range	7.25		7.75	GHz
Gain	Linear Gain		36.5		dB
RL_{IN}	Input Return Loss		12		dB
RL_{OUT}	Output Return Loss		8		dB
P_{OUT}	Output power at maximum PAE		34.5		dBm
PAE	Maximum Power Added Efficiency		43		%
I_{DQ}	Typical Quiescent current		70		mA

These values are representative of onboard measurements as defined on the drawing paragraph “Evaluation board”.

This device is electrostatic discharge sensitive please observe caution while handling.

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Typical Bias Conditions

$T_{backside}$ = 25°C

Symbol	Parameter	Value	Unit
V_{G1}, V_{G2}, V_{G3}	Gate voltage tuned for I_{DQ} = 70mA	-3.41	V
V_{D1}, V_{D2}, V_{D3}	Drain voltage	28	V

Absolute Maximum Ratings[1]

Symbol	Parameter	Values	Unit
V_D	Drain bias voltage	45	V
V_G	Gate bias voltage	-7 to -3.1	V
P_{IN}	Maximum peak input power overdrive	10	dBm

[1] Operation of this device above anyone of these parameters may cause permanent damage.

Recommended Operating Range [2], [3]

Symbol	Parameter	Values	Unit
V_D	Drain bias voltage	24-30	V
I_{DQ}	Quiescent drain current	0-140	mA
P_{IN}	Maximum peak input power overdrive [2]	6	dBm
T_J	Maximum Junction temperature [4]	200	°C

[2] Electrical performances are defined for specified test conditions.
[3] Electrical performances are not guaranteed over all recommended operating conditions.
[4] See device thermal performances section.

Temperature range

$T_{backside}$	Operating temperature range	-20 to 100	°C
T_{STG}	Storage temperature range	-55 to 150	°C

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Biasing procedure

Device power up instructions:

1. Set the gate voltage to -5V
2. Apply the drain voltage V_D (typically 28V)
3. Increase V_G up to quiescent bias drain current I_{DQ} (typically 70mA)
4. Apply RF signal

Device power down instructions:

1. Turn off RF signal
2. Decrease the gate voltage to -5V
3. Decrease the drain voltage to 0V
4. Increase the gate voltage to 0V
5. Turn off V_D supply
6. Turn off V_G supply

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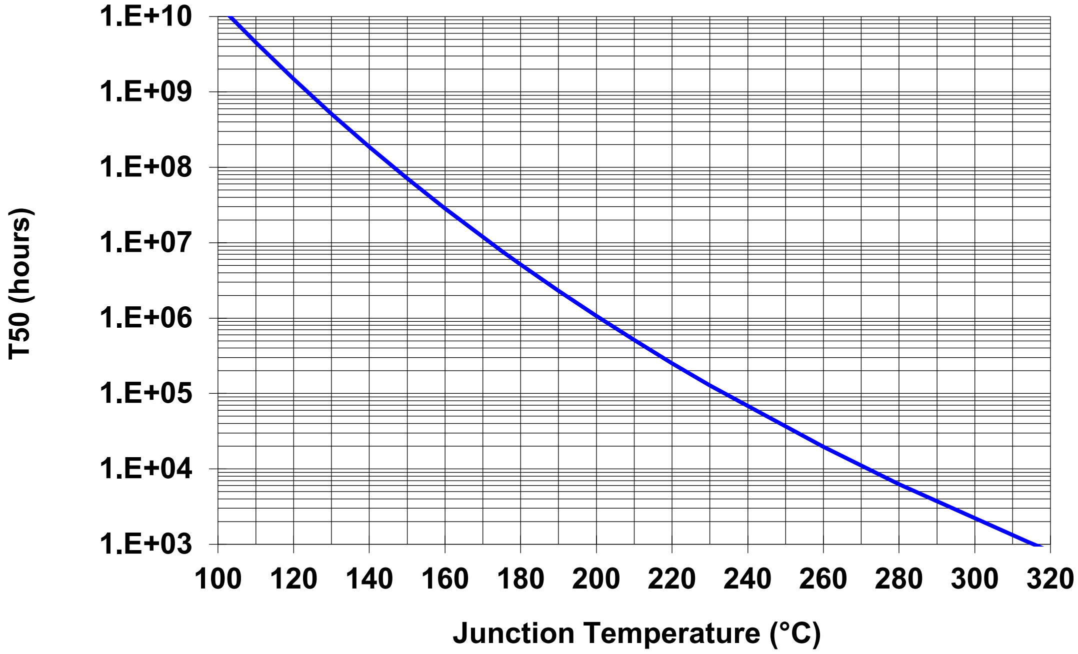
Device thermal performances

All figures given in this section are obtained assuming the chip backside is only cooled down by the conduction through the test board (no convection mode is considered).
The temperature is monitored at the chip backside ($T_{backside}$).
The system maximum temperature must be adjusted in order to guarantee that T_J remains below the maximum value specified in the Recommended Operating Range table.
The system PCB must be designed to comply with this requirement.

Parameter	Biasing conditions	T_J (°C)	R_{TH} (°C/W)	T50 (hours)
R_{TH}(1) Thermal resistance (Junction to backside)	V_D = 28V I_{DQ} = 70mA At 8dB compression P_{DISS} = 4.2W (CW)	139	9.3	1.9E+8

(1) Assuming 100°C $T_{backside}$



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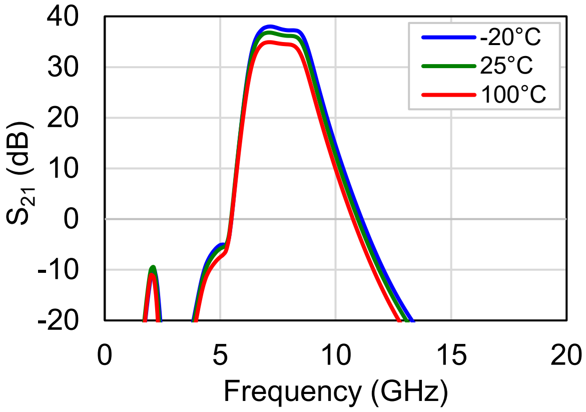
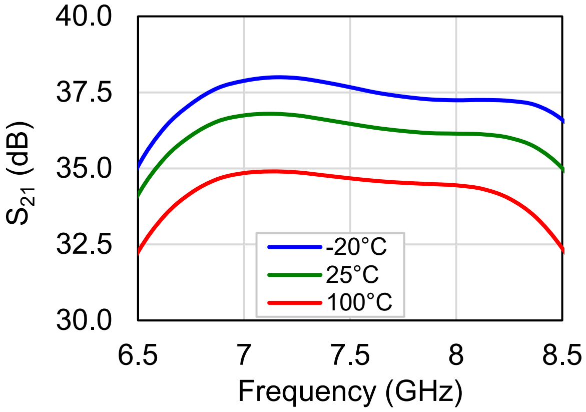
Typical Board Measurements: Small Signal Performance

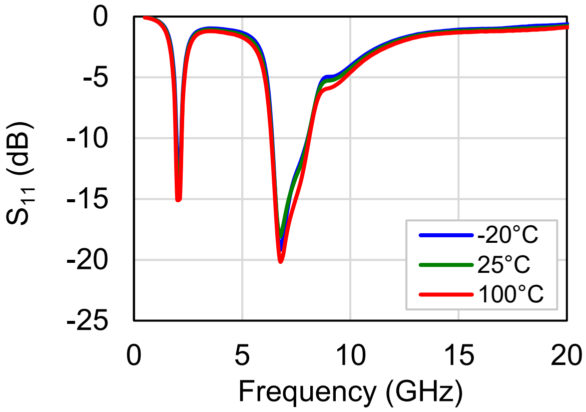
Test conditions: CW, V_D = 28V, V_G = -3.41V, $T_{backside}$ = -20°C / 25°C / 100°C

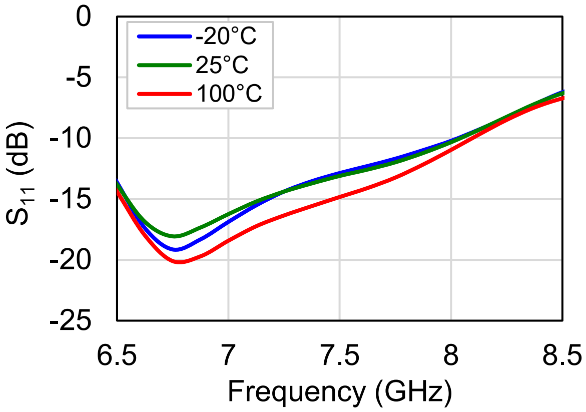
Linear Gain vs. Frequency vs. Temperature



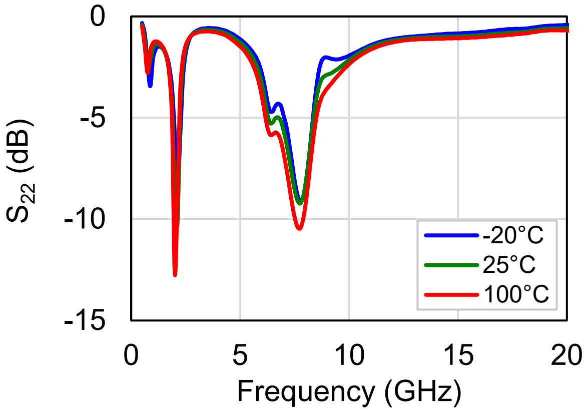


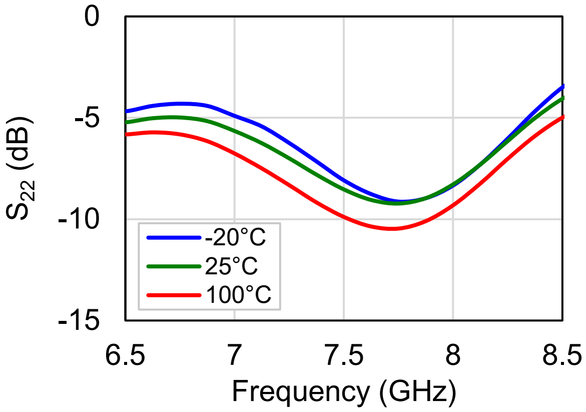
Input Return Loss vs. Frequency vs. Temperature





Output Return Loss vs. Frequency vs. Temperature





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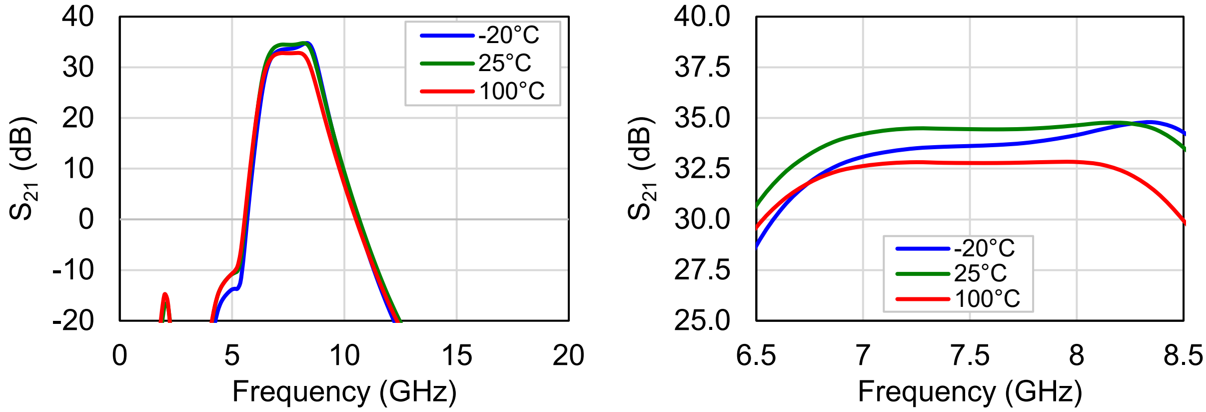
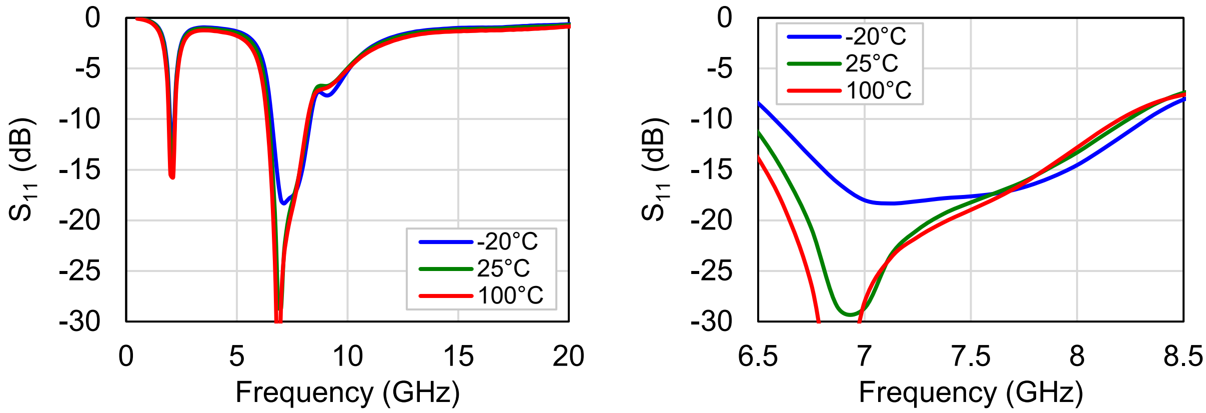
Typical Board Measurements: Small Signal Performance

Test conditions: CW, V_D = 28V, V_G = -3.53V, $T_{backside}$ = -20°C / 25°C / 100°C

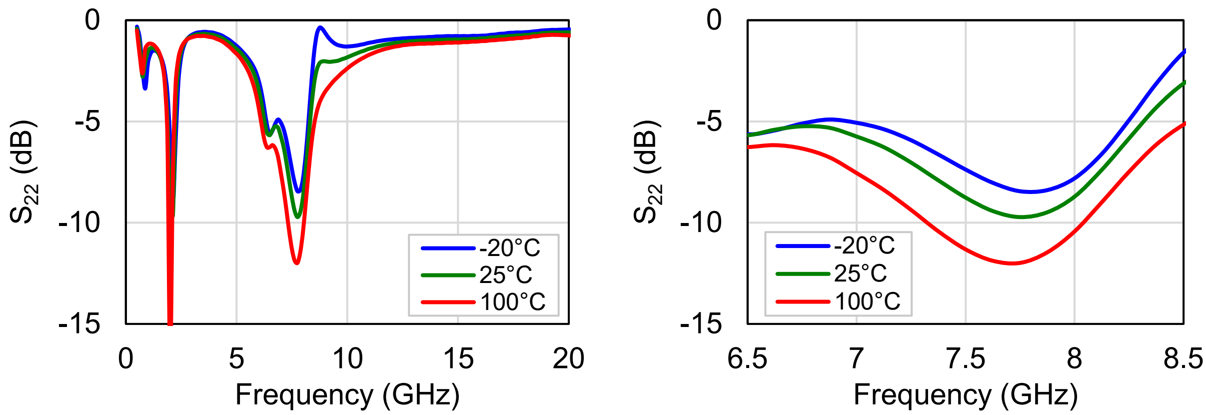
Linear Gain vs. Frequency vs. Temperature



Input Return Loss vs. Frequency vs. Temperature



Output Return Loss vs. Frequency vs. Temperature



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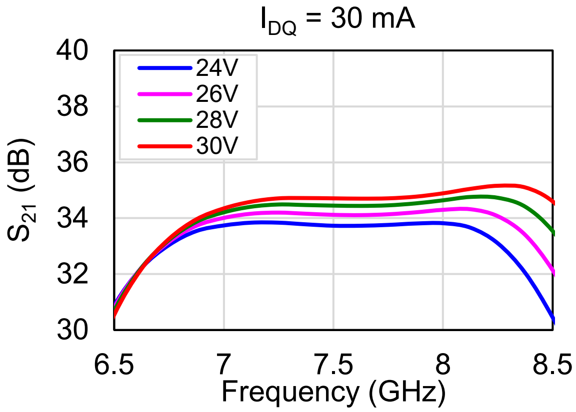
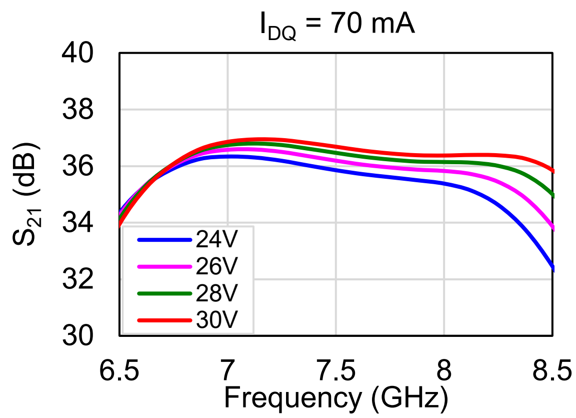
Typical Board Measurements: Small Signal Performance

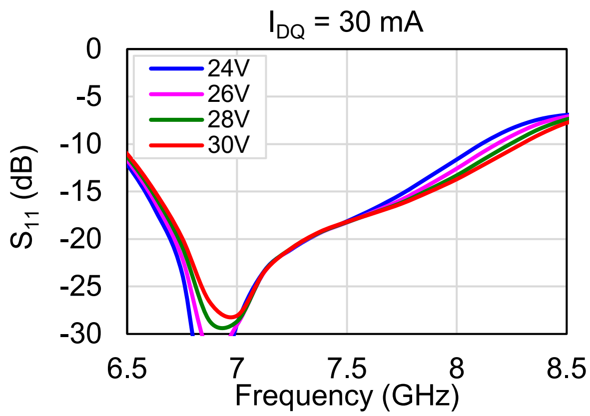
Test conditions: CW, V_D = 24V / 26V / 28V / 30V, I_{DQ} = 30mA / 70mA, $T_{backside}$ = 25°C

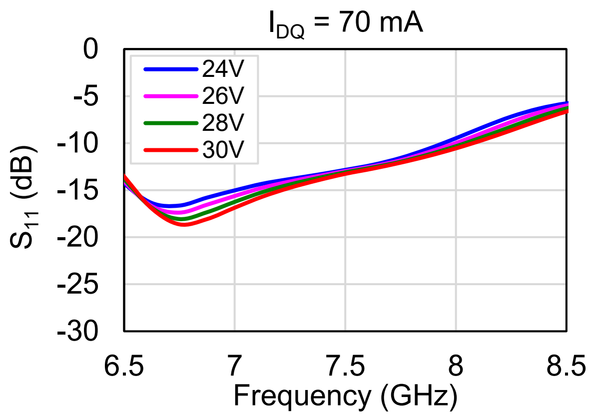
Linear Gain vs. Frequency vs. V_D



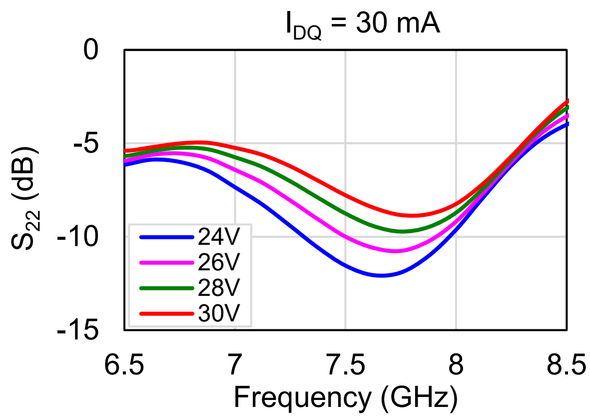


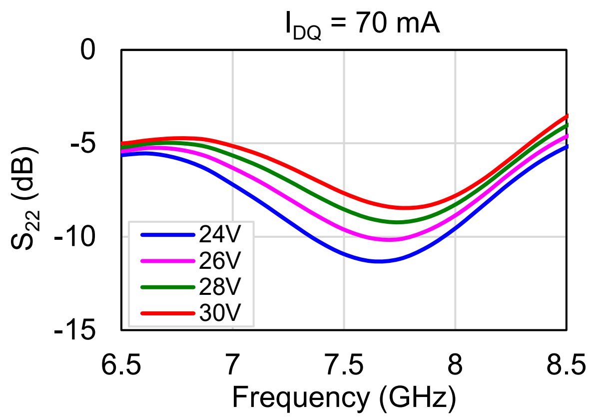
Input return Loss vs. Frequency vs. V_D





Output Return Loss vs. Frequency vs. V_D





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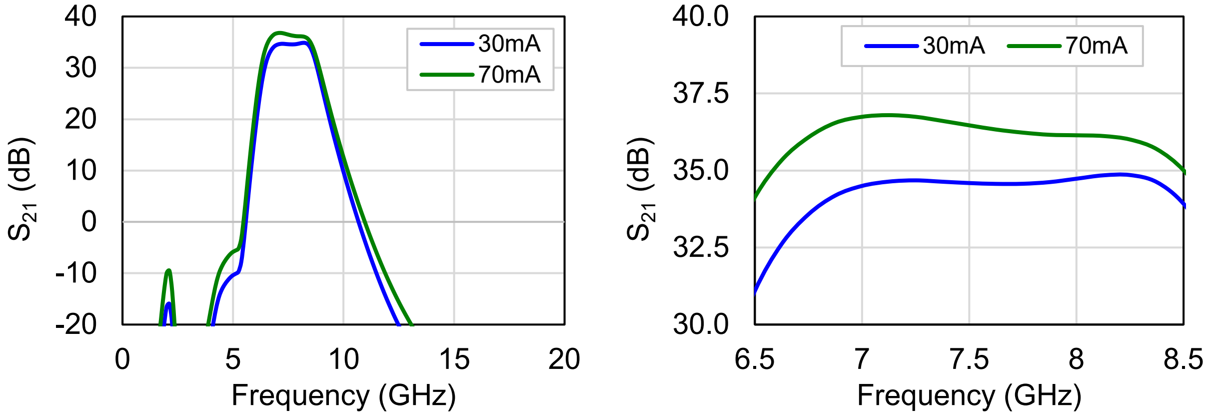
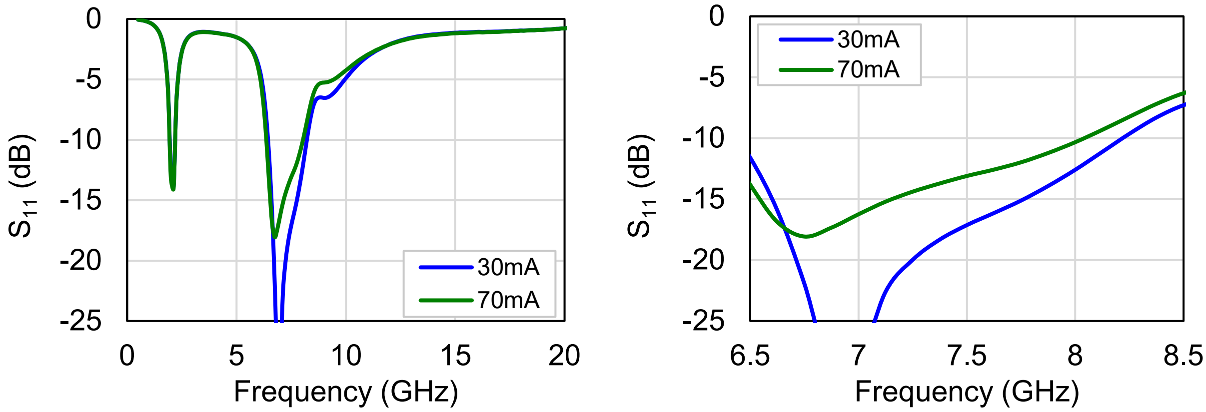
Typical Board Measurements: Small Signal Performance

Test conditions: CW, V_D = 28V, I_{DQ} = 30mA / 70mA, $T_{backside}$ = 25°

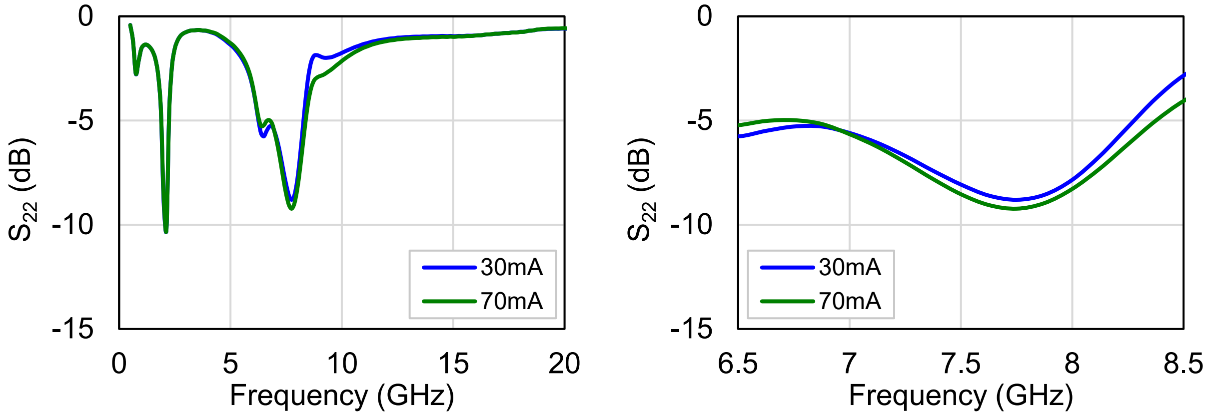
Linear Gain vs. Frequency vs. I_{DQ}



Input Return Loss vs. Frequency vs. I_{DQ}



Output Return Loss vs. Frequency vs. I_{DQ}



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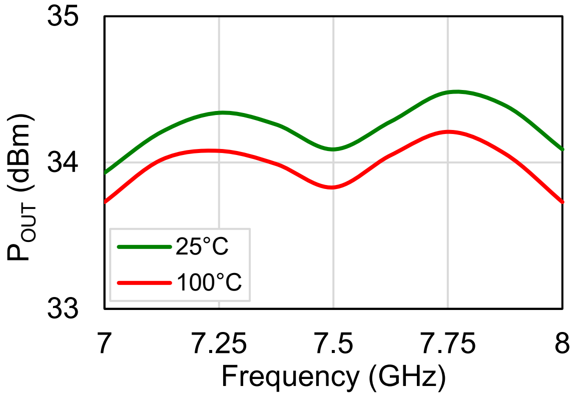
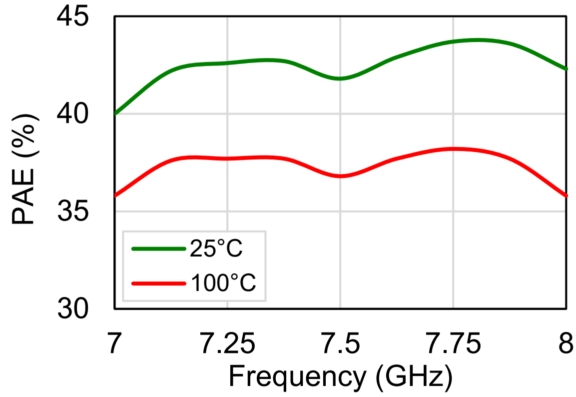
Typical Board Measurements: Large Signal Performance

Test conditions: CW, V_D = 28V, V_G = -3.41V, P_{OUT} at maximum PAE
$T_{backside}$ = 25°C, P_{IN} = 5.8 dBm,
$T_{backside}$ = 100°C, P_{IN} = 8.4 dBm

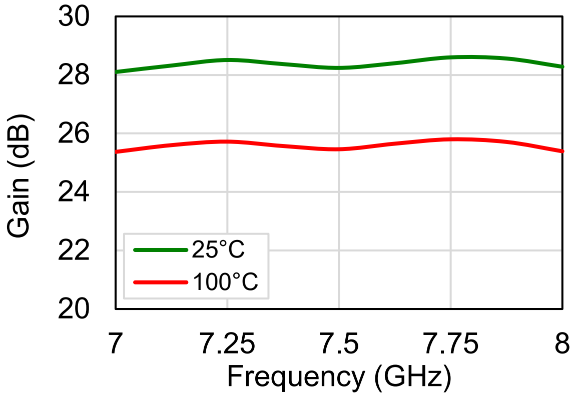
Output Power vs. Frequency vs. Temperature



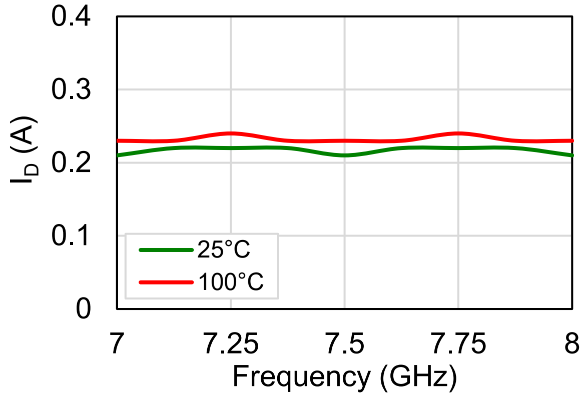
Power Added Efficiency vs. Frequency vs. Temperature



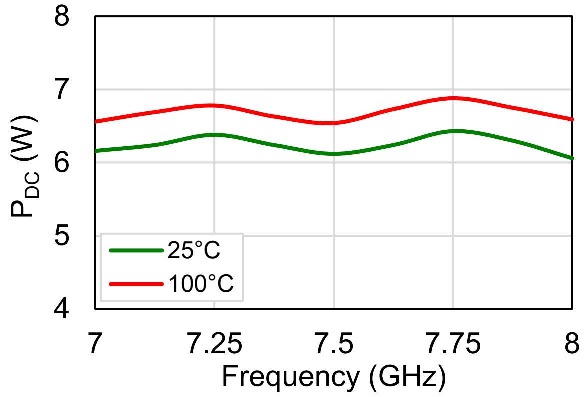
Gain vs. Frequency vs. Temperature



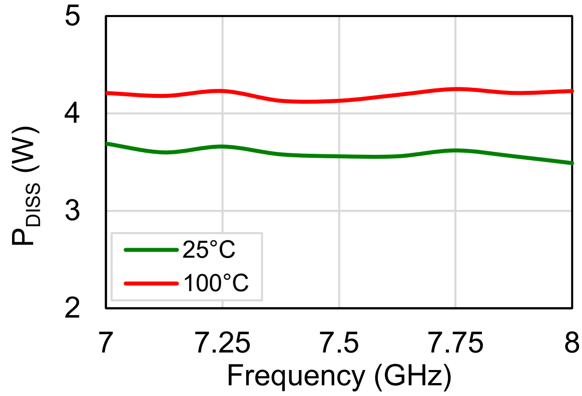
Drain current vs. Frequency vs. Temperature



DC power vs. Frequency vs. Temperature



Dissipated power vs. Frequency vs. Temperature



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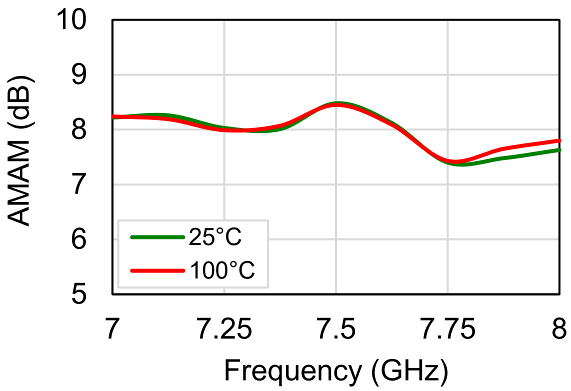
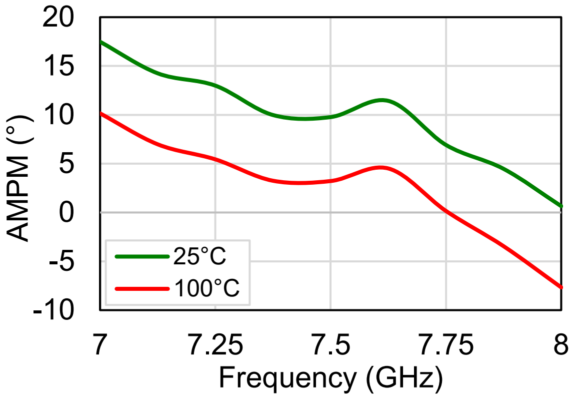
Typical Board Measurements: Large Signal Performance

Test conditions: CW, V_D = 28V, V_G = -3.41V, P_{OUT} at maximum PAE
$T_{backside}$ = 25°C, P_{IN} = 5.8 dBm, $T_{backside}$ = 100°C, P_{IN} = 8.4 dBm

AMAM vs. Frequency vs. Temperature



AMPM vs. Frequency vs. Temperature



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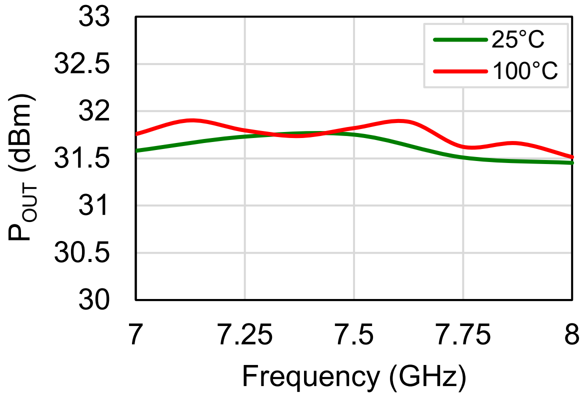
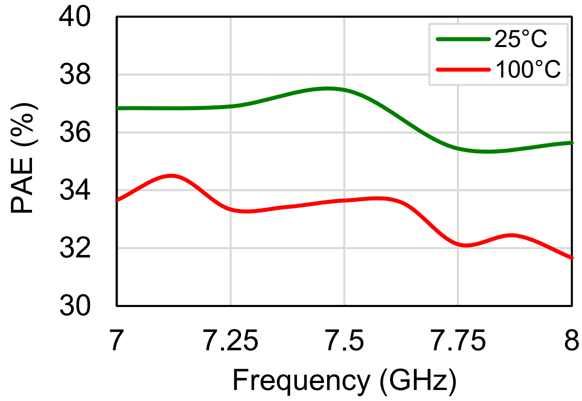
Typical Board Measurements: Large Signal Performance

Test conditions: CW, V_D = 28V, V_G = -3.41V
$T_{backside}$ = 25°C, P_{IN} = -2.2 dBm i.e. 3dB Output Power Back-Off
$T_{backside}$ = 100°C, P_{IN} = 0.8 dBm i.e. 3dB Output Power Back-Off

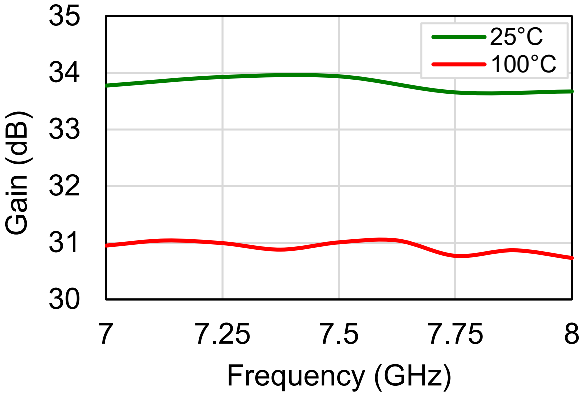
Output Power vs. Frequency vs. Temperature



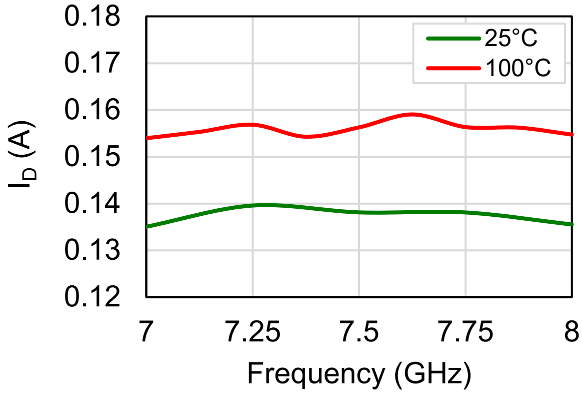
Power Added Efficiency vs. Frequency vs. Temperature



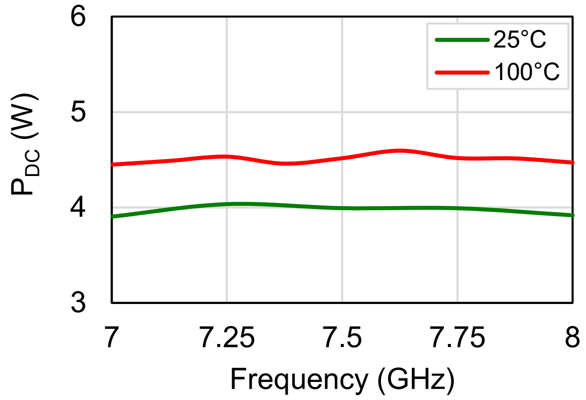
Gain vs. Frequency vs. Temperature



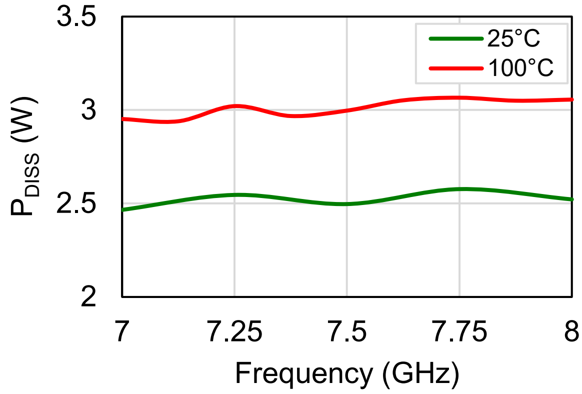
Drain current vs. Frequency vs. Temperature



DC power vs. Frequency vs. Temperature



Dissipated power vs. Frequency vs. Temperature



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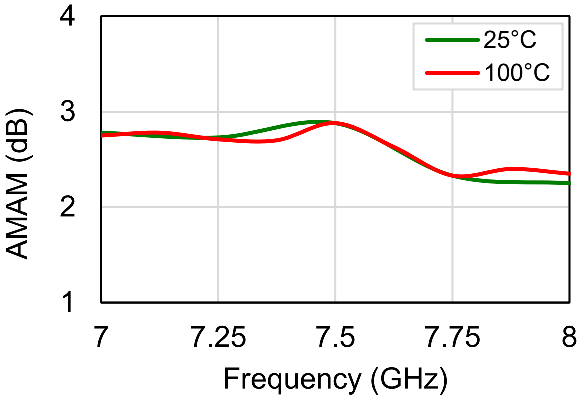
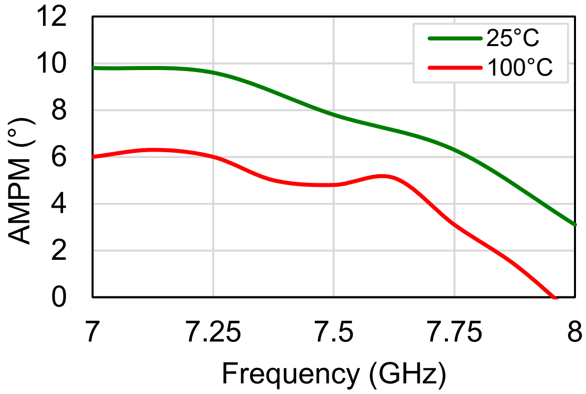
Typical Board Measurements: Large Signal Performance

Test conditions: CW, V_D = 28V, V_G = -3.41V
$T_{backside}$ = 25°C, P_{IN} = -2.2 dBm i.e. 3dB Output Power Back-Off
$T_{backside}$ = 100°C, P_{IN} = 0.8 dBm i.e. 3dB Output Power Back-Off

AMAM vs. Frequency vs. Temperature



AMPM vs. Frequency vs. Temperature



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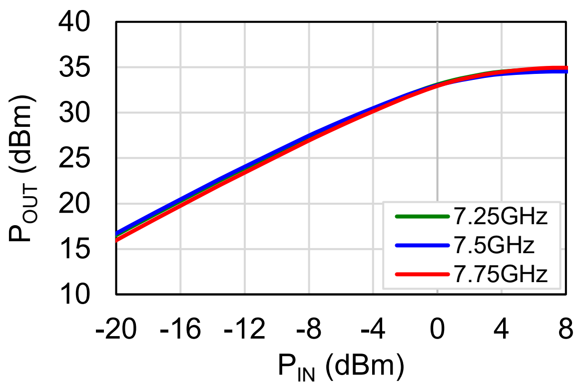
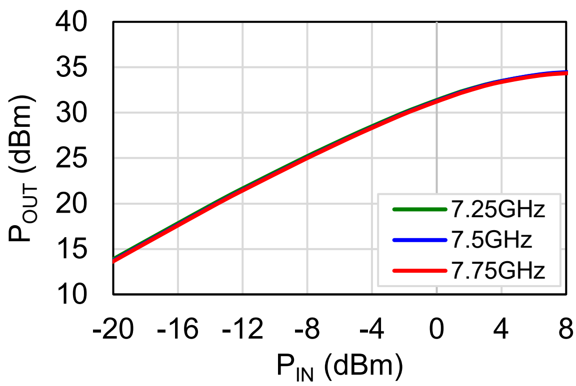
Typical Board Measurements: Large Signal Performance

Test conditions: CW, V_D = 28V, V_G = -3.41V, $T_{backside}$ = 25°C / 100°C

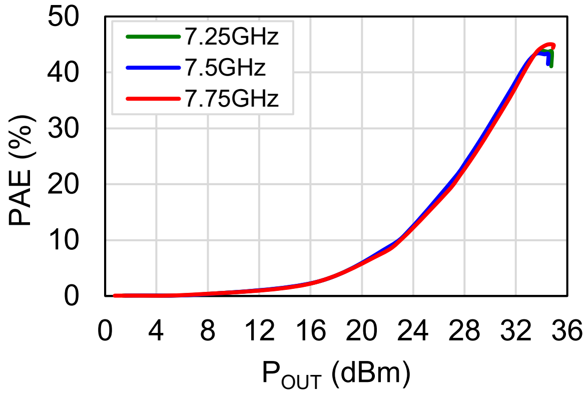
Output power vs. input power at 25°C



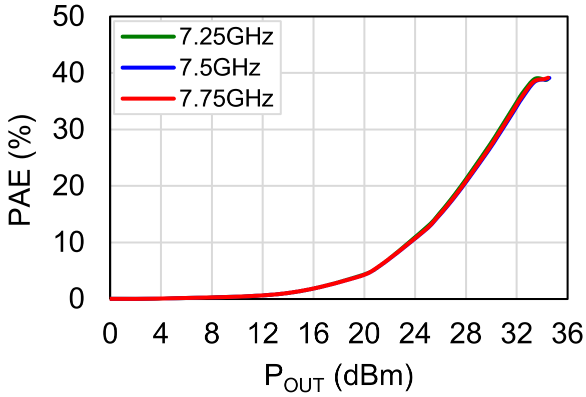
Output power vs. input power at 100°C



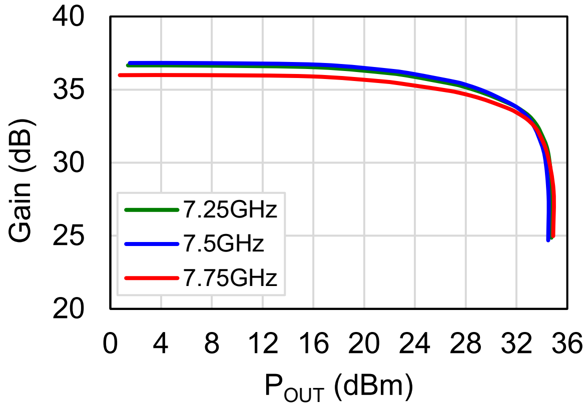
Power Added Efficiency vs. output power at 25°C



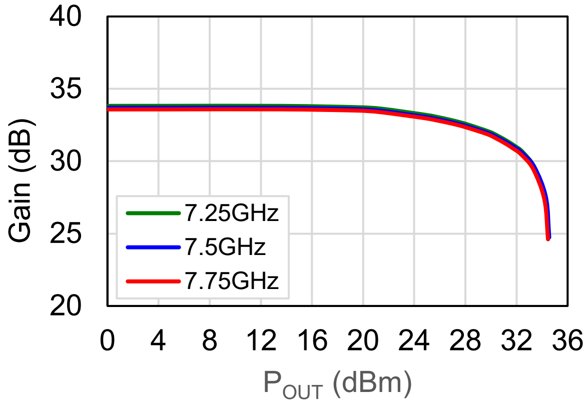
Power Added Efficiency vs. output power at 100°C



Gain vs. output power at 25°C



Gain vs. output power at 100°C



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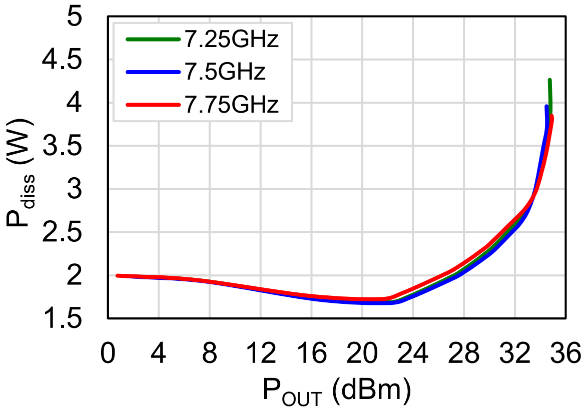
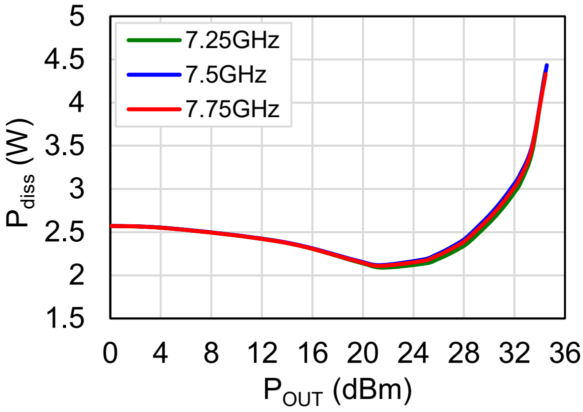
Typical Board Measurements: Large Signal Performance

Test conditions: CW, V_D = 28V, V_G = -3.41V, $T_{backside}$ = 25°C / 100°C

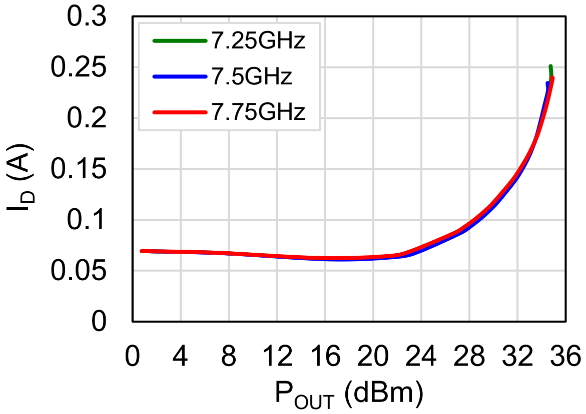
Dissipated power vs. output power at 25°C



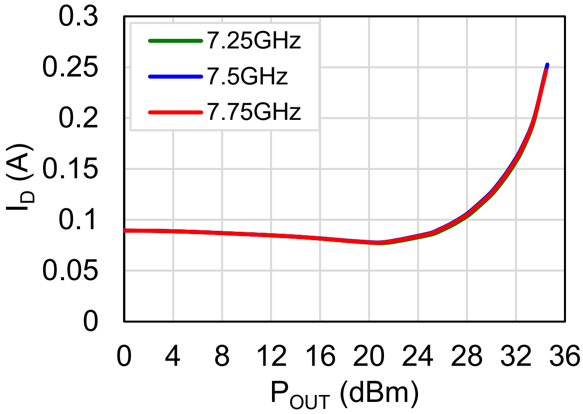
Dissipated power vs. output power at 100°C



Drain current vs. output power at 25°C



Drain current vs. output power at 100°C



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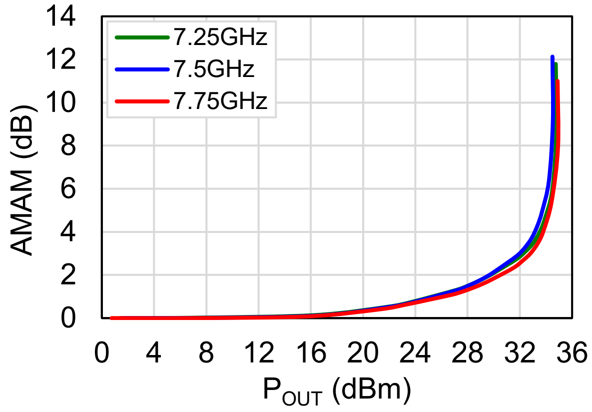
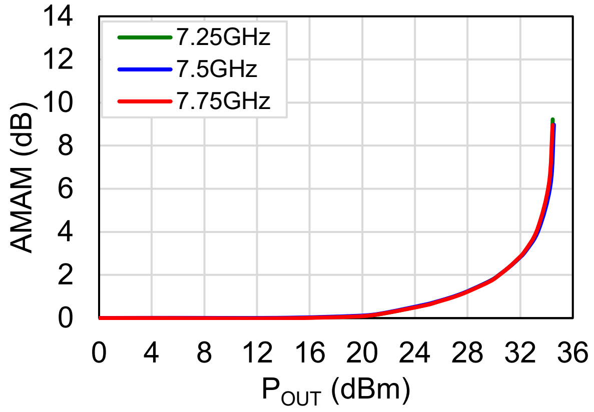
Typical Board Measurements: Large Signal Performance

Test conditions: CW, V_D = 28V, V_G = -3.41V, $T_{backside}$ = 25°C / 100°C

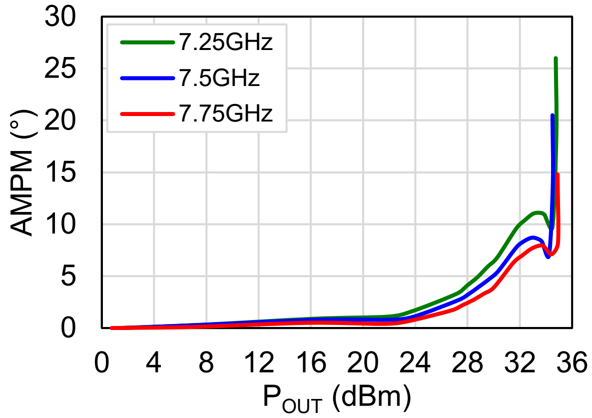
AMAM vs. output power at 25°C



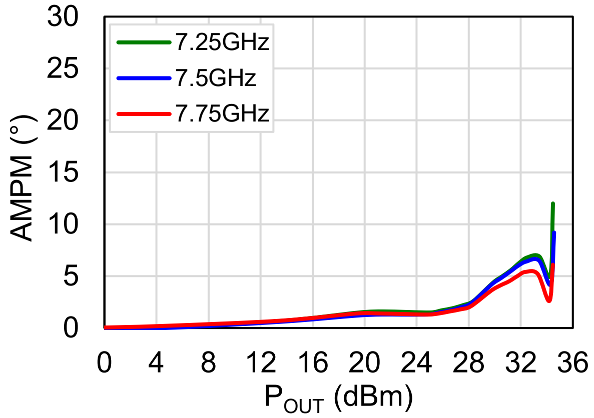
AMAM vs. output power at 100°C



AMPM vs. output power at 25°C



AMPM vs. output power at 100°C



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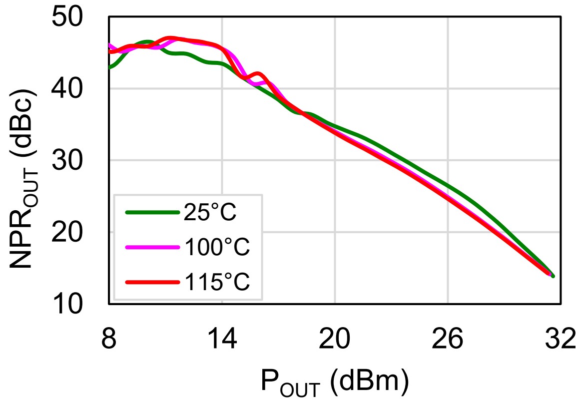
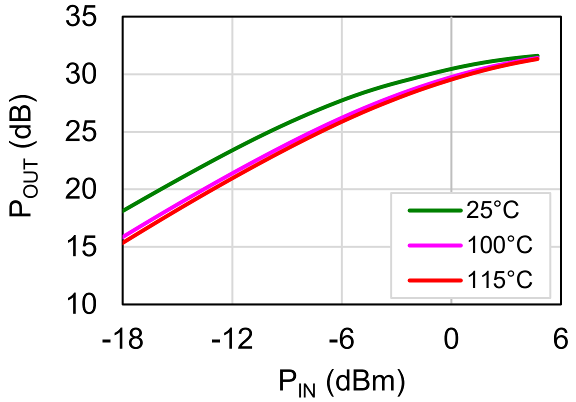
Typical Board Measurements: Noise power ratio

Test conditions: CW, V_D = 28V, V_G = -3.41V, $T_{backside}$ = 25°C / 100°C / 115°C, center frequency = 7.5GHz, BW= 500MHz, Notch=10% Number of tones: 4000

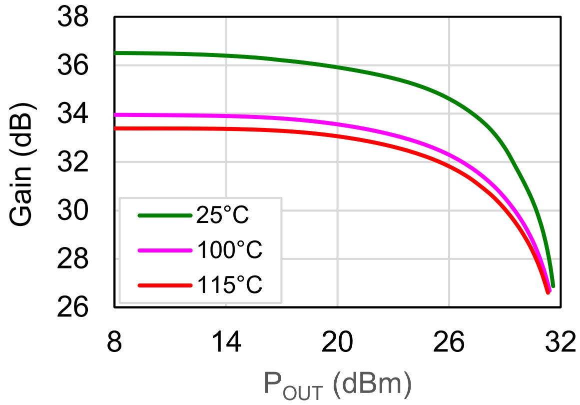
Output noise power ratio vs. output power vs temperature



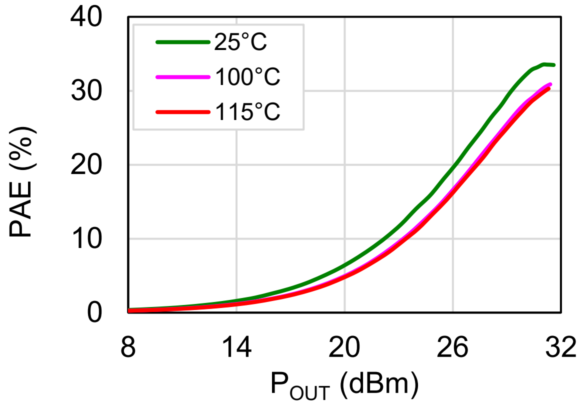
Output power vs. input power vs temperature



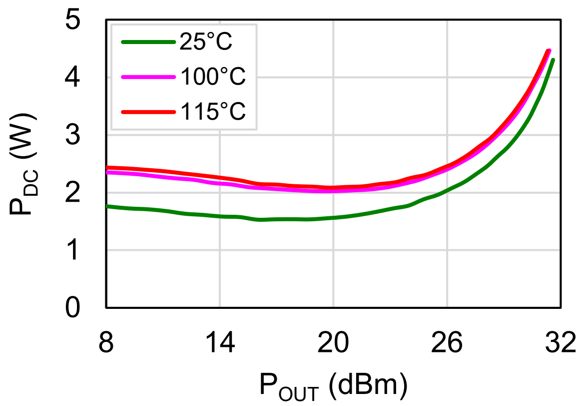
Gain vs. output power vs. temperature



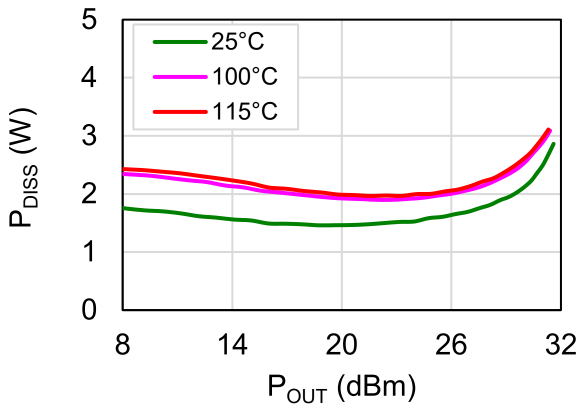
PAE vs. output power vs. temperature



DC power vs. output power vs. temperature



Dissipated power vs. output power vs. temperature



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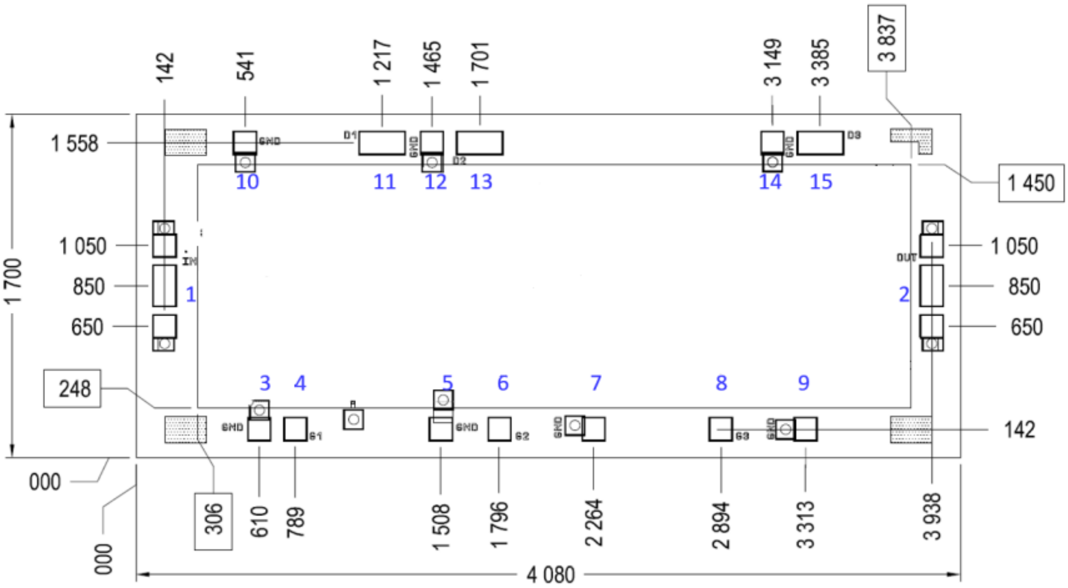
Chip mechanical data



Chip size : 4080 x 1700 µm² +/- 50µm
Chip thickness = 100µm +/- 10µm

Pad	Name	Description	Pad Size (µm²)
1	IN	RF Input	116 x 206
2	OUT	RF Output	116 x 206
3	GND	Ground	116 x 116
4	G1	DC Gate voltage, 1st stage	116 x 116
5	GND	Ground	116 x 116
6	G2	DC Gate voltage, 2nd stage	116 x 116
7	GND	Ground	116 x 116
8	G3	DC Gate voltage, 3rd stage	116 x 116
9	GND	Ground	116 x 116
10	GND	Ground	116 x 116
11	D1	DC Drain voltage, 1st stage	230 x 116
12	GND	Ground	116 x 116
13	D2	DC Drain voltage, 2nd stage	230 x116
14	GND	Ground	116 x 116
15	D3	DC Drain voltage, 3rd stage	230 x 116

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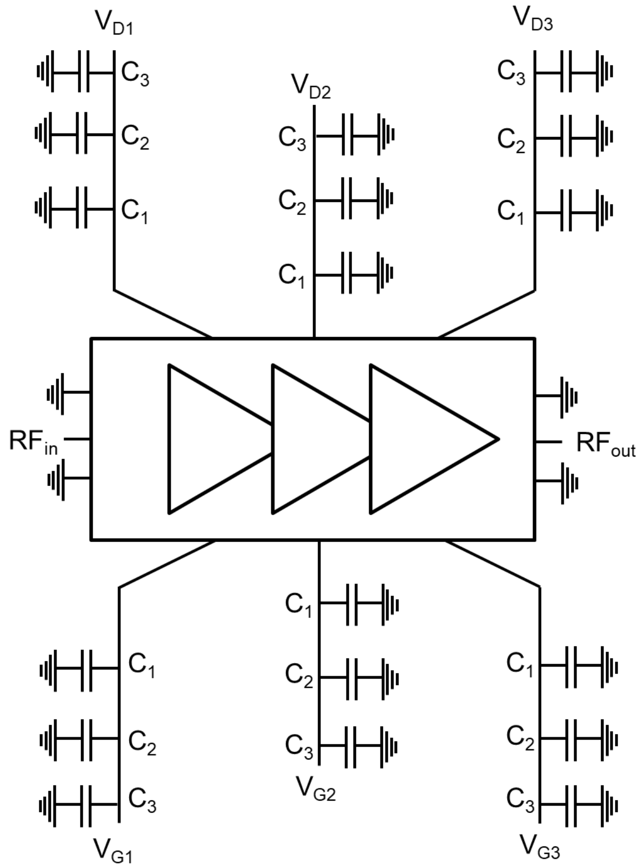
Recommended Assembly Plan



Bill of materials

Component	Value	Description
C_1	120pF	Capacitor 120pF ±10% 50V
C_2	10nF	Capacitor 10nF ±20% 50V
C_3	100nF	1206 SMD Capacitor 100nF ±10% 100V

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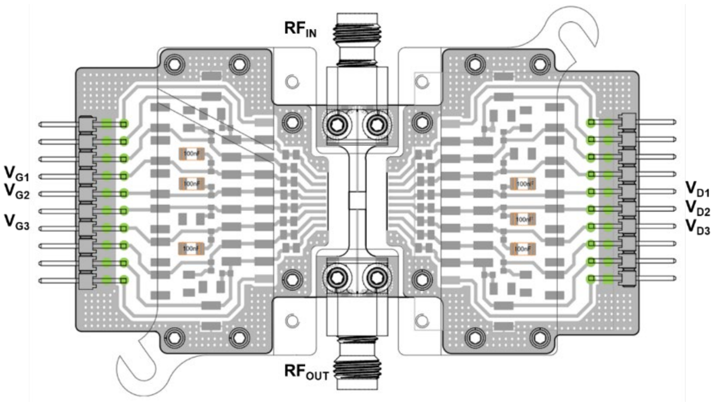
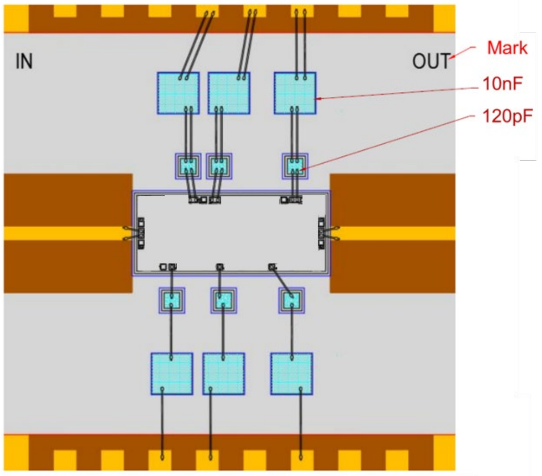
Evaluation Board (EVB)





Three levels of decoupling capacitors have been used: two on the tab, one on the board. The first level is composed of 120pF chip capacitors. The second level is composed of 10nF chip capacitors. The third level is composed of 100nF 1206 SMD capacitors. The first two levels should be as close as possible to the die.

Recommended circuit bonding table

Input / Output	Bonding	External capacitor
RF_{IN} / RF_{OUT}	2 bond wires in parallel with a diameter of 25µm	Not required
Gate pins	Inductance ≤ 1nH (mainly for first decoupling level) ⇒ 1.2mm long wires with a diameter of 25 µm	C1 = 120pF C2 = 10nF C3 = 100nF
Drain pins	.Inductance ≤ 1nH (mainly for first decoupling level) ⇒ 1.2mm long wires with a diameter of 25 µm 2 bond wires in parallel minimum	C1 = 120pF C2 = 10nF C3 = 100nF

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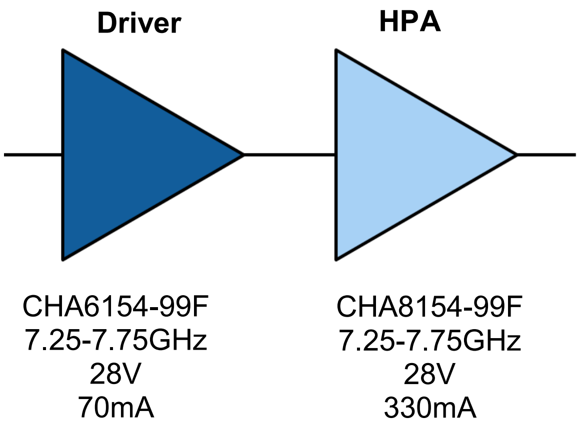
Recommended UMS power chain

The CHA6154-99F is recommended with the CHA8154-99F as HPA.
The complete chain exhibits a gain > 65dB.
For more information about the CHA8154-99F, visit our website www.ums-rf.com



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Recommended reflow process assembly

Refer to the application note AN0001 available at https://www.ums-rf.com for die attach.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at https://www.ums-rf.com.

Recommended ESD management

Refer to the application note AN0020 available at https://www.ums-rf.com for ESD sensitivity and handling recommendations for the UMS package products.

Recommended Evaluation board assembly

Refer to the application note AN0030 available at https://www.ums-rf.com Evaluation board.

Ordering Information

Chip form :	CHA6154-99F/00
Evaluation board:	EVB-CHA6154-99F

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