

36-43.5GHz Power Amplifier

GaAs Monolithic Microwave IC in bare die

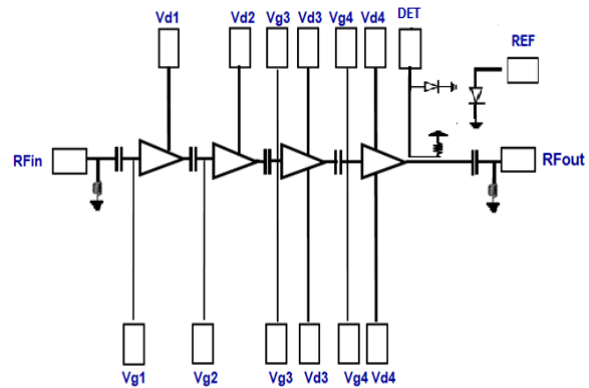
Description

The CHA5659-98F is a four stage monolithic GaAs High Power Amplifier producing 1.3 W output power. It is highly linear, with possible gain control and integrates a power detector. ESD protections are included.

It is designed for Point To Point Radio or Q-band SatCom applications.

The CHA5659-98F is recommended with the CHA3398-98F as a driver.

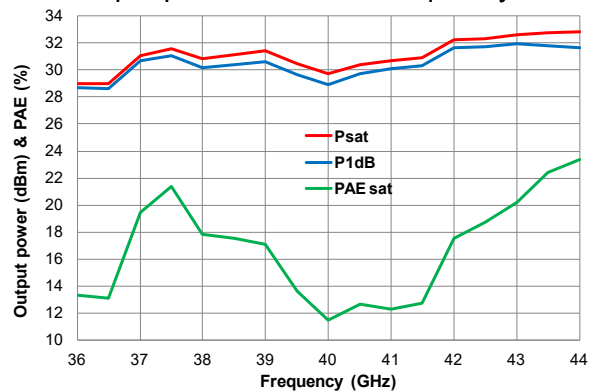
The circuit is manufactured with a pHEMT process.



Main Features

- Broadband performances: 36 - 43.5GHz
- 31dBm saturated power
- 38dBm OIP3
- 22dB gain
- Gain control up to 15dB
- DC bias: $V_d = 6.0V @ I_{dq} = 0.8A$
- Chip size 3.60 x 3.00 x 0.07mm

Output power & PAE vs frequency



Main Electrical Characteristics

$T_{backside} = +25^{\circ}C$

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	36.0		43.5	GHz
Gain	Linear Gain		22		dB
Psat	Saturated output power		31		dBm
OIP3	Output IP3		38		dBm

Specifications

$T_{\text{backside}} = +25^{\circ}\text{C}$, $V_d = +6.0\text{V}$

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	36.0		43.5	GHz
Gain	Small Signal Gain		22		dB
ΔG	Gain variation in temperature		± 0.04		dB/ $^{\circ}\text{C}$
Psat	Saturated Output Power		31		dBm
OIP3	Output IP3		38		dBm
P1dB	Pout at 1dB of compression		30		dBm
PAE	PAE at saturation		15		%
CG	Gain control range		15		dB
Rlin	Input Return Loss		8		dB
Rlout	Output Return Loss		10		dB
Dr	Detection dynamic range(for output power detection up to Psat)		30		dB
Vdetect	Voltage detection $V_{\text{REF}} - V_{\text{DET}}$ up to Psat		20 to 2000		mV
Vg	DC gate Voltage		-0.65		V
Idq	Total drain current		0.8		A

These values are representative of on-board measurements.

Absolute Maximum Ratings ^{(1), (2)} $T_{\text{backside}} = +25^{\circ}\text{C}$

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	8	V
Id	Drain bias current at saturated output power	1900	mA
Vg	Gate bias voltage	-2 to 0	V
Pin	Maximum Input Power	+15	dBm

⁽¹⁾ Operation of this device above anyone of these parameters may cause permanent damage.⁽²⁾ These are stress rating only, and functional operation of the devices at these conditions is not implies.**Recommended Operating Ratings** ^{(3), (4)}

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	5 to 6	V
Id	Drain bias current	640 to 800	mA
Vg	Gate bias voltage	-2 to 0	V
T_{backside}	Operating temperature range	-40 to 85	$^{\circ}\text{C}$
T_j	Maximum Junction temperature	175	$^{\circ}\text{C}$

⁽³⁾ Electrical performances are defined for specified test conditions⁽⁴⁾ Electrical performances are not guaranteed over all recommended operating conditions**Temperature Range**

T_{backside}	Operating temperature range	-40 to +95	$^{\circ}\text{C}$
T_{stg}	Storage temperature range	-55 to +150	$^{\circ}\text{C}$

Typical Bias Conditions $T_{\text{backside}} = +25^{\circ}\text{C}$

Symbol	Parameter	Values	Unit
Vd1	DC Drain voltage 1 st stage	6V	V
Vd2	DC Drain voltage 2 nd stage	6V	V
Vd3	DC Drain voltage 3 rd stage	6V	V
Vd4	DC Drain voltage 4 th stage	6V	V
Vg1	DC Gate voltage 1 st stage	-0.65	V
Vg2	DC Gate voltage 2 nd stage	-0.65	V
Vg3	DC Gate voltage 3 rd stage	-0.65	V
Vg4	DC Gate voltage 4 th stage	-0.65	V

Device thermal performances

All the figures given in this section are obtained assuming that the chip device is only cooled down by conduction through the package thermal pad (no convection mode considered).

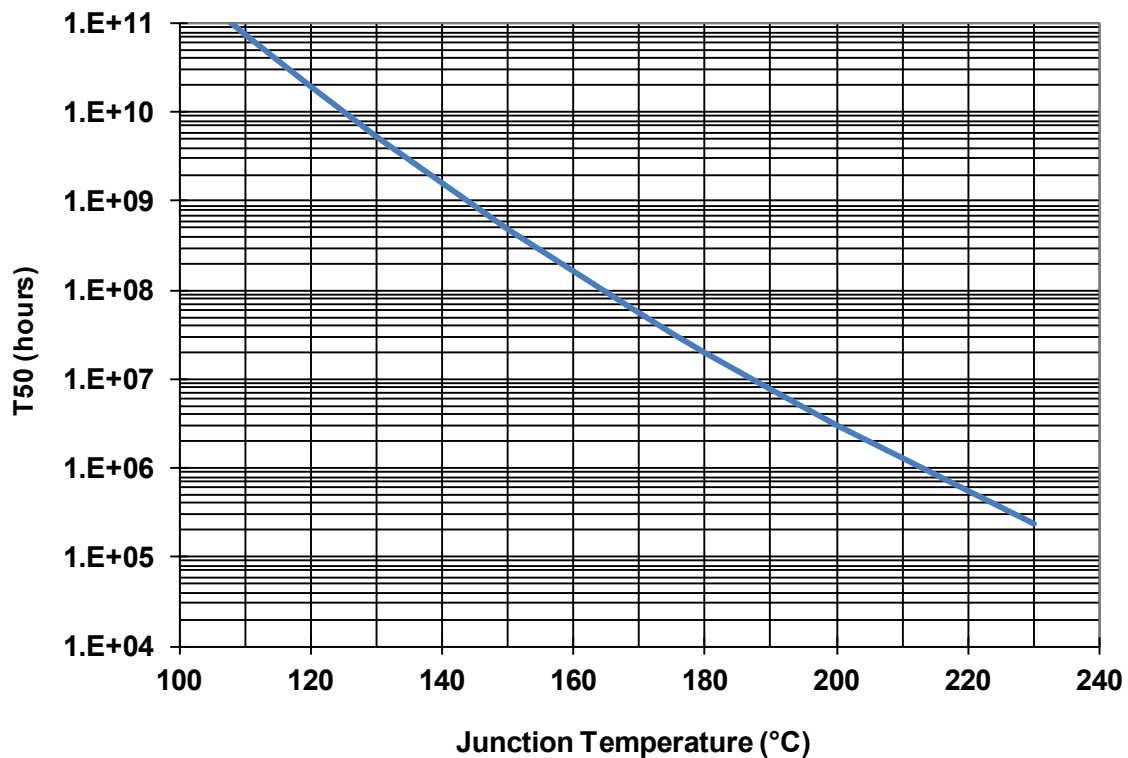
The temperature is monitored at the chip back-side interface ($T_{backside}$).

The system maximum temperature must be adjusted in order to guarantee that $T_{junction}$ remains below the maximum value specified in the Absolute Maximum Ratings table.

So, the system PCB must be designed to comply with this requirement.

Parameter	Biasing conditions	$T_{junction}$ (°C)	R_{TH} (°C/W)	T_{50} (hours)
$R_{TH}^{(1)}$ Thermal Resistance (Back of the chip)	Vd= 6V Idq = 800mA Pdiss= 4.8W	170	17.8	5.3E+07
$R_{TH}^{(1)}$ Thermal Resistance (Back of the chip)	Vd= 5V Idq = 640mA Pdiss= 3.2W	125	12.5	9.0E+09

⁽¹⁾ Assuming 85°C $T_{backside}$



Typical on-wafer Sij parameters (Pulsed mode)T_{backside} = +25°C, V_d = +6.0V, I_d = 800mA, Pulse width = 25µs, Duty cycle = 10%

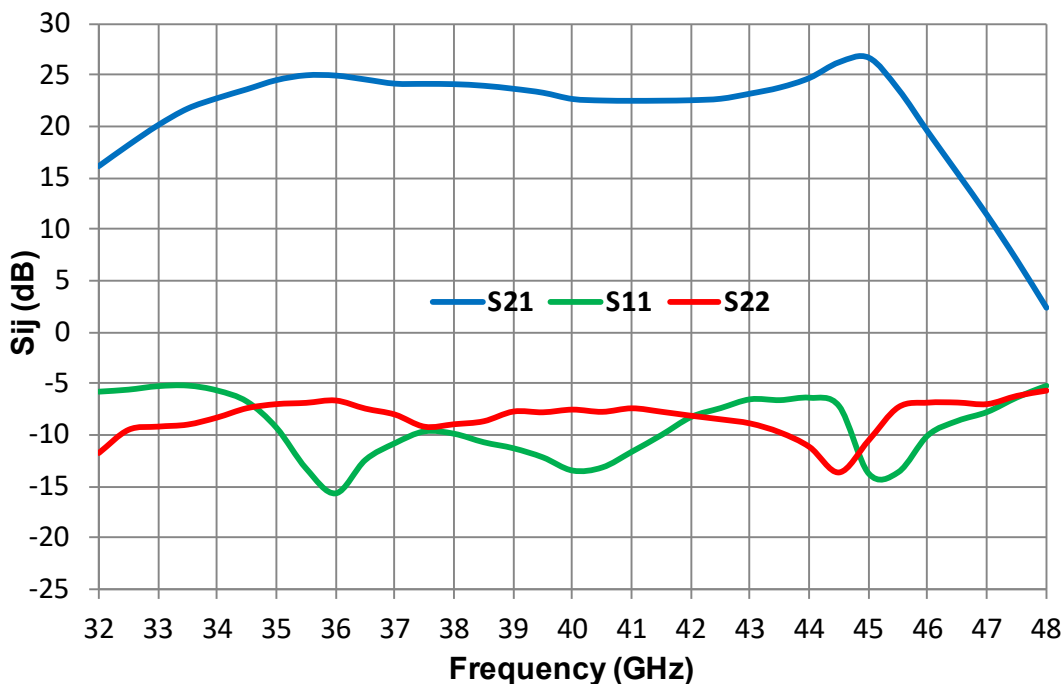
Freq (GHz)	S11 (dB)	PhS11 (°)	S12 (dB)	PhS12 (°)	S21 (dB)	PhS21 (°)	S22 (dB)	PhS22 (°)
5	-0.6	138.1	-77.6	-84	-92.5	129.1	-0.2	164.4
6	-0.7	124.1	-80.1	99.6	-72.7	-61.7	-0.3	160.7
7	-1.1	103	-90.3	61.3	-59.4	-79.1	-0.3	156.6
8	-1.7	68.1	-80.7	-44	-45.7	-109.1	-0.4	151.8
9	-2.8	7.6	-87.2	-163.2	-34.5	-168.6	-0.6	145.5
10	-2.6	-67.9	-86.5	177.9	-25.6	129.5	-1	136.6
11	-1.9	-119.5	-73	-128.7	-17.3	62.6	-2	120.5
12	-1.6	-149.4	-65.2	-110.2	-9.1	-21.5	-7.7	76.4
13	-1.7	-167.8	-55.8	-160	-6.5	-134.5	-5.1	-137.1
14	-2	-179.7	-56.2	160.2	-9.8	143.6	-1.2	-176.8
15	-2.2	171.6	-56.4	110.6	-13.2	78.2	-0.6	167.3
16	-2.4	165.3	-57.7	92	-16.9	30.3	-0.5	157.7
17	-2.4	159.6	-56.6	49	-20.9	-5.6	-0.5	151
18	-2.3	153.7	-58.3	22.3	-23.5	-28.7	-0.4	145
19	-2.3	147.7	-62	-45.8	-24.7	-52.8	-0.5	139.4
20	-2.4	142	-67.5	166.1	-26.1	-72.9	-0.6	133.5
21	-2.4	135.7	-65.7	132.3	-27	-95.1	-0.6	127.5
22	-2.5	129	-58.7	83.6	-28.5	-104.7	-0.6	121.2
23	-2.7	122.9	-60.9	67.9	-27	-100.7	-0.7	114.7
24	-2.7	115.8	-60.6	34.6	-22.6	-109.5	-0.8	106.6
25	-2.7	108.4	-76.2	95.1	-18.1	-126.1	-0.9	97.7
26	-3	99.9	-58.4	19.3	-13.9	-154.3	-1	87.1
27	-3.2	90.6	-56.4	21.2	-9.9	-179	-1.3	73.6
28	-3.2	81	-57.1	-27.8	-4.4	152.8	-1.5	56.4
29	-3.4	69.6	-54.6	-28.9	1.1	116	-2.3	34.1
30	-3.6	57.2	-54.1	-29.3	7.2	73.3	-4	2.9
31	-3.8	43.5	-58.6	-47.7	13.2	21.4	-7	-42.1
32	-4.2	28.7	-52.4	-39.3	18.9	-43.1	-12	-108.4
33	-4.8	15.7	-51.4	-64	23	-114.3	-16.8	177.4
34	-5.3	4	-54.3	-93.7	25.4	169.1	-20.4	126.4
35	-5.3	-13.2	-51.2	-96.8	25.9	93.6	-21.4	135.1
36	-5.5	-28.1	-52	-118.8	25.9	29.1	-21.1	114.7
37	-6.4	-46.5	-59.7	178.5	26	-38.8	-20.5	120.2
38	-7.3	-57.2	-58.5	139.4	25.5	-97.5	-20.7	108.3
39	-8.4	-70	-71.3	-131.3	25.2	-157.6	-20.8	100.9
40	-9.9	-80.9	-57.4	9.4	25.4	141.4	-19.1	93.6
41	-11.7	-84.3	-61.6	130.4	25.3	78	-16.7	73.3
42	-14.5	-78.7	-58.6	-45.4	25.7	12.3	-13.4	48.5
43	-14.3	-62.6	-58.6	88.4	25.8	-61.7	-9.7	27.9
44	-14.3	-35.4	-56.5	73.4	25.8	-150.1	-5	-2.6
45	-6.5	-27.2	-60.1	-99.9	20.5	110.3	-3.5	-41.2

Typical Board Measurements (CW)

$T_{\text{backside}} = +25^{\circ}\text{C}$, $V_d = +6\text{V}$, $I_{dq} = 800\text{mA}$ & $V_d = +5\text{V}$, $I_{dq} = 640\text{mA}$
 Measurement performed in the access plans of the die.

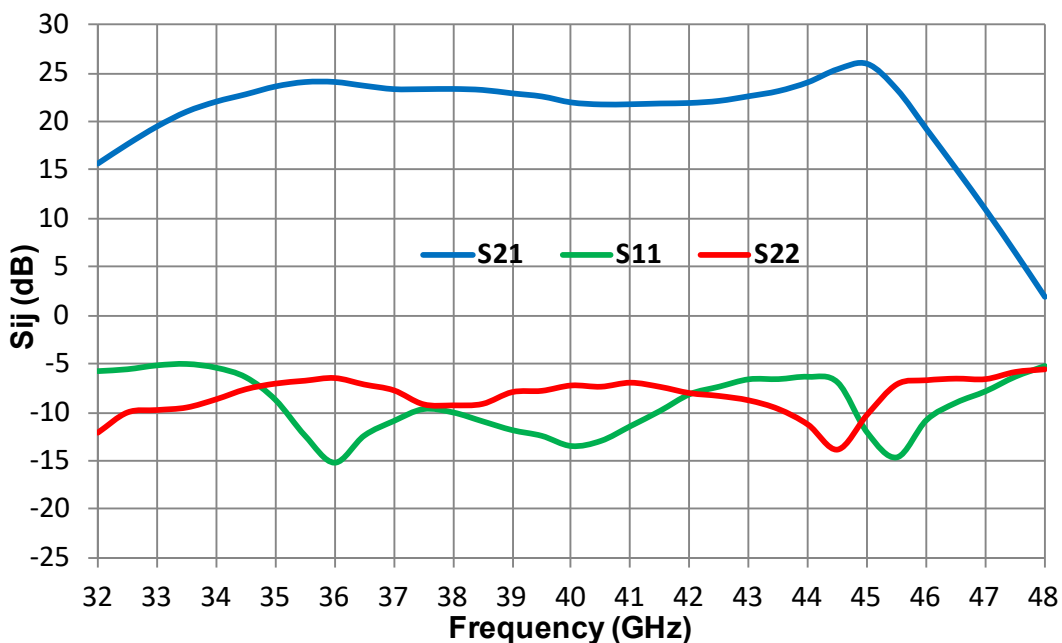
Gain & Return Loss vs. Frequency

$V_d = +6\text{V}$, $I_{dq} = 800\text{mA}$



Gain & Return Loss vs. Frequency

$V_d = +5\text{V}$, $I_{dq} = 640\text{mA}$

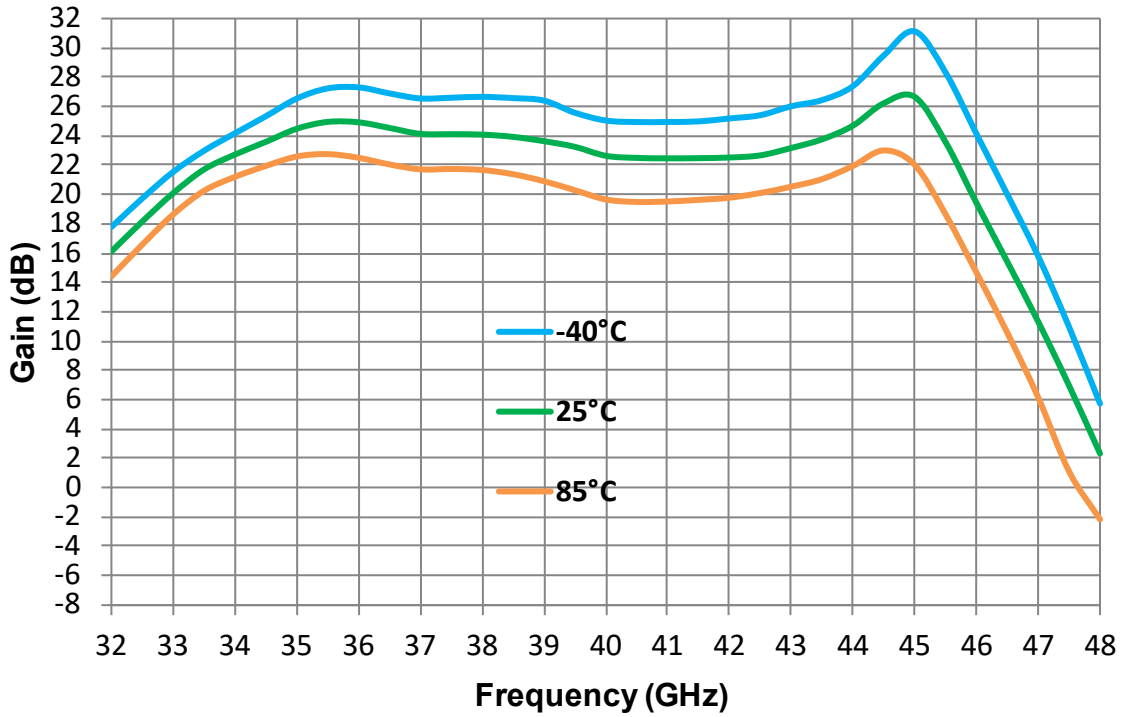


Typical Measurements on a probe compatible Board (CW)

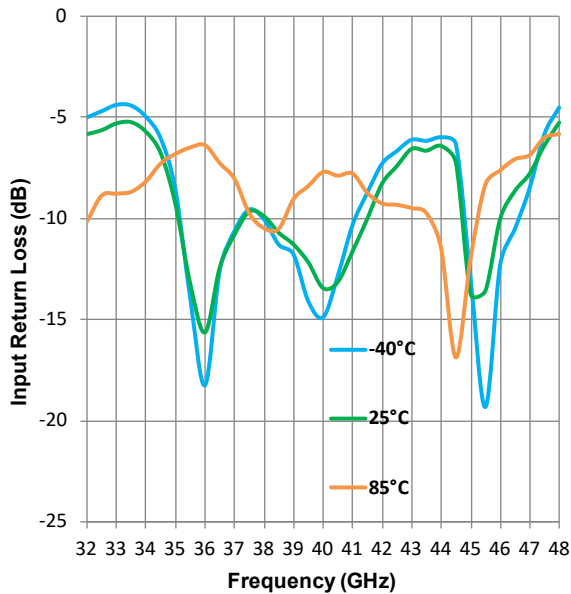
T_{backside} = +25°C, V_d = +6.0V, I_{dq} = 800mA

Measurement performed in the access plans of the die.

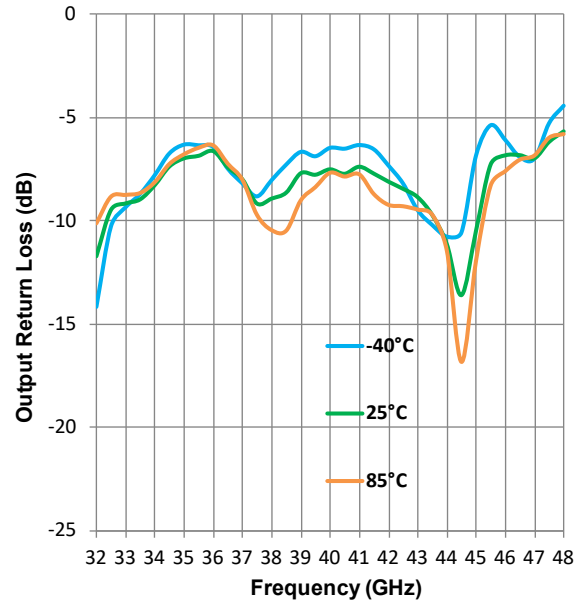
Gain vs. Frequency in Temperature



Input Return Loss vs. Frequency in Temperature



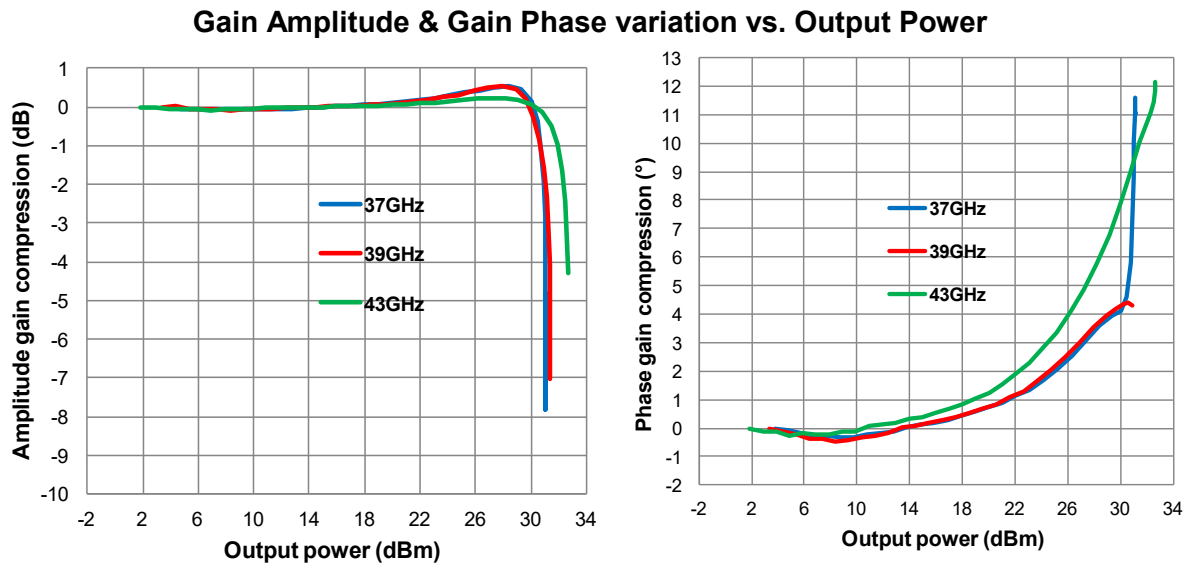
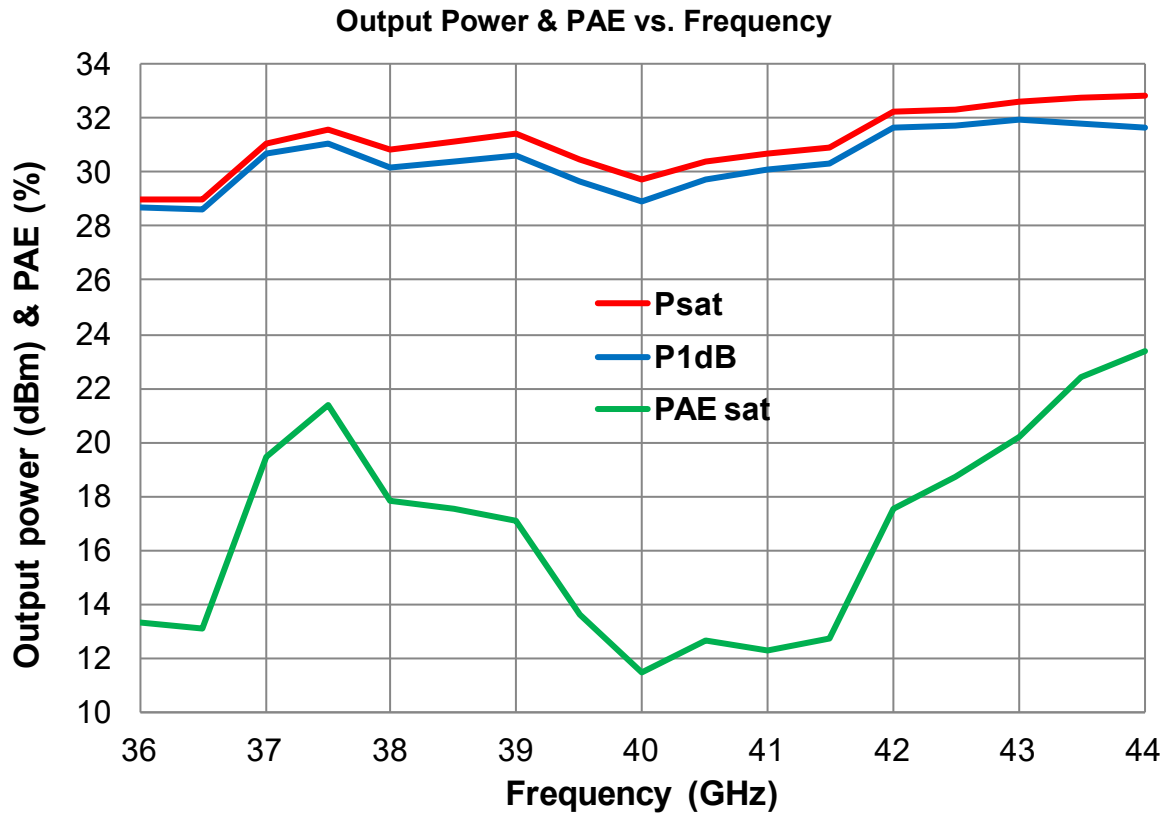
Output Return Loss vs. Frequency in Temperature



Typical Board Measurements (CW)

$T_{\text{backside}} = +25^{\circ}\text{C}$, $V_d = +6.0\text{V}$, $I_{dq} = 800\text{mA}$

Measurement performed in the access plans of the die.

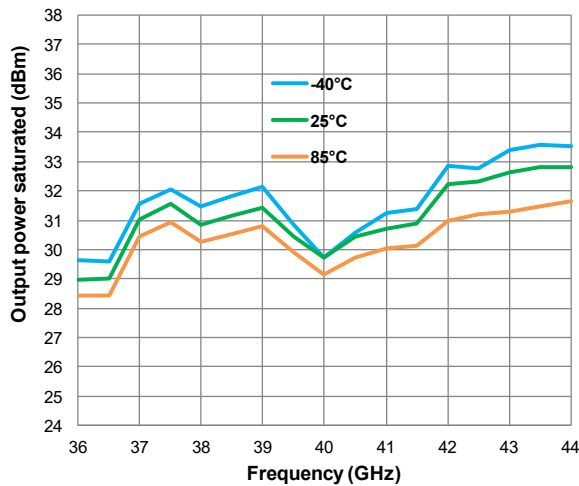


Typical Board Measurements (CW)

$T_{\text{backside}} = +25^{\circ}\text{C}$, $V_d = +6.0\text{V}$, $I_{dq} = 800\text{mA}$ & $V_d = +5\text{V}$, $I_{dq} = 640\text{mA}$

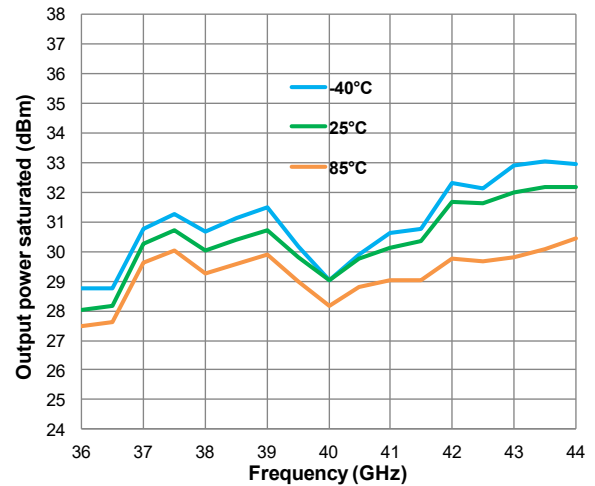
Saturated Power vs. Frequency in Temperature

$V_d = +6\text{V}$, $I_{dq} = 800\text{mA}$



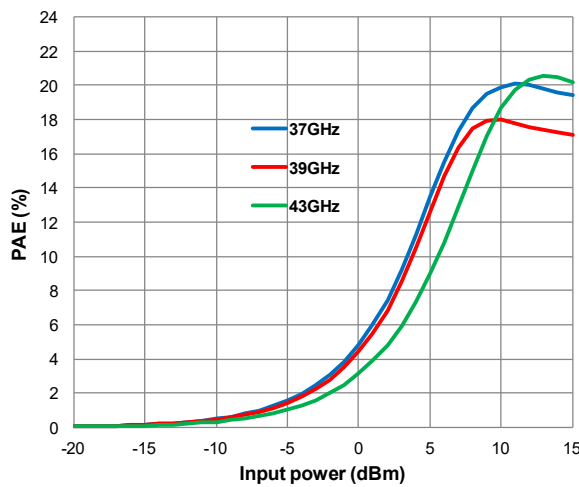
Saturated Power vs. Frequency in Temperature

$V_d = +5\text{V}$, $I_{dq} = 640\text{mA}$



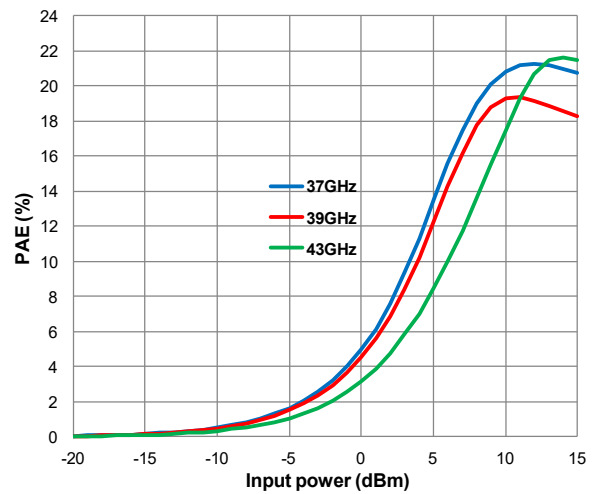
PAE vs. Input Power

$V_d = +6\text{V}$, $I_{dq} = 800\text{mA}$



PAE vs. Input Power

$V_d = +5\text{V}$, $I_{dq} = 640\text{mA}$



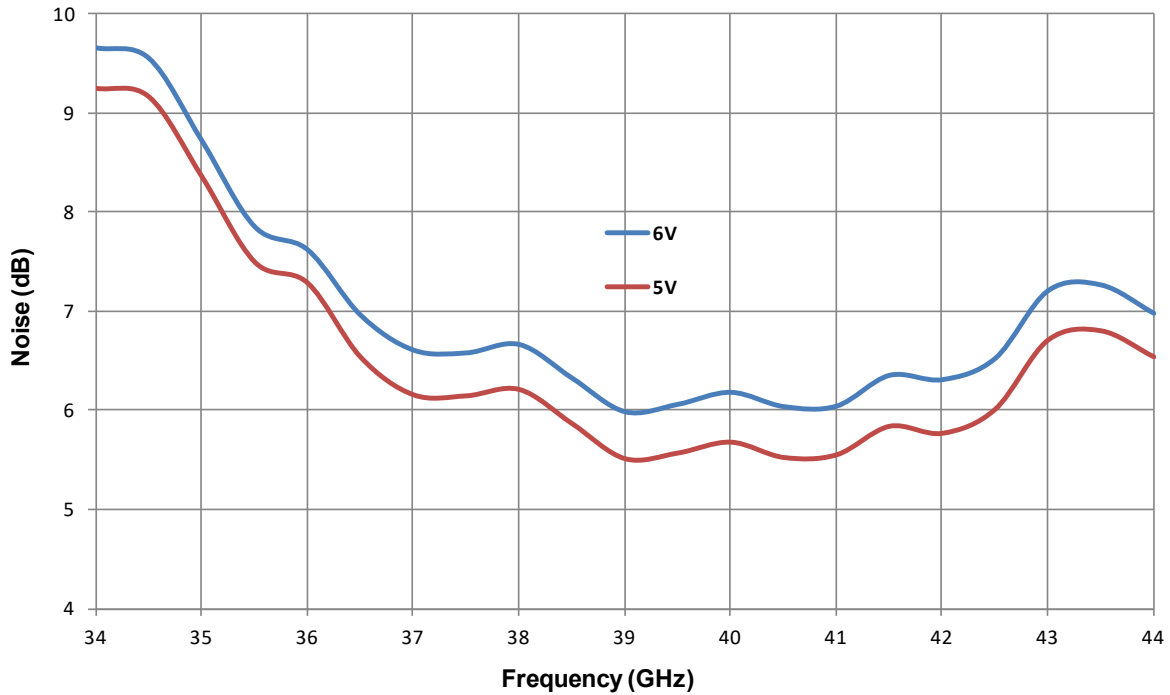
Typical Board Measurements (CW)

$T_{\text{backside}} = +25^{\circ}\text{C}$, $V_d = +6.0\text{V}$, $I_{dq} = 800\text{mA}$ & $V_d = +5\text{V}$, $I_{dq} = 640\text{mA}$

Noise Figure vs. Frequency

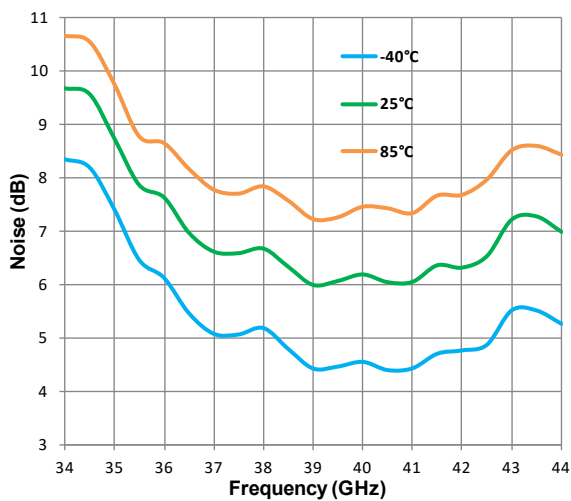
$V_d = +6\text{V}$, $I_{dq} = 800\text{mA}$

$V_d = +5\text{V}$, $I_{dq} = 640\text{mA}$



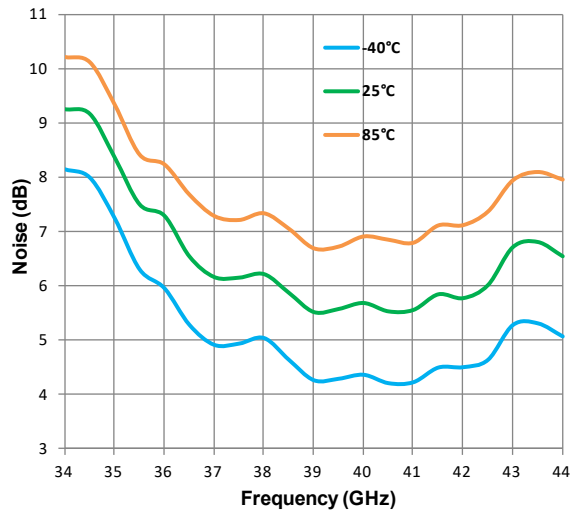
Noise Figure vs. Frequency in Temperature

$V_d = +6\text{V}$, $I_{dq} = 800\text{mA}$



Noise Figure vs. Frequency in Temperature

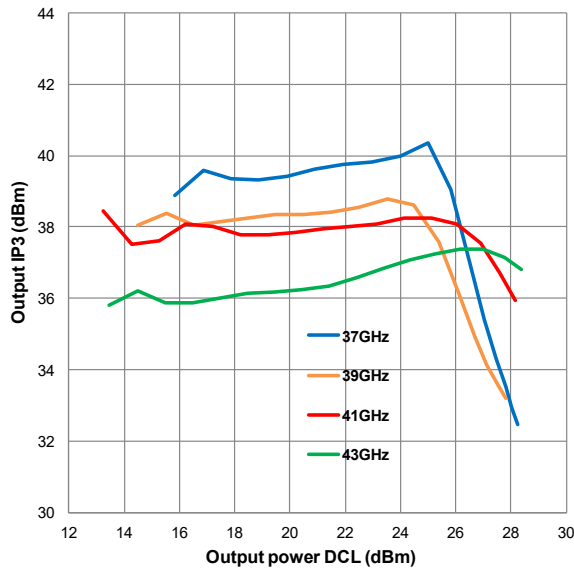
$V_d = +5\text{V}$, $I_{dq} = 640\text{mA}$



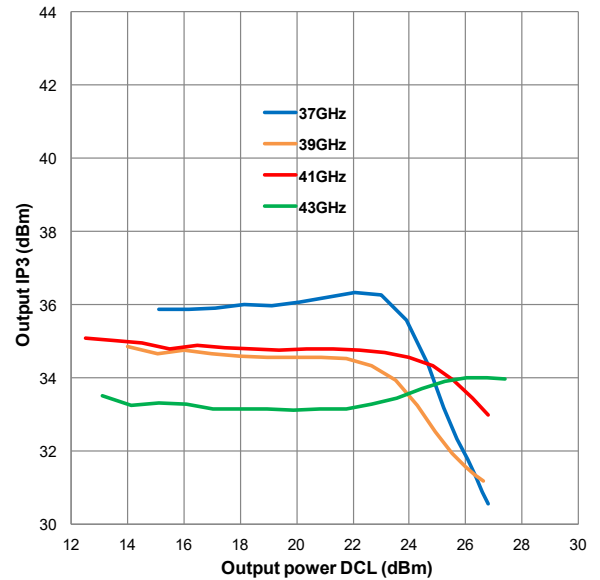
Typical Board Measurements (CW)

$T_{\text{backside}} = +25^{\circ}\text{C}$, $V_d = +6.0\text{V}$, $I_{dq} = 800\text{mA}$ & $V_d = +5\text{V}$, $I_{dq} = 640\text{mA}$

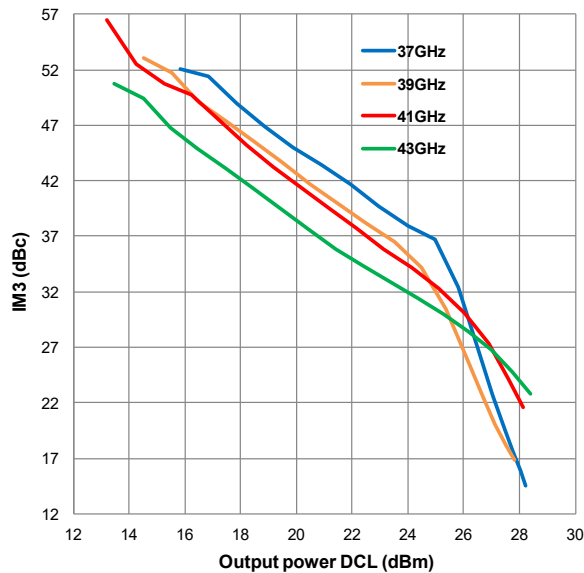
Output IP3 vs. Output Power
 $V_d = +6\text{V}$, $I_{dq} = 800\text{mA}$



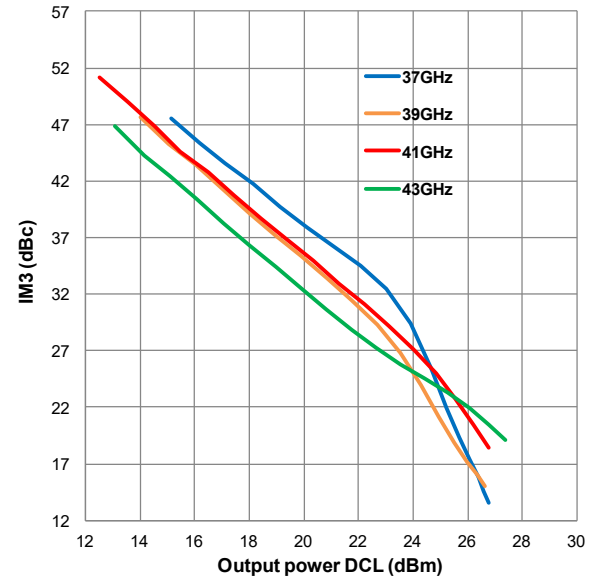
Output IP3 vs. Output Power
 $V_d = +5\text{V}$, $I_{dq} = 640\text{mA}$



Output IM3 vs. Output Power
 $V_d = +6\text{V}$, $I_{dq} = 800\text{mA}$



Output IM3 vs. Output Power
 $V_d = +5\text{V}$, $I_{dq} = 640\text{mA}$

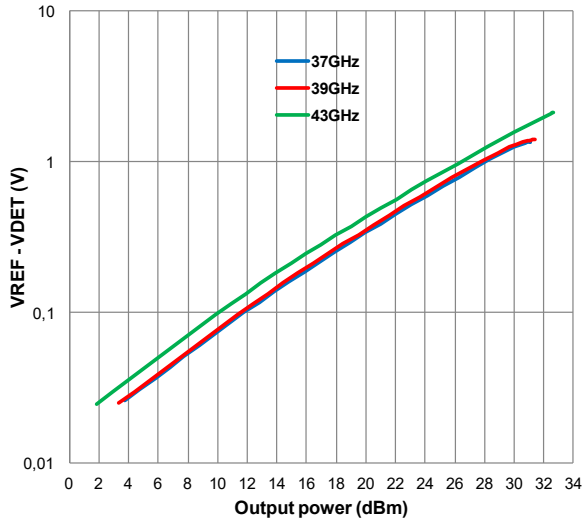


Typical Board Measurements (CW)

$T_{\text{backside}} = +25^{\circ}\text{C}$, $V_d = +6.0\text{V}$, $I_{dq} = 800\text{mA}$ & $V_d = +5\text{V}$, $I_{dq} = 640\text{mA}$

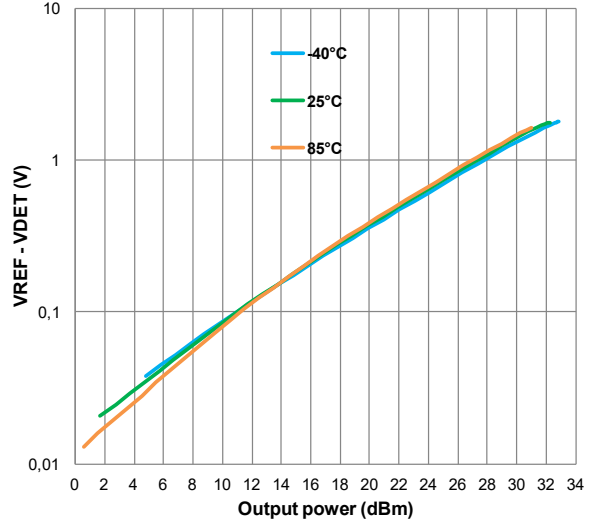
Power Detector vs. Output Power

$V_d = +6\text{V}$, $I_{dq} = 800\text{mA}$



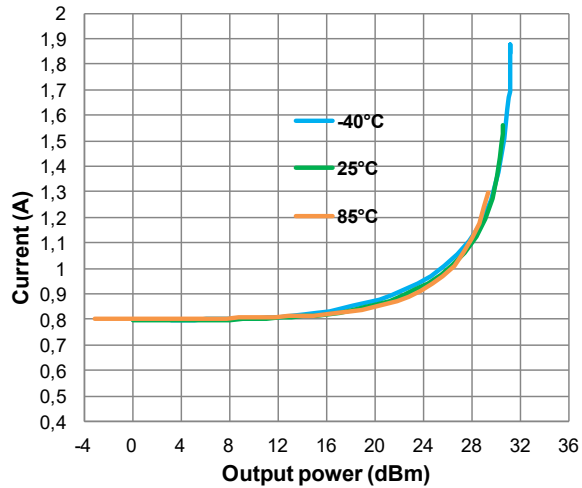
Power Detector vs. Output Power & Temperature at 42GHz

$V_d = +6\text{V}$, $I_{dq} = 800\text{mA}$



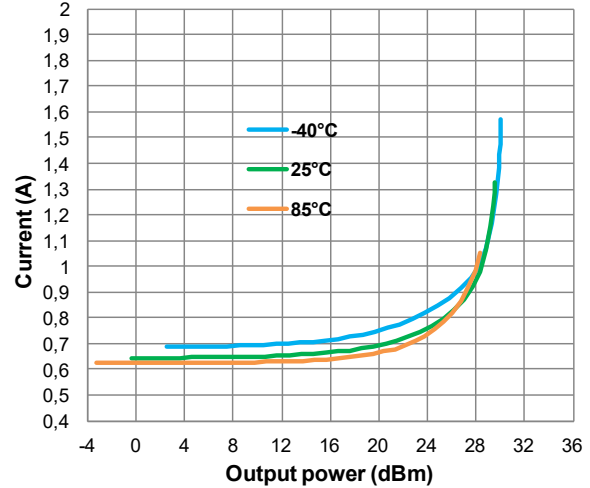
Total Drain Current vs. Output Power at 42GHz

$V_d = +6\text{V}$, $I_{dq} = 800\text{mA}$

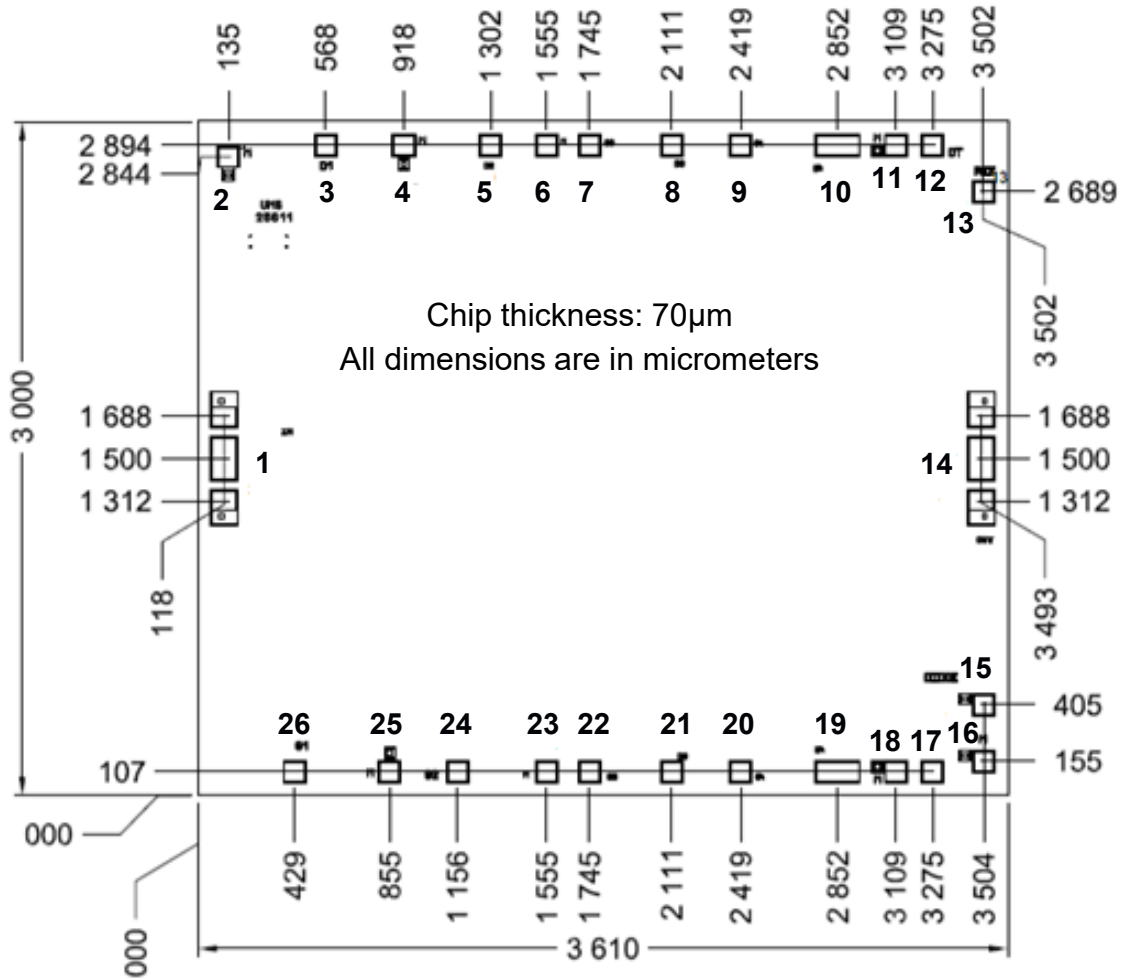


Total Drain Current vs. Output Power at 42GHz

$V_d = +5\text{V}$, $I_{dq} = 640\text{mA}$



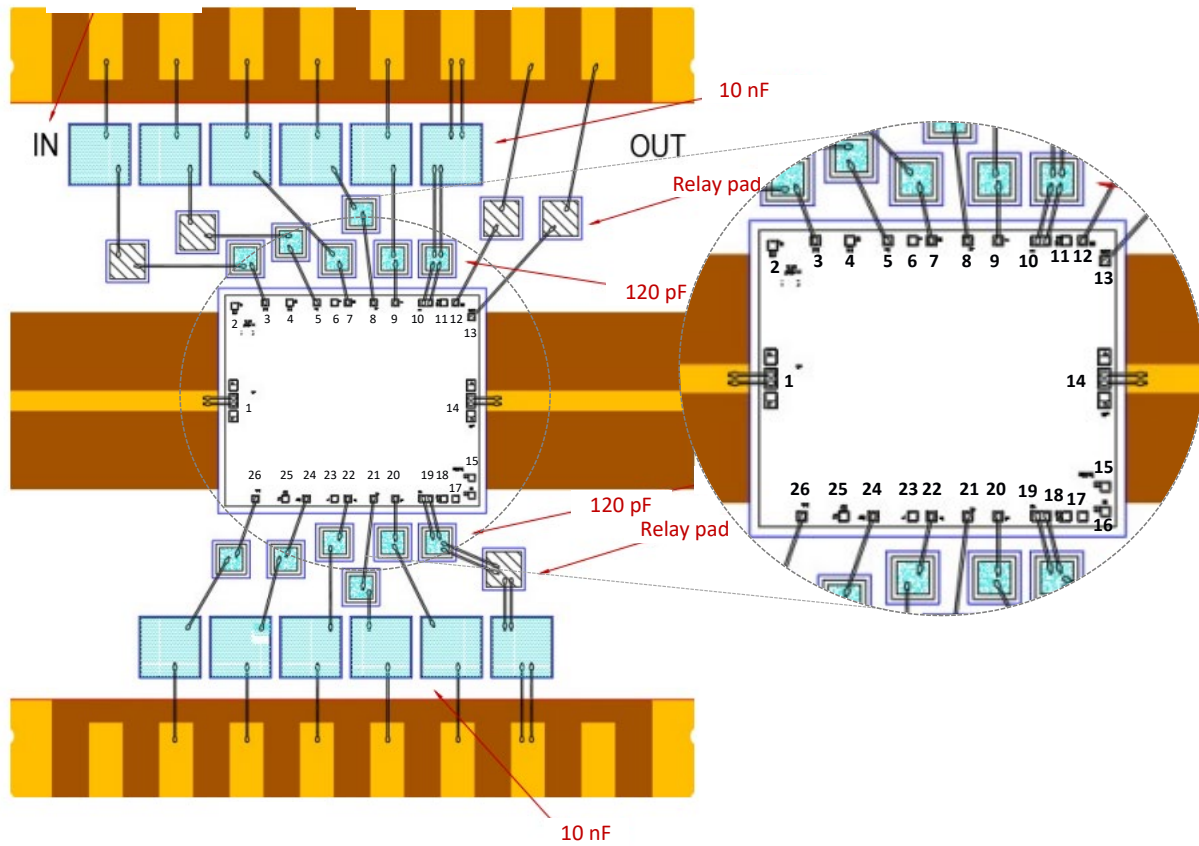
Mechanical data



DC pad size: 83µm x 83 µm (BCB opening)
RF pad size: 105µm x 186 µm (BCB opening)

PAD Number	Name	Description
1	RF IN	Input RF port
14	RF OUT	Output RF port
26	Vg1	DC Gate voltage 1 st stage
3	Vd1	DC Drain voltage 1 st stage
24	Vg2	DC Gate voltage 2 nd stage
5	Vd2	DC Drain voltage 2 nd stage
7, 22	Vg3	DC Gate voltage 3 rd stage
8, 21	Vd3	DC Drain voltage 3 rd stage
9, 20	Vg4	DC Gate voltage 4 th stage
10, 19	Vd4	DC Drain voltage 4 th stage
12	DET	Voltage detection
13	REF	Voltage reference
2, 4, 6, 11, 15, 16, 18, 23, 25	GND	Ground pad

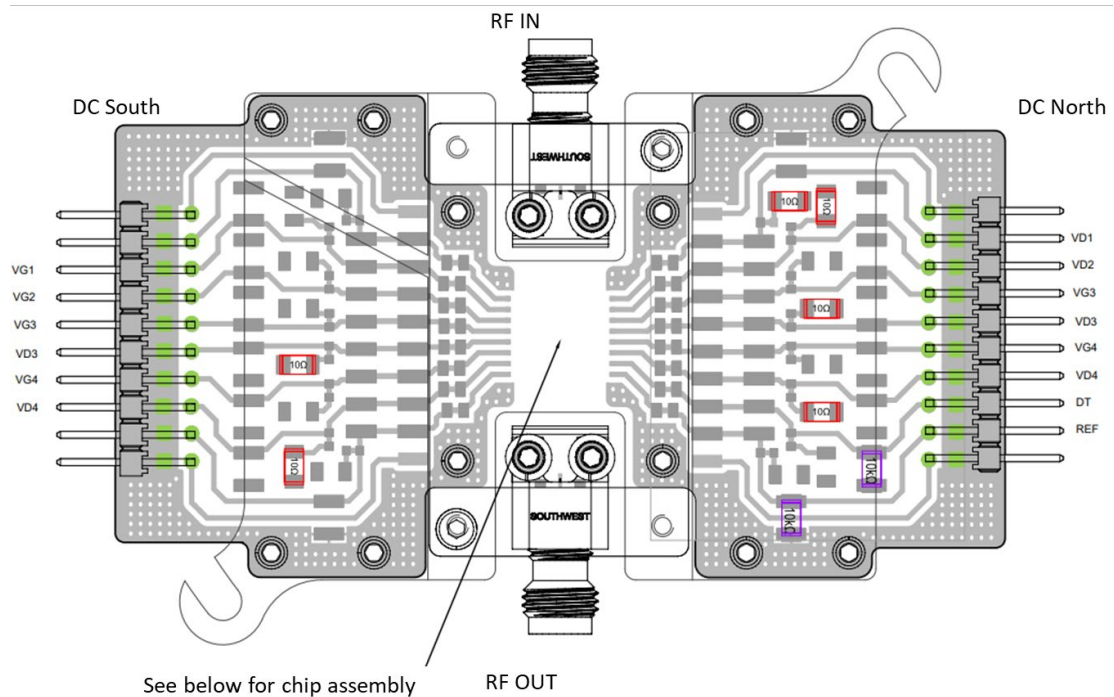
Recommended assembly plan



Decoupling capacitors: 120pF, 10nF & 1 μ F (on gate & drain access)

Note: Supply feed should be bypassed. 25 μ m diameter gold wire is to be preferred.

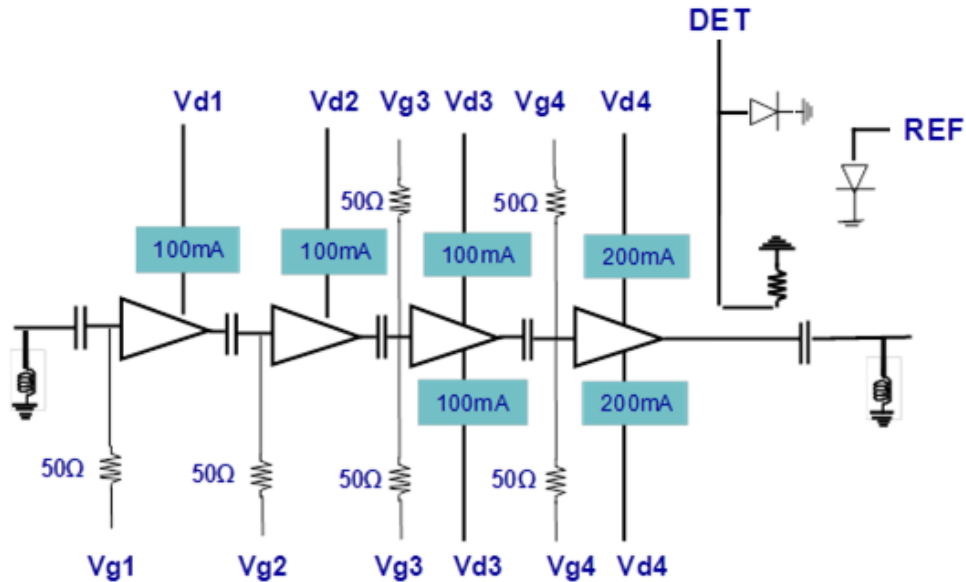
Evaluation board



Three levels of decoupling capacitors have been used: two on the tab, one on the board. The first level is composed of 120pF chip capacitors. The second level is composed of 10nF chip capacitors. The third level is composed of 1µF capacitors. The first two levels should be as close as possible to the die.

DC Schematic

HPA : 6V, 800mA



Biasing procedure

Device Power Up instructions:

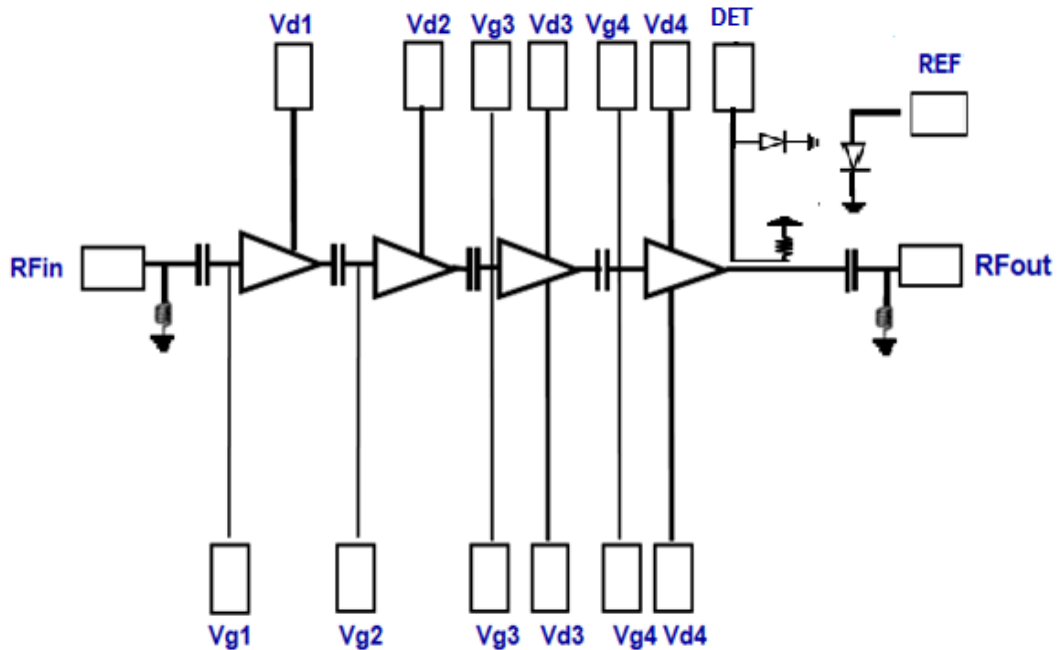
1. Ground the device
2. Bias HPA gate voltage at V_{gs} close to $V_{pinch-off}$ (example: $V_g \approx -2V$)
3. Apply V_{ds} quiescent bias voltage (Example: $V_d = 6V$)
4. Increase V_{gs} up to quiescent bias drain current I_{dq}
5. Apply RF input power

Device Power Up instructions:

1. Turn off RF signal
2. Decrease HPA gate voltage up to $V_{gs} -2V$
3. Decrease drain voltage up to 0V
4. Turn V_g bias voltage to 0V

Notes

Due to ESD protection circuits on RF input and output, an external capacitance might be requested to isolate the product from external voltage potentially present on the RF accesses.



Limited DC decoupling is implemented on chip. Additional external DC decoupling (100pF, 10nF, 1µF) on the PC Board, as close as possible to the bare die, is required.

A 10KΩ resistor is recommended in parallel to VDET, and VREF accesses.

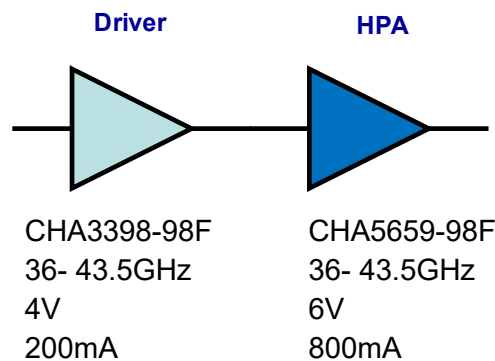
The circuit includes ESD protections on all RF and DC accesses.

Recommended UMS Power chain

The CHA3398-98F is recommended with the CHA5659-98F as driver.

Total Gain: 42dB

Gain control: 30dB with the both amplifiers.



Recommended ESD management

Refer to the application note AN0020 available at <https://www.ums-rf.com> for ESD sensitivity and handling recommendations for the UMS products.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACH N°1907/2006. More environmental data are available in the application note AN0019 also available at <https://www.ums-rf.com>.

Recommended Evaluation board assembly

Refer to the application note AN0030 available at <https://www.ums-rf.com> Evaluation board.

Ordering Information

Chip form: CHA5659-98F/00

Evaluation Board EVB-CHA5659-98F

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