21-27GHz Medium Power Amplifier

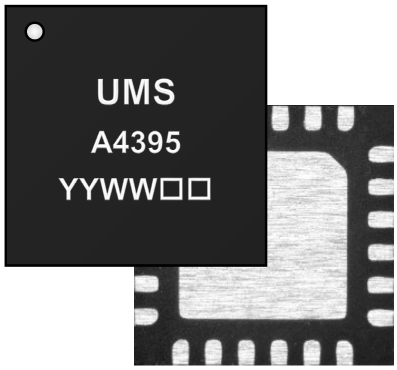
GaAs Monolithic Microwave IC

Description

The CHA4395-QDG is a three-stage GaAs Medium Power Amplifier operating between 21GHz and 27GHz. This amplifier provides 23dBm maximum output power with 15% Power Added Efficiency and 21dBm Output Power at 1dB gain compression. The circuit exhibits a typical small signal gain of 22dB.

This Medium Power Amplifier is well suited for a wide range of Telecom applications including RADAR and Space Communications.

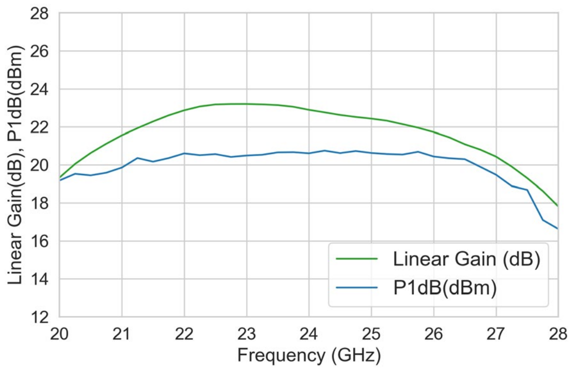
It is available in QFN plastic package. Input and output are 50Ω matched and integrate ESD RF protections.



Main Features

- Frequency range: 21-27GHz
- P1dB = 20dBm
- Linear Gain = 22dB
- ACPR < -35dBc @Pout = 17dBm[(1)]
- EVM <3.5% @Pout = 17dBm[(1)]
- DC bias: Vd=4V@Id=230mA
- 24L-QFN 4x4mm²
- MSL1

(1) with 16QAM modulation, 150MHz & 300MHz bandwidth, Tcase = +25°C



Main Electrical Characteristics

Tcase = +25°C (Tcase : QFN backside temperature)

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	21		27	GHz
Gain	Linear Gain		22		dB
PAE	Power Added Efficiency		15		%
P1dB	Output Power @1dB comp.		21		dBm

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Electrical Characteristics

T_{case} = +25°C, Vd = +4V, (T_{case} : QFN backside temperature)

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	21		27	GHz
Gain	Linear Gain		22		dB
S_{11}	Input Return Loss		-12		dB
S_{22}	Output Return Loss		-10		dB
P1dB	Output Power @1dB Gain compression		21		dBm
NF	Noise Figure		4		dB
ACPR	ACPR @Pout = 17dBm with 16QAM modulation (BW = 150MHz, α = 0.22)		-35		dBc
PAE	Power Added Efficiency @Pin = 2dBm		15		%
Idq	Quiescent Drain Current		230		mA

Absolute Maximum Ratings [1]

T_{case} = +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	4.5	V
Idq	Maximum Quiescent Drain current	280	mA
Vg	Gate bias voltage	-1.5 to +0.4	V
Pin	Maximum peak input power overdrive	+4	dBm
Tj	Junction temperature	175	°C

[1] Operation of this device above anyone of these parameters may cause permanent damage.

Recommended Operating Range [2]

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	3 to 4	V
Idq	Quiescent drain current	170 to 230	mA
Vg	Gate bias voltage	-1.5 to -0.7	V
Pin	Maximum peak input power overdrive [2]	+3	dBm
T_{case}	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +150	°C

[2] Electrical performances are defined for specified test conditions

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Typical Bias Conditions

T_{case} = +25°C

Symbol	Parameter	Value	Unit
VG1, VG2, VG3	Gate voltage tuned for Idq = 230mA	-0.3	V
VD1, VD2, VD3	Drain voltage	4	V

"Power ON" sequence

1. Ground the device
2. Set the gate voltage to -1.5V
3. Apply the drain voltage Vd (typically +4V)
4. Increase Vg up to quiescent drain current Idq
5. Apply RF signal

"Power OFF" sequence

1. Turn off RF signal
2. Decrease the gate voltage to -1.5V
3. Decrease the drain voltage to 0V
4. Decrease the gate voltage to 0V
5. Turn off Vd supply
6. Turn off Vg supply

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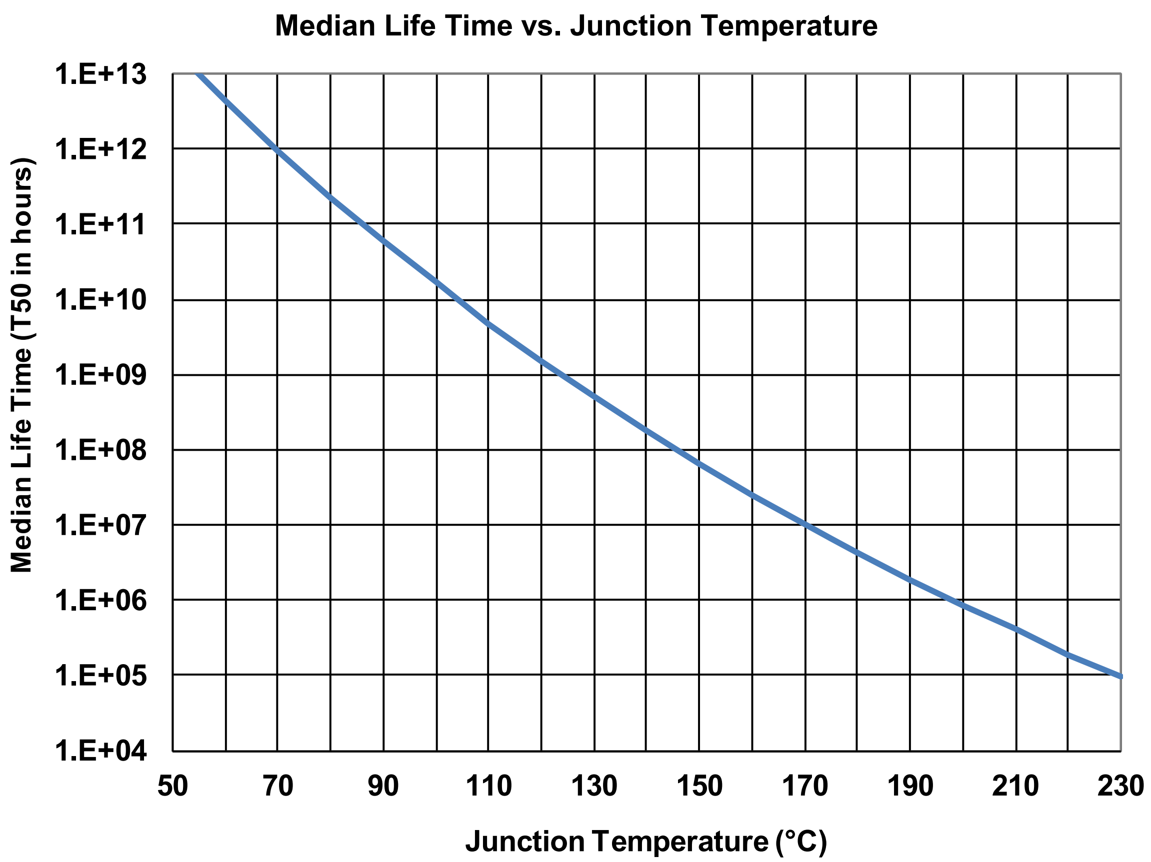
Device thermal performances

All figures provided in this section are based on the assumption that the QFN device is cooled solely by conduction through the package thermal pad, with no consideration of convection mode.
The temperature is monitored at the package backside interface (T_{case}).
For nominal operation, the system maximum temperature must be adjusted in order to guarantee that the junction temperature ($T_{junction}$) remains below the maximum value specified in the Absolute Maximum Ratings table. So the system PCB must be designed to comply with this requirement.

Parameter	Biasing conditions	$T_{JUNCTION}$ (°C)	RTH (°C/W)	T50 (hours)
RTH [1] Thermal Resistance (Junction to QFN Backside)	Vd=4V Pout=22dBm Pdiss=0.85W	165	95	2E+7
	Vd=4V Small Signal Pdiss=0.9W	170	95	1E+7

[1] Assuming 85°C T_{case}



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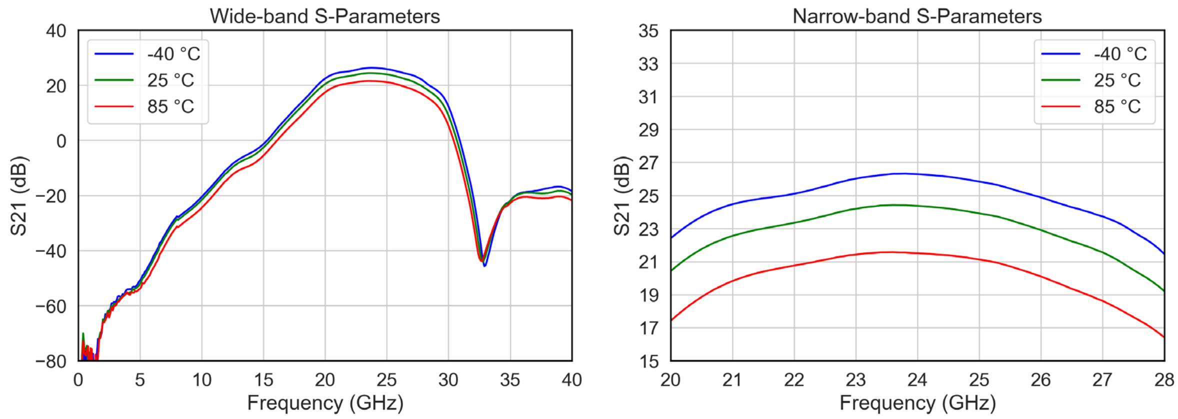
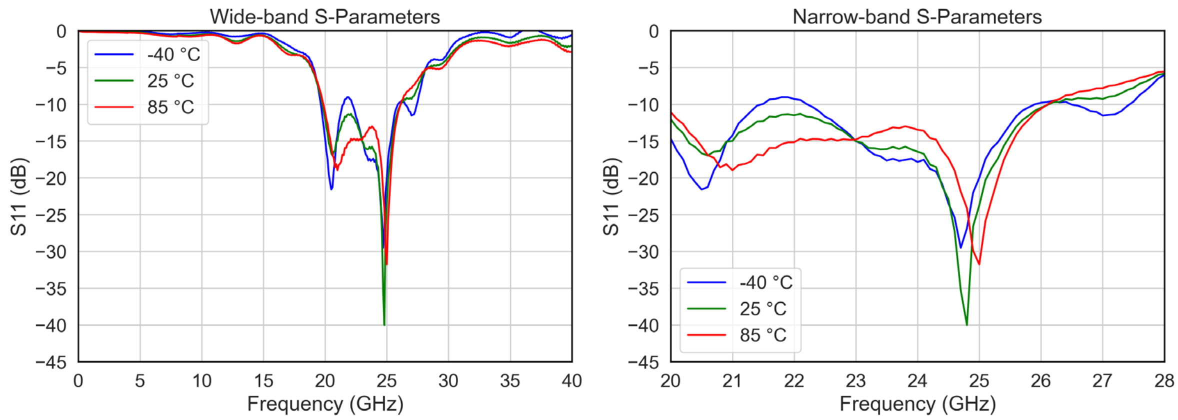
Typical S-Parameters Board Measurements

Test conditions : CW, Vd = +4V, Idq = 230mA, T_{case} = -40°C/25°C/85°C
Measurements are given in QFN access planes.

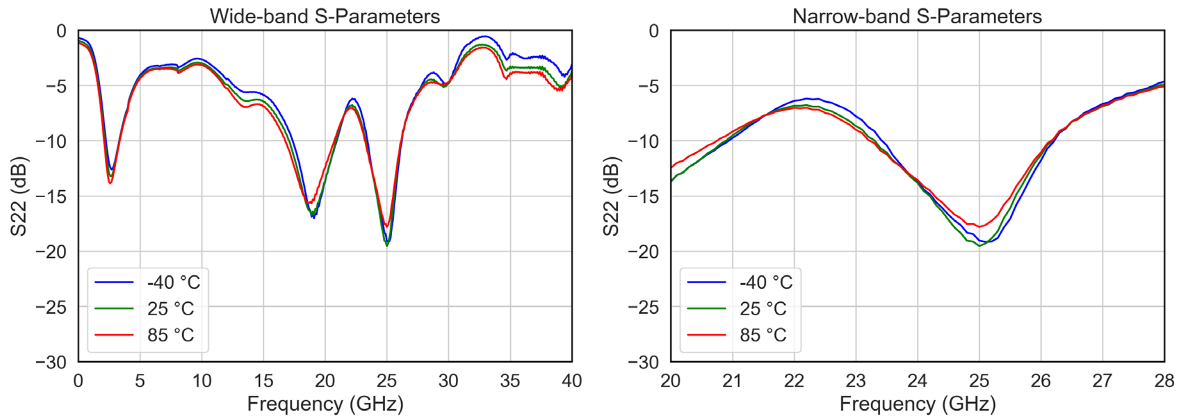
Linear Gain vs. Frequency & Temperature



Input Return Loss vs. Frequency & Temperature



Output Return Loss vs. Frequency & Temperature



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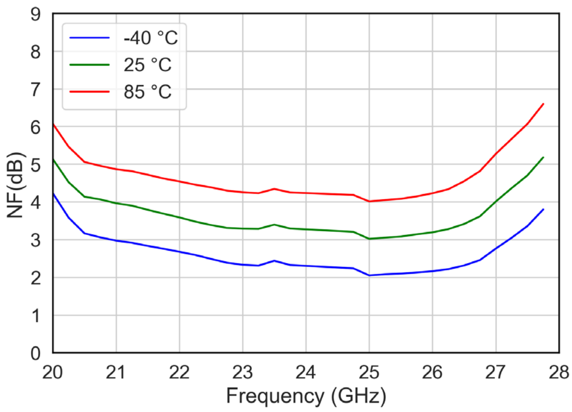
Typical Board Measurements : Noise Figure

Test conditions : CW, Vd = +4V, Idq = 230mA, T_{case} = -40°C/25°C/85°C
Measurements are given in QFN access planes.

Noise Figure vs. Frequency & Temperature



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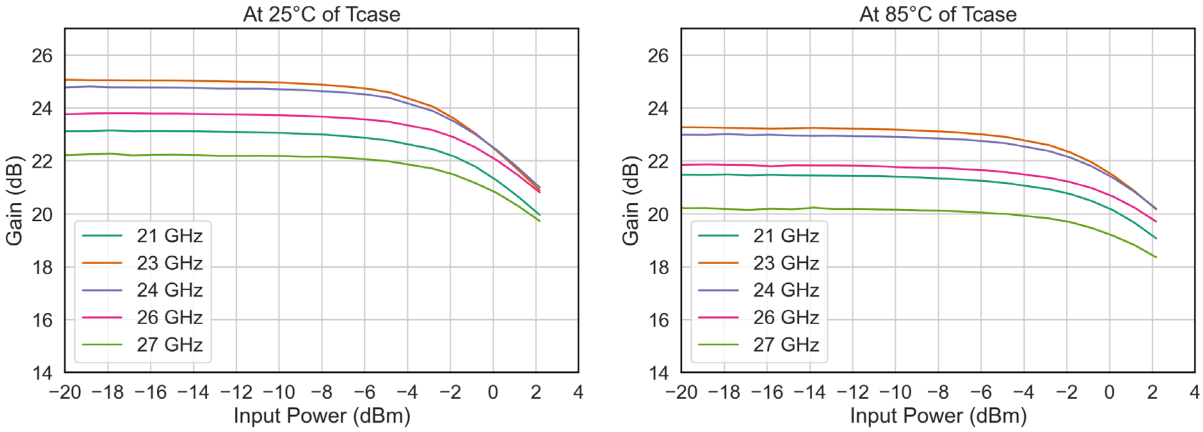
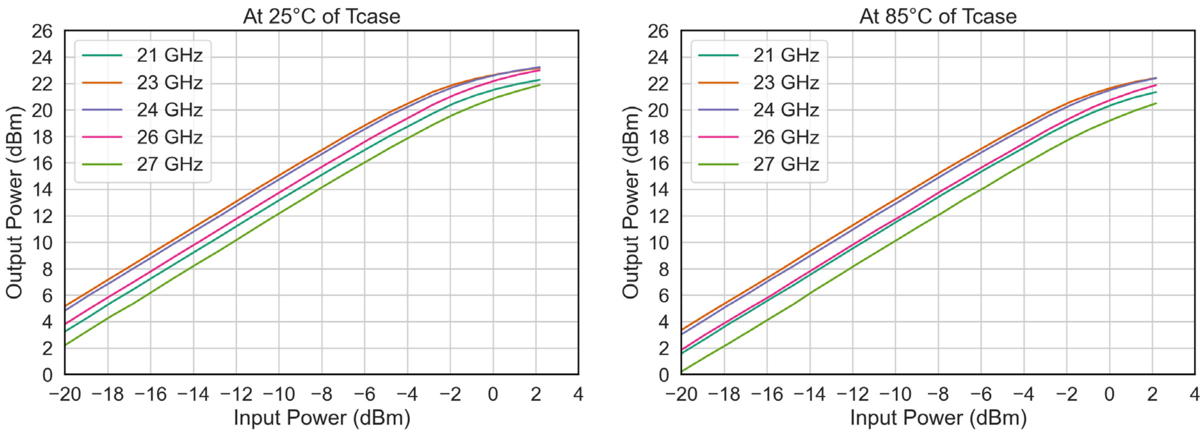
Typical CW Board Measurements vs. Input Power

Test conditions : CW, Vd = +4V, Idq = 230mA, T_{case} = +25°C/85°C
Measurements are given in the QFN access planes.

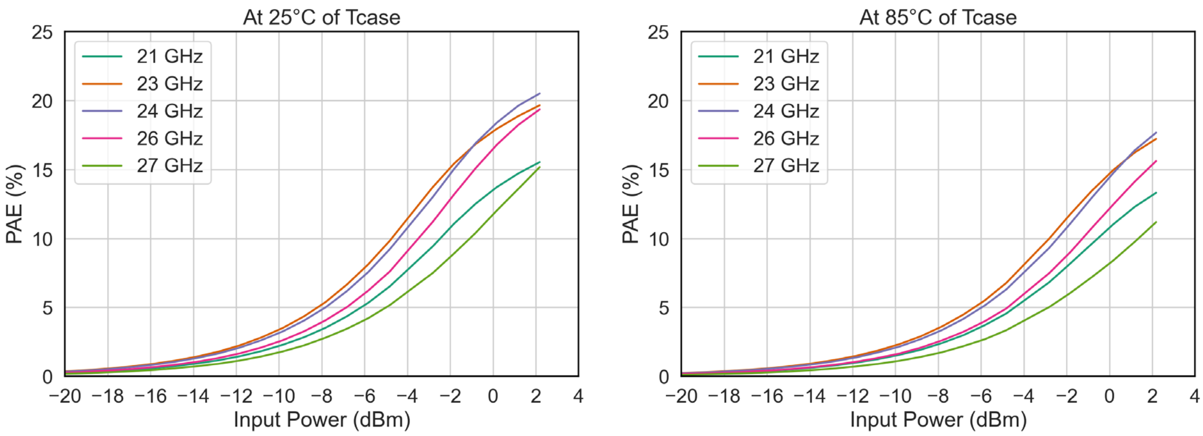
Gain vs. Input Power & Frequency



Output Power vs. Input Power & Frequency



Power Added Efficiency vs. Input Power & Frequency



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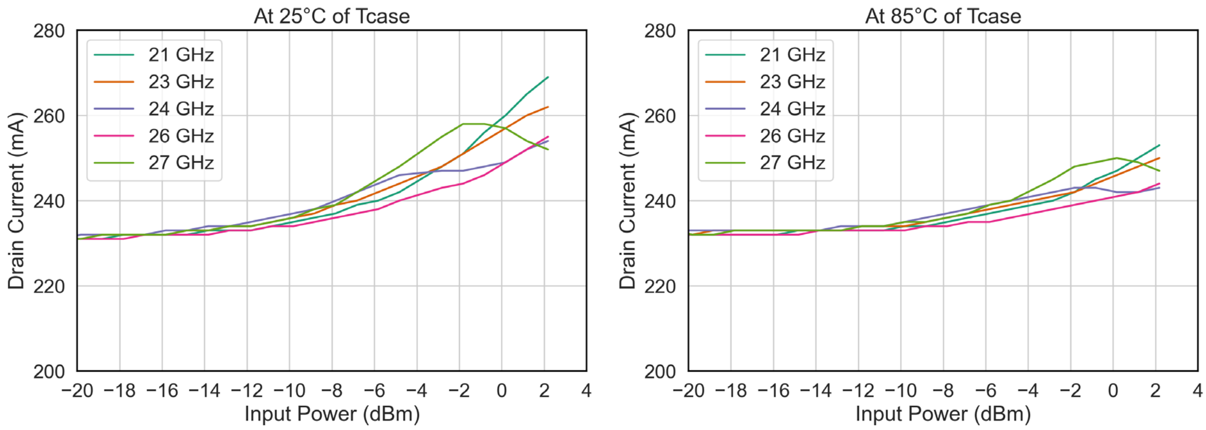
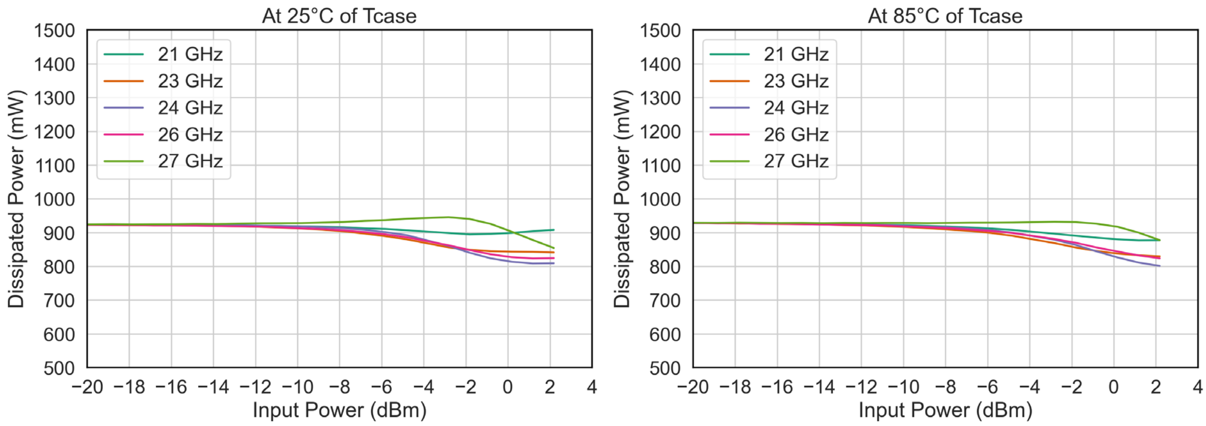
Typical CW Board Measurements vs. Input Power

Test conditions : CW, Vd = +4V, Idq = 230mA, T_{case} = +25°C/85°C
Measurements are given in the QFN access planes.

Drain Current vs. Input Power & Frequency



Dissipated Power vs. Input Power & Frequency



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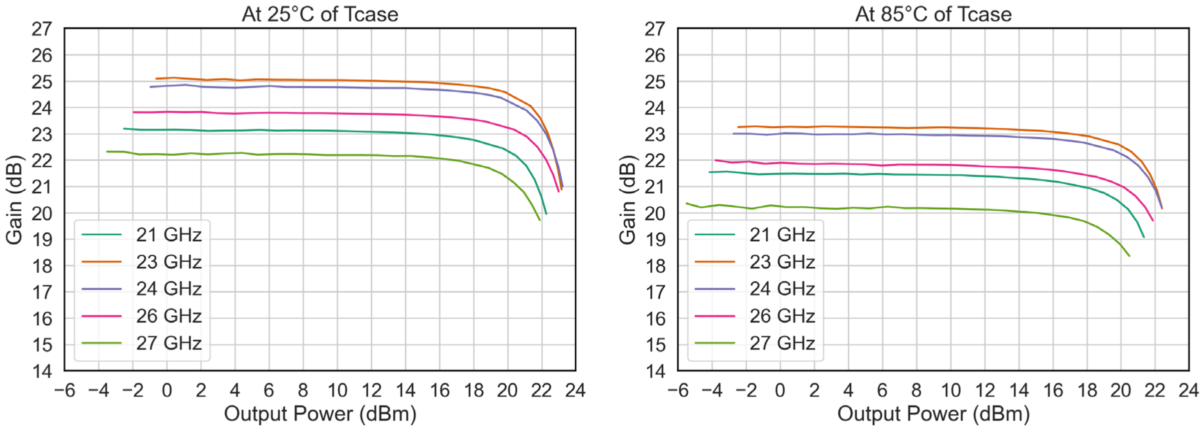
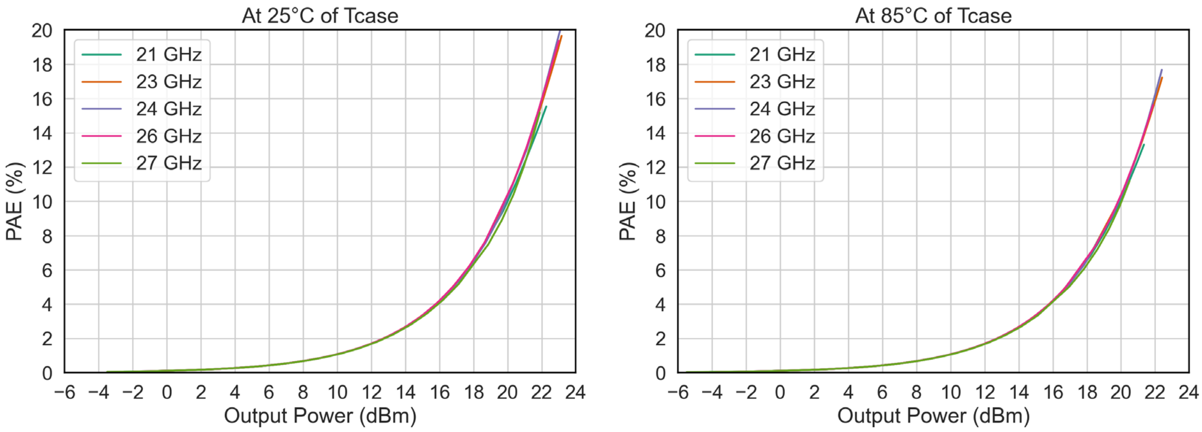
Typical CW Board Measurements vs. Output Power

Test conditions : CW, Vd = +4V, Idq = 230mA, T_{case} = +25°C/85°C
Measurements are given in the QFN access planes.

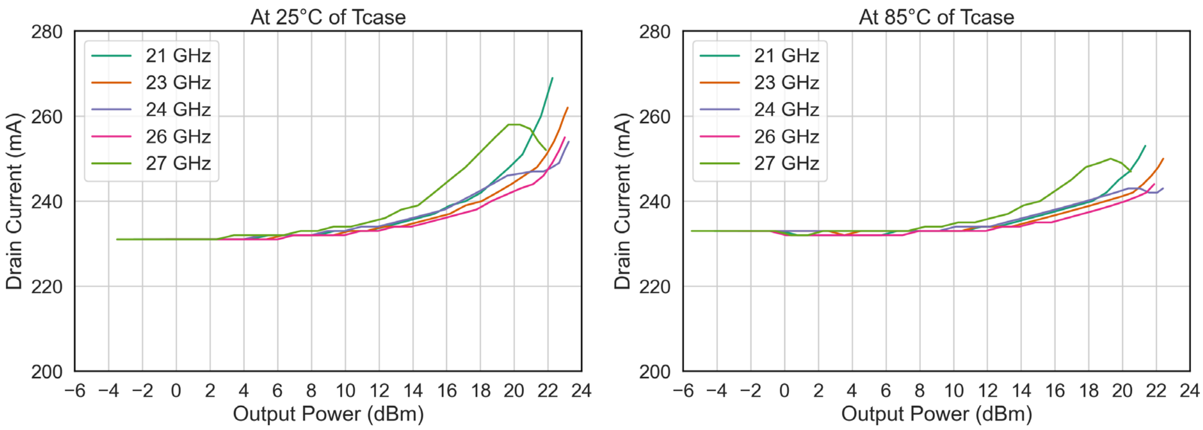
Gain vs. Output Power & Frequency



Power Added Efficiency vs. Output Power & Frequency



Drain Current vs. Output Power & Frequency



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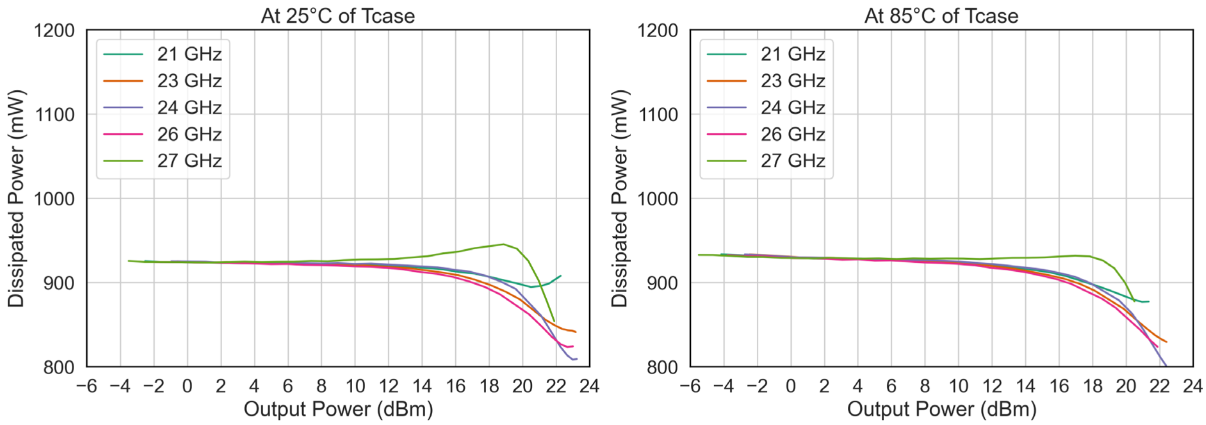
Typical CW Board Measurements vs. Output Power

Test conditions : CW, Vd = +4V, Idq = 230mA, T_{case} = +25°C/85°C
Measurements are given in the QFN access planes.

Dissipated Power vs. Output Power & Frequency



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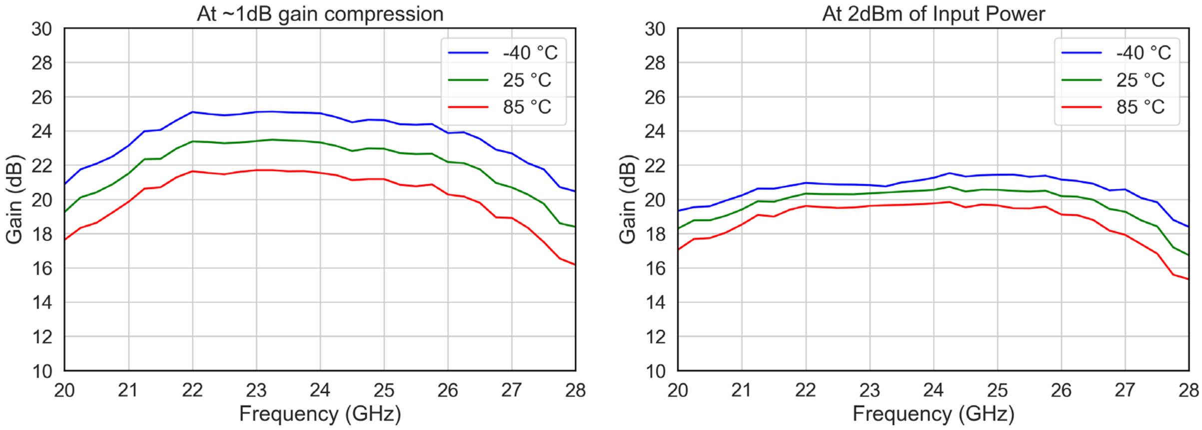
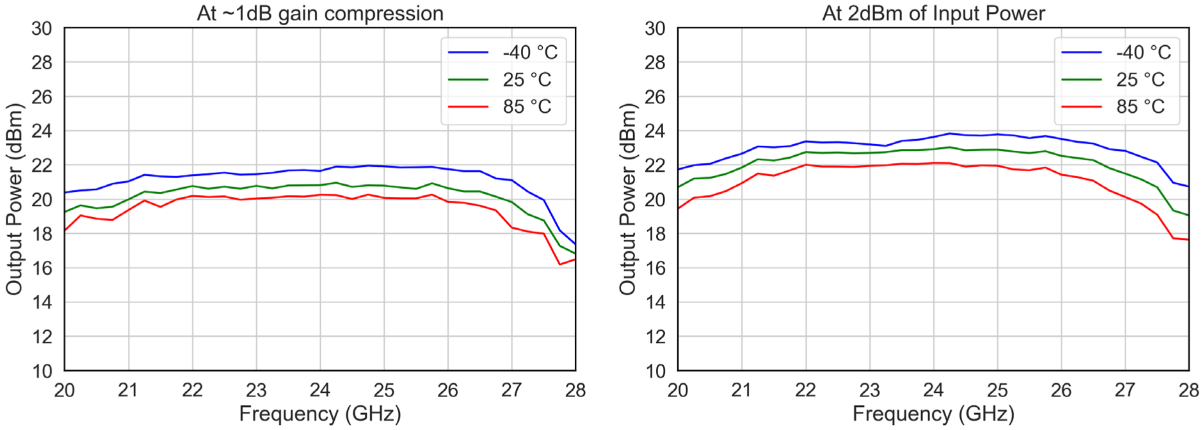
Typical CW Board Measurements vs. Frequency

Test conditions : CW, Vd = +4V, Idq = 230mA, T_{case} = -40°C/25°C/85°C
Measurements are given in the QFN access planes

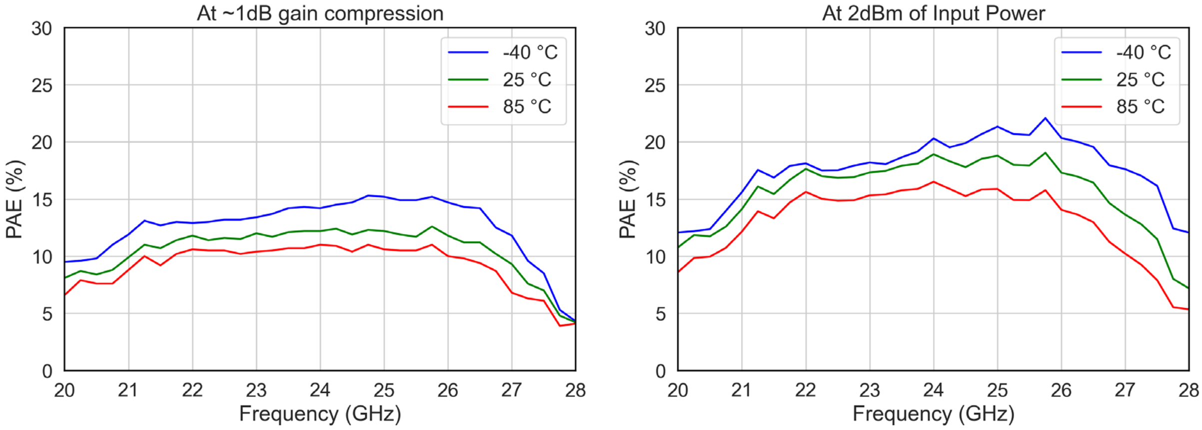
Gain vs. Frequency & Temperature



Output Power vs. Frequency & Temperature



Power Added Efficiency vs. Frequency & Temperature



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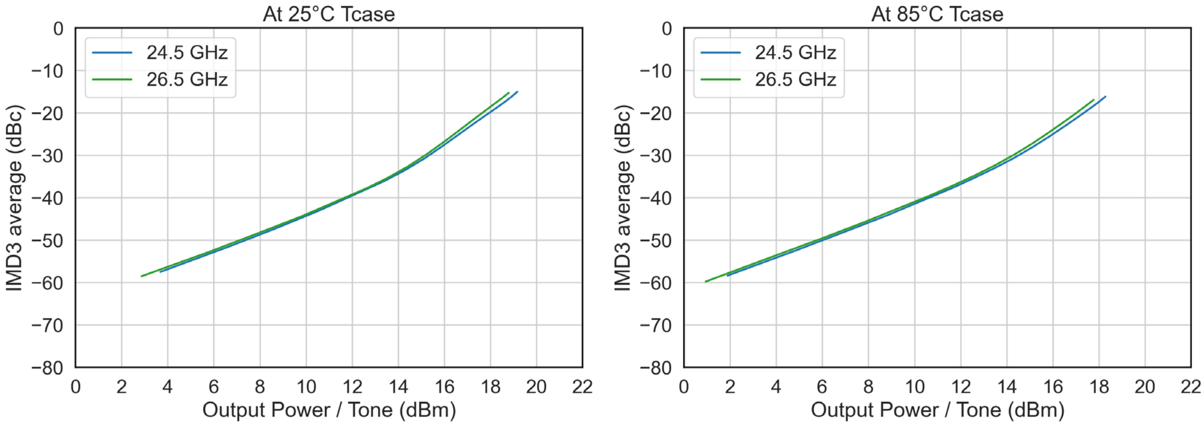
Typical Board Measurements : Modulation Results

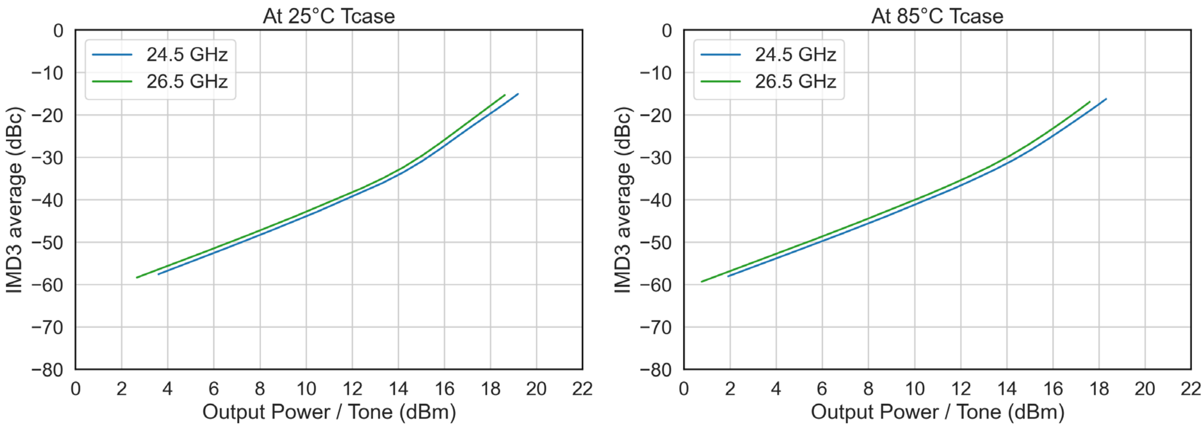
Test conditions : CW dual tones, Vd = +4V, Idq = 230mA, Δf = 10MHz, T_{case} = +25°C/85°C

IMD3 vs. Output Power per Tone & Frequency



Test conditions : CW dual tones, Vd = +4V, Idq = 230mA, Δf = 100MHz, T_{case} = +25°C/85°C

IMD3 vs. Output Power per Tone & Frequency



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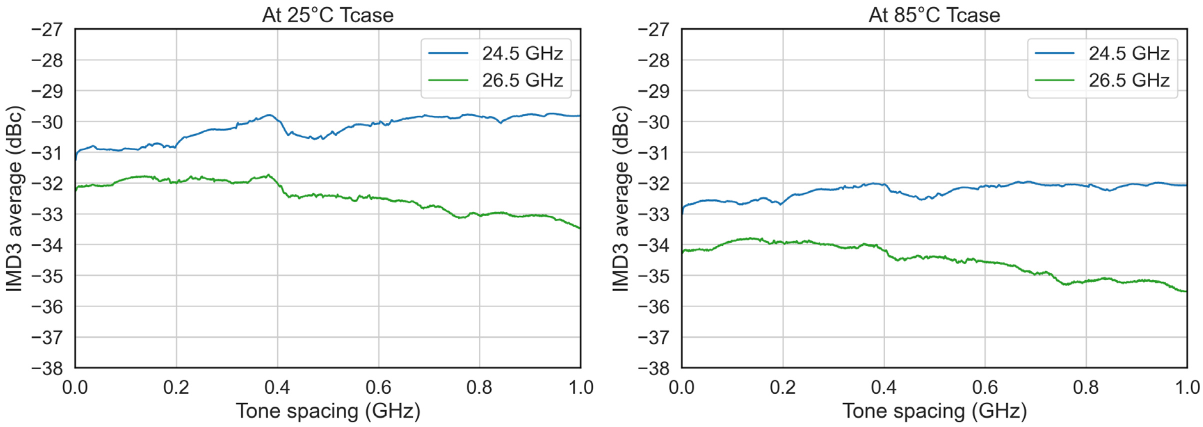
Typical Board Measurements : Modulation Results

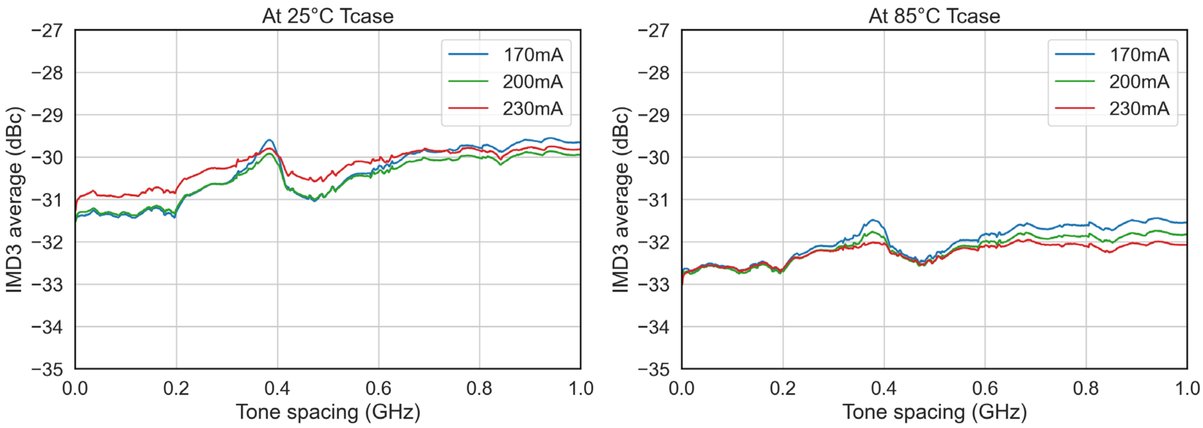
Test conditions : CW dual tones, Vd = +4V, Idq = 230mA, Pout = 17dBm, T_{case} = +25°C/85°C

IMD3 vs. Tone Spacing & Frequency



Test conditions : CW dual tones, Vd = +4V, Fc = 24.5GHz, Pout = 17dBm, T_{case} = +25°C/85°C

IMD3 vs. Tone Spacing & Drain Current



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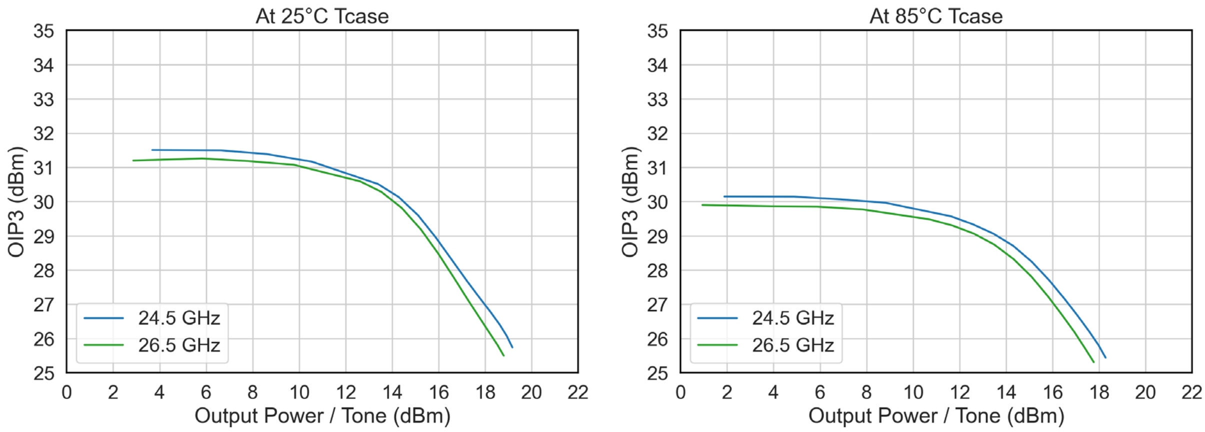
Typical Board Measurements : Modulation Results

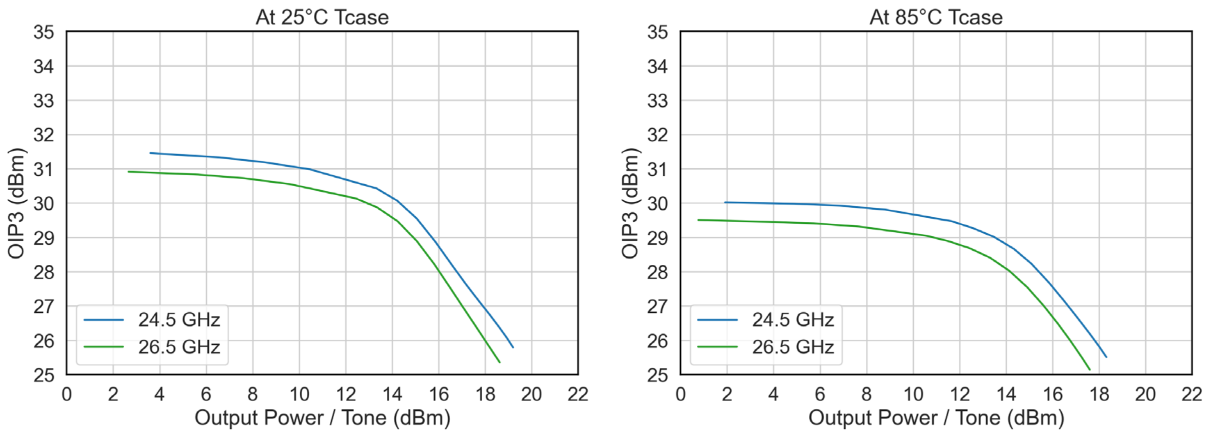
Test conditions : CW dual tones, Vd = +4V, Idq = 230mA, Δf = 10MHz, T_{case} = +25°C/85°C

OIP3 vs. Output Power per Tone & Central Frequency



Test conditions : CW dual tones, Vd = +4V, Idq = 230mA, Δf = 100MHz, T_{case} = +25°C/85°C

OIP3 vs. Output Power per Tone & Frequency



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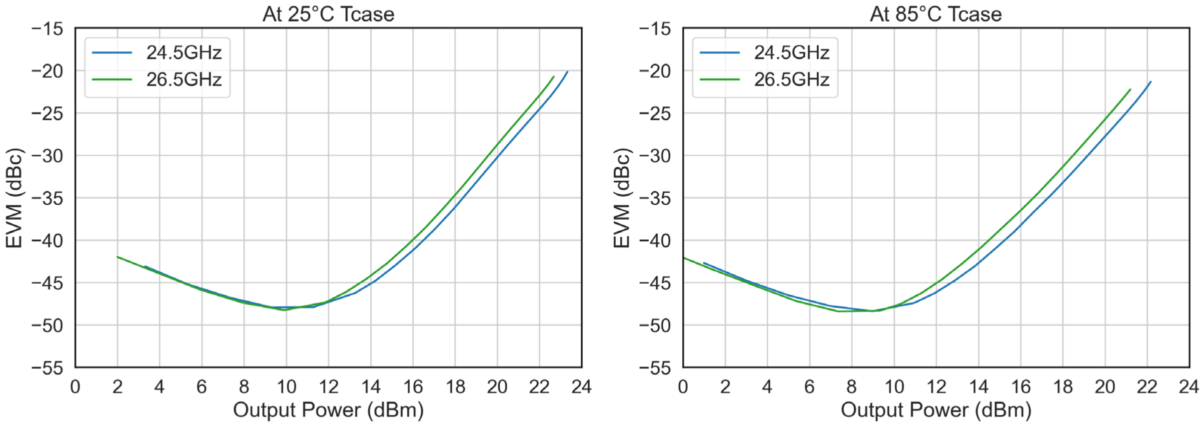
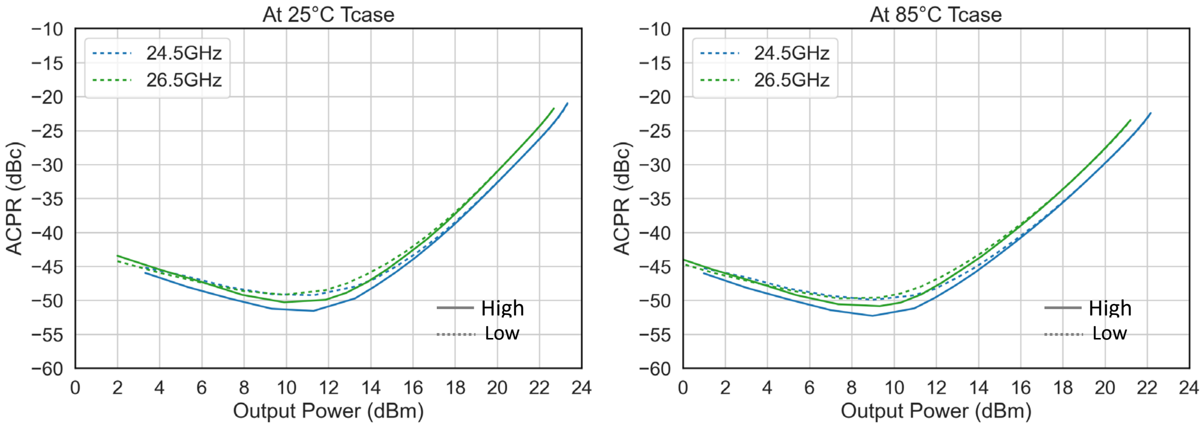
Typical Board Measurements : Modulation Results

Test conditions : Vd = +4V, Idq = 230mA, **8PSK**, **BW = 150MHz**, Roll-off = 0.2, PAPR = 5.1dB, T_{case} = +25°C/85°C

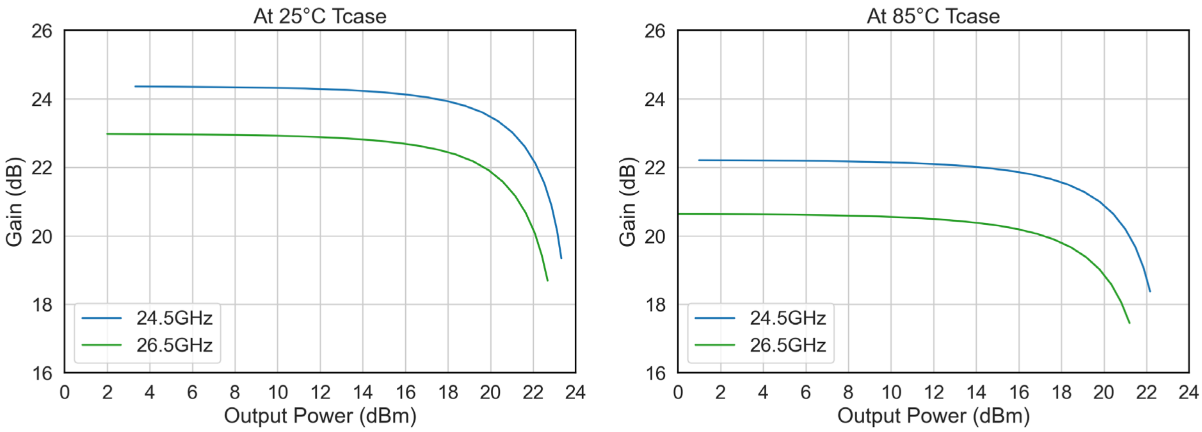
EVM vs. Output Power & Central Frequency



ACPR vs. Output Power & Central Frequency



Gain vs. Output Power & Central Frequency



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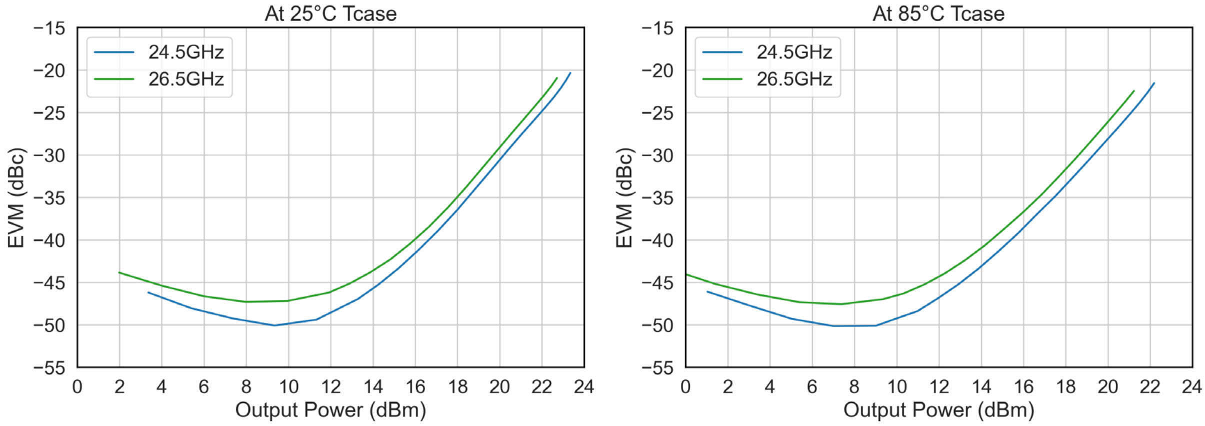
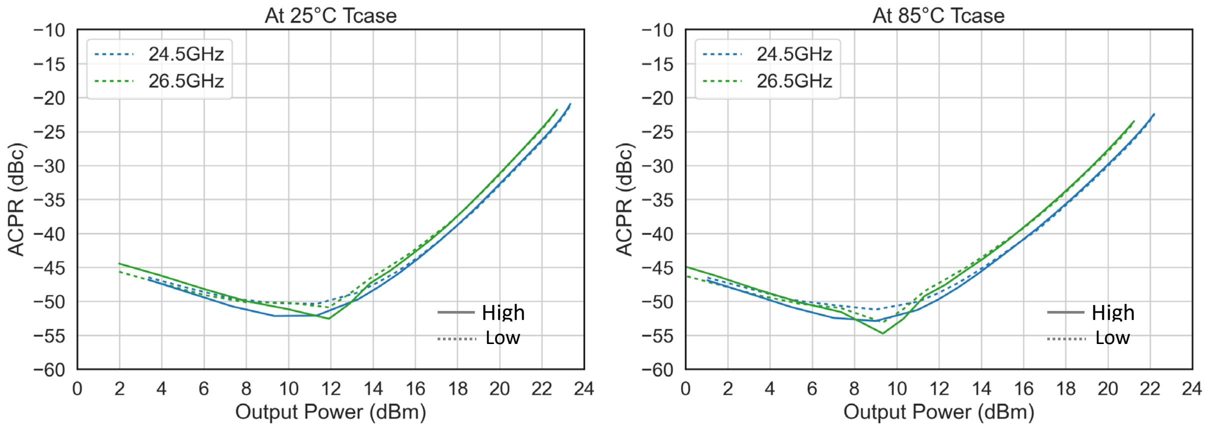
Typical Board Measurements : Modulation Results

Test conditions : Vd = +4V, Idq = 230mA, **8PSK, BW = 300MHz**, Roll-off = 0.2, PAPR = 5.1dB, T_{case} = +25°C/85°C

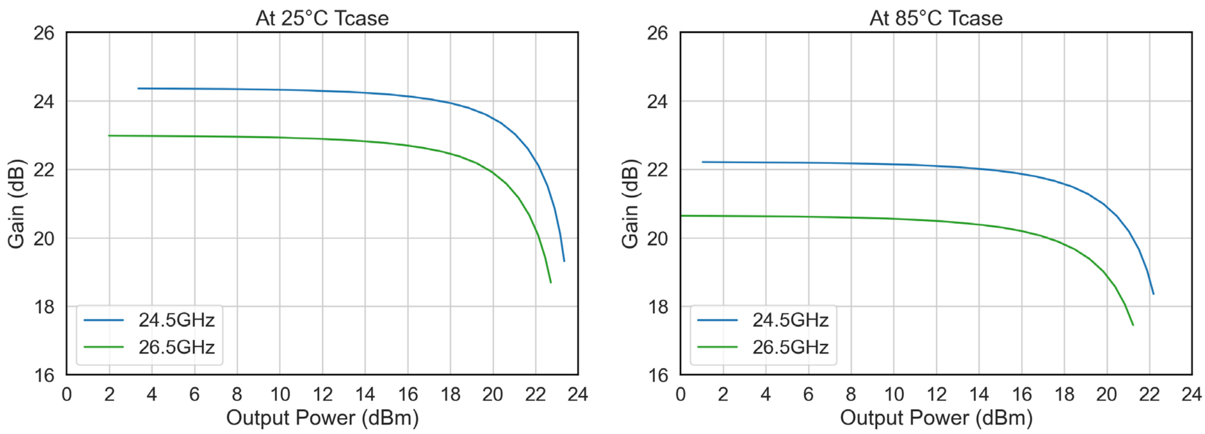
EVM vs. Output Power & Central Frequency



ACPR vs. Output Power & Central Frequency



Gain vs. Output Power & Central Frequency



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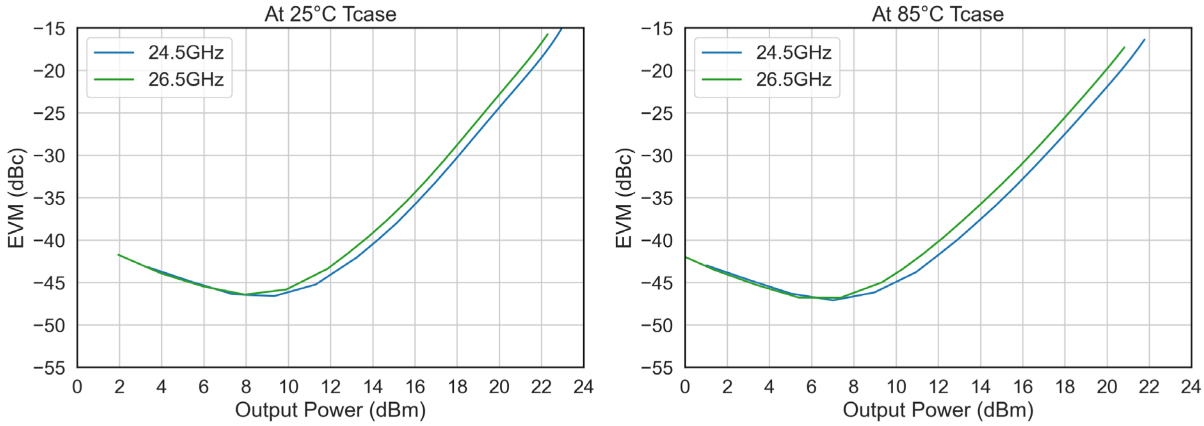
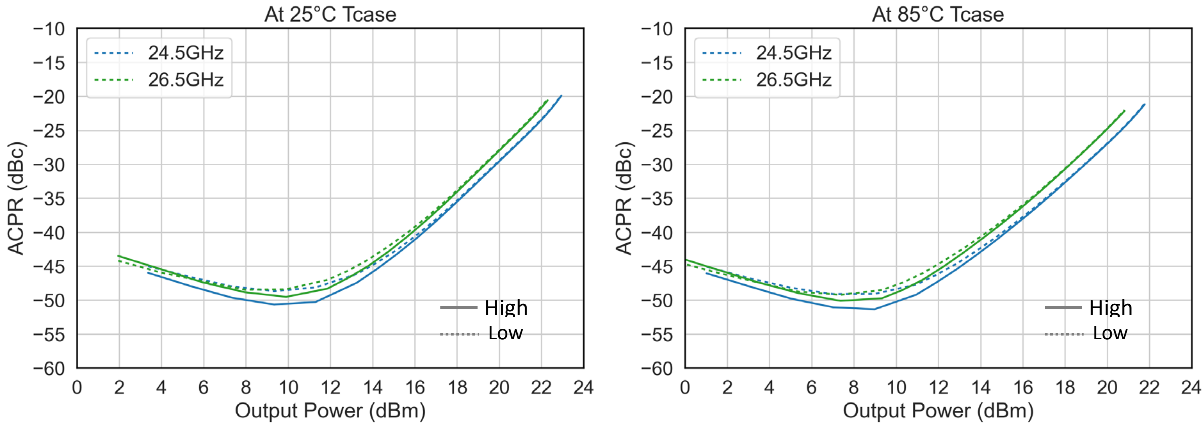
Typical Board Measurements : Modulation Results

Test conditions : Vd = +4V, Idq = 230mA, **16QAM, BW = 150MHz**, Roll-off = 0.2, PAPR = 6.5dB, T_{case} = +25°C/85°C

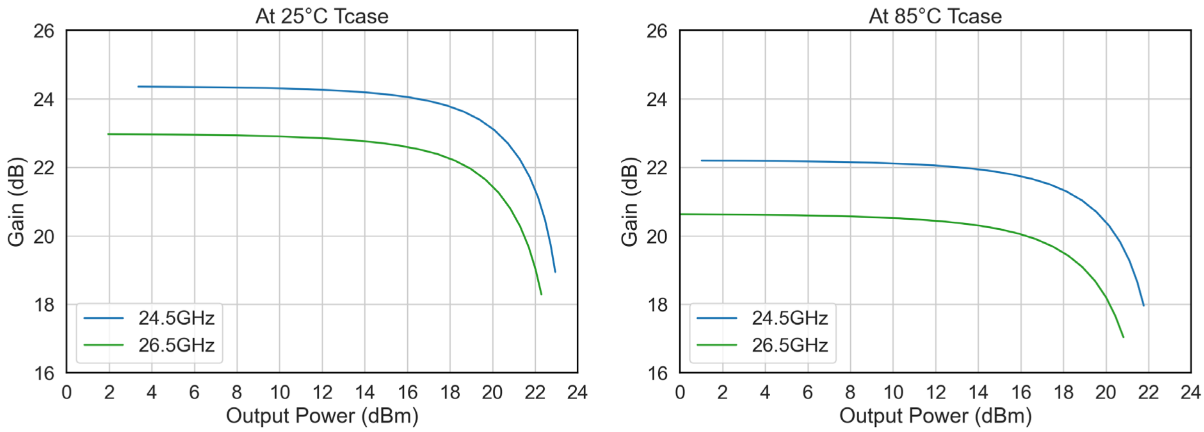
EVM vs. Output Power & Central Frequency



ACPR vs. Output Power & Central Frequency



Gain vs. Output Power & Central Frequency



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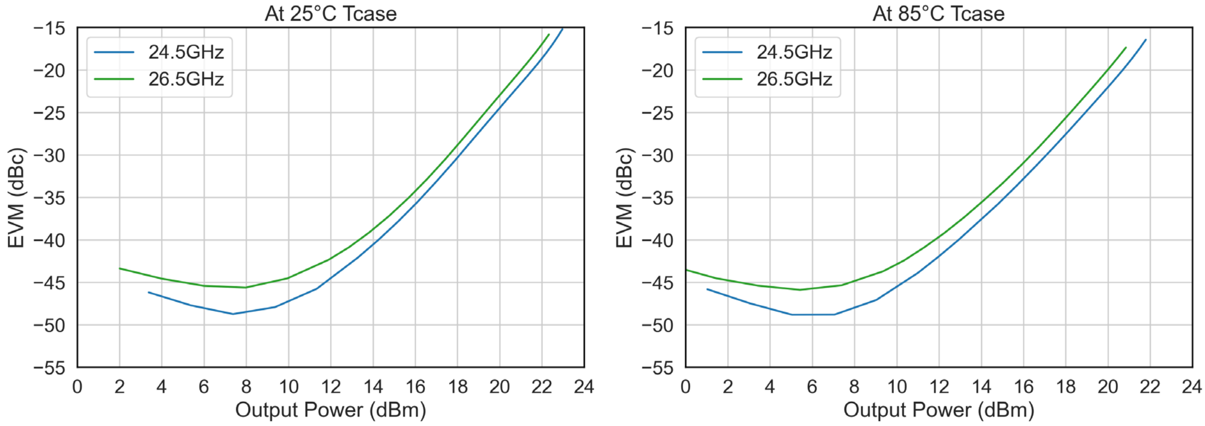
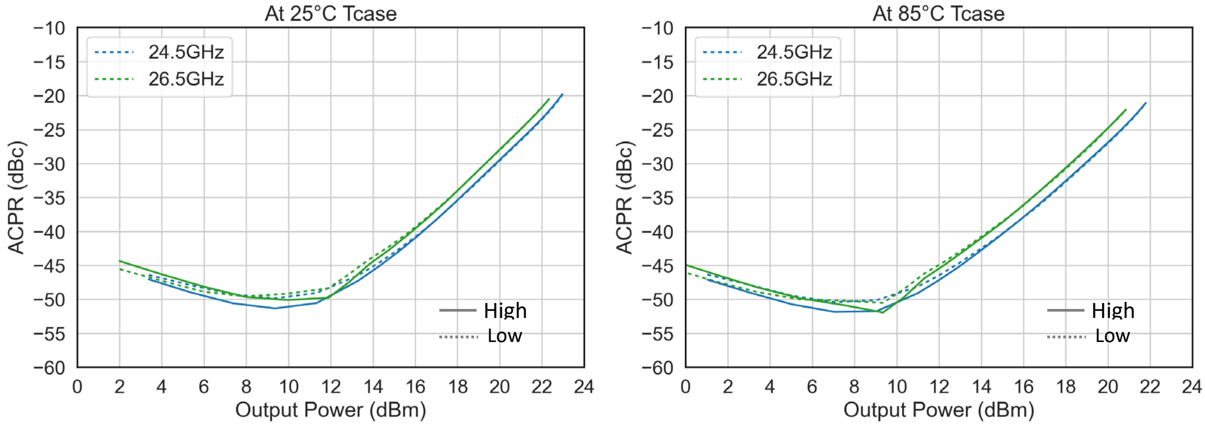
Typical Board Measurements : Modulation Results

Test conditions : Vd = +4V, Idq = 230mA, **16QAM, BW = 300MHz**, Roll-off = 0.2, PAPR = 6.5dB, T_{case} = +25°C/85°C

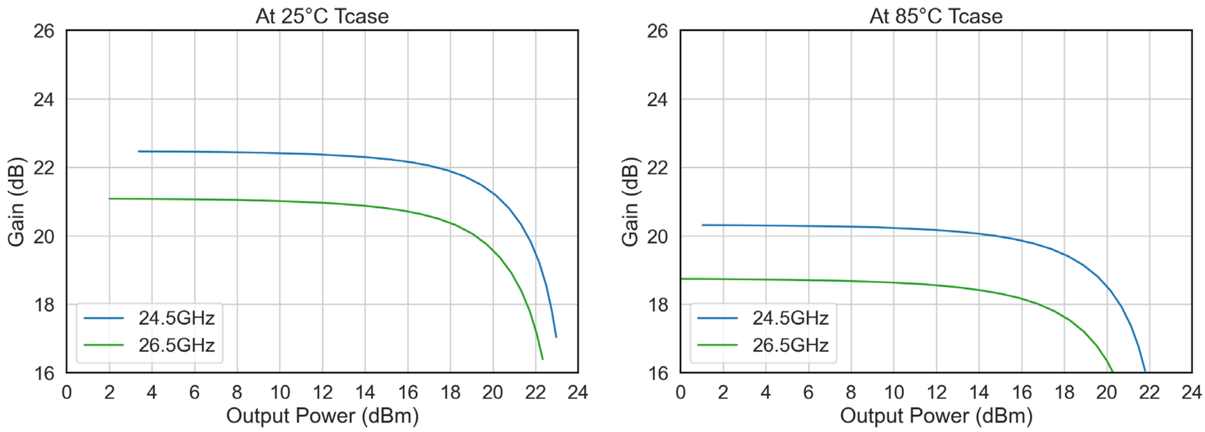
EVM vs. Output Power & Central Frequency



ACPR vs. Output Power & Central Frequency



Gain vs. Output Power & Central Frequency



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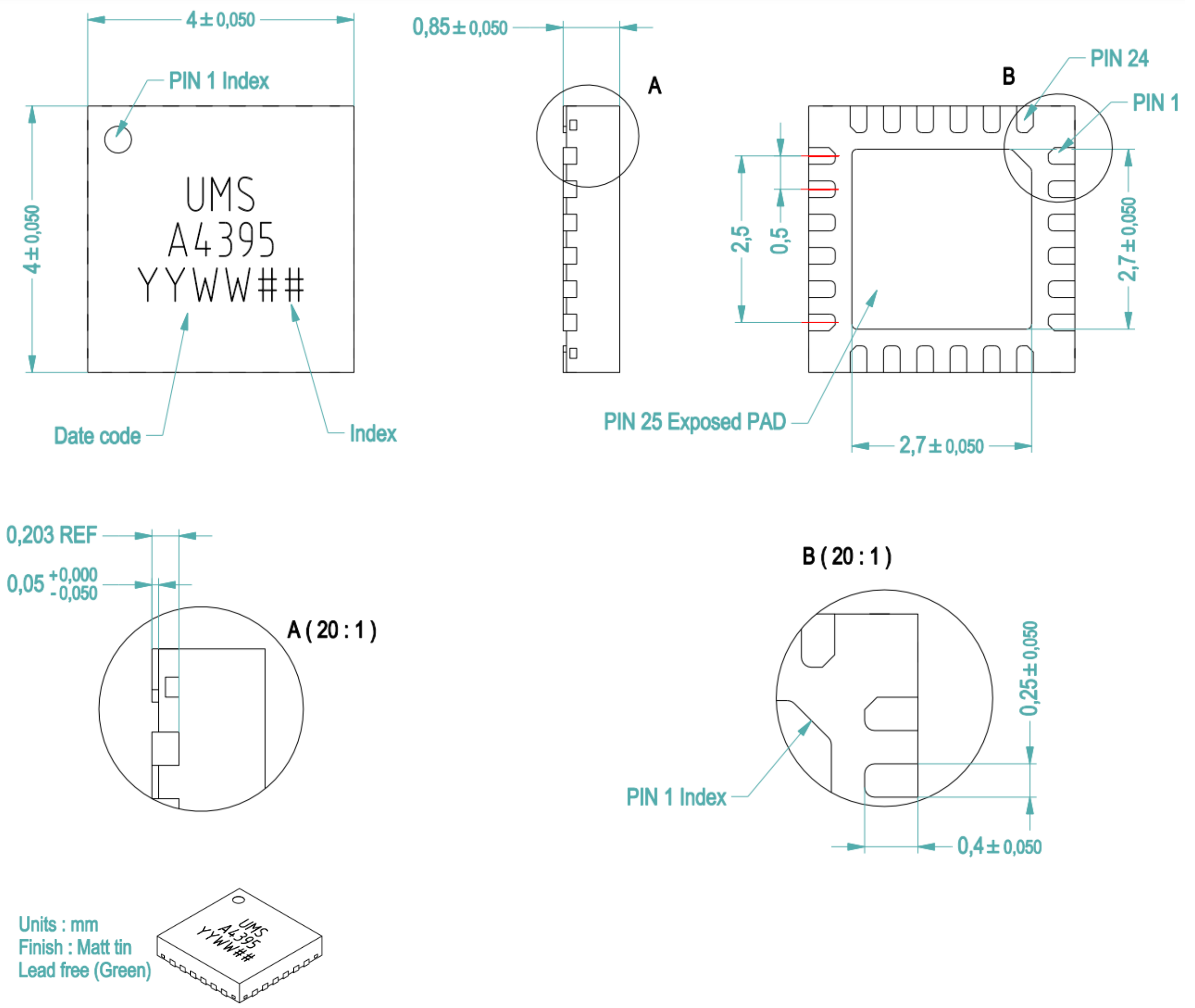
Package outline



Finish:	Matt Tin Lead Free (Green)	1- NC	11- GND[1]	21- VD3
Units :	mm	2- GND[1]	12- NC	22- VD2
From the standard :	JEDEC MO-220	3- GND[1]	13- GND[1]	23- VD1
	(VGGD)	4- RFin	14- GND[1]	24- NC
		5- GND[1]	15- RFout	25- GND[1]
		6- GND[1]	16- GND[1]	
		7- NC	17- GND[1]	
		8- VG1	18- NC	
		9- VG2	19- NC	
NC :	Not Connected	10- VG3	20- GND[1]	

[1] It is strongly recommended to ground all pins marked "GND" through the PCB. Ensure that the PCB board is designed to provide the best possible ground to the package.

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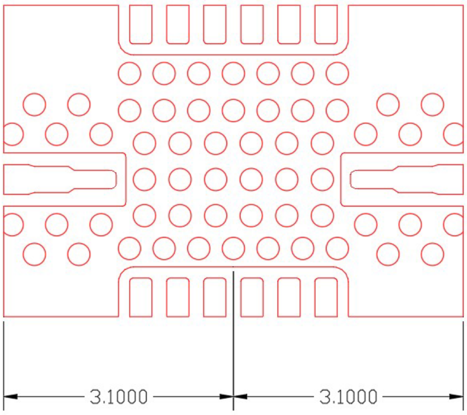
Definition of measurement reference planes

Reference planes used for measurements given above are symmetrical from the central axis of the package (see drawing beside). Input and output reference planes are located at 3.1mm offset (input wise and output wise respectively) from this axis.



ESD sensitivity

Parameter	Classification	Standard
Human Body Model (HBM)	1A	JESD22 A114
Charge Device Model (CDM)	III	JESD22 A101

Package Information

Parameter	Value
Package body material	RoHS-compliant
	Low stress Injection Molded Plastic
Lead finish	100% Matt Tin
Moisture Sensitivity Level	MSL1

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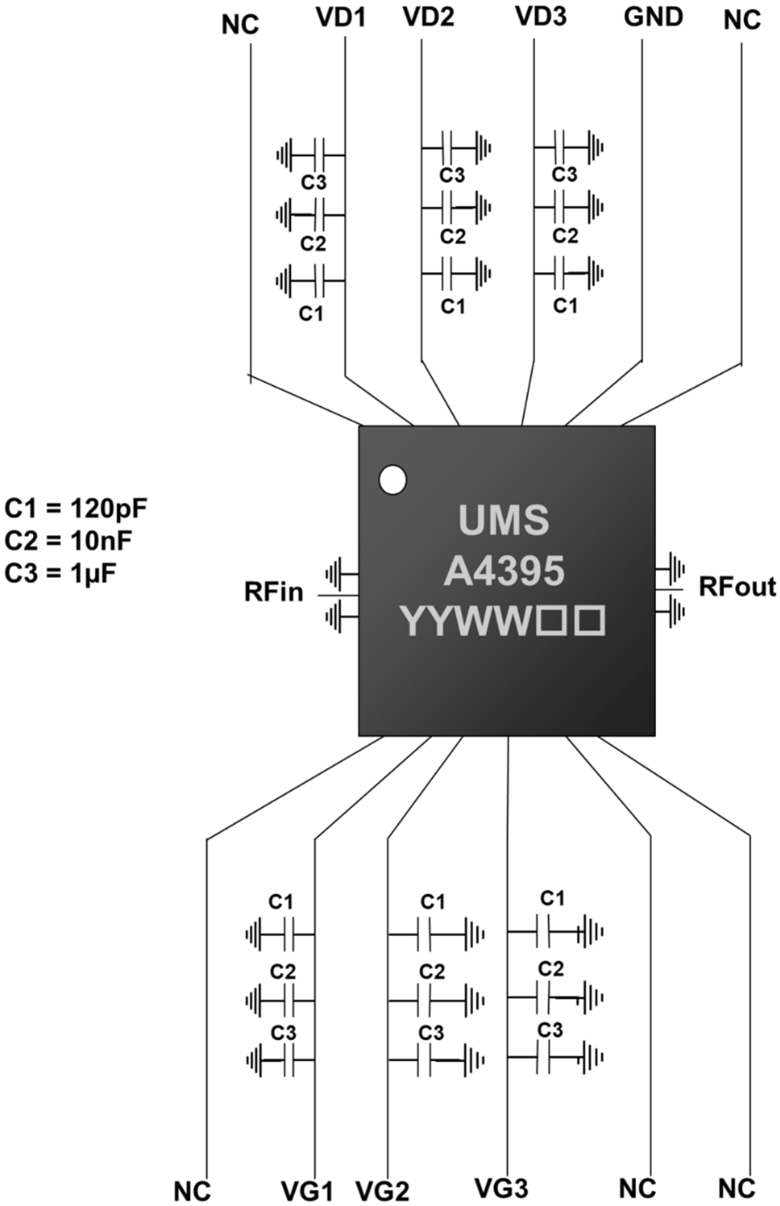
Recommended assembly plan



Recommended circuit bonding table

Label	Pin	Type	Decoupling	Comment
VD1, VD2, VD3	21, 22, 23	Vd	120pF, 10nF & 1µF	Drain Supply
VG1, VG2, VG3	8, 9, 10	Vg	120pF, 10nF & 1µF	Gate Supply

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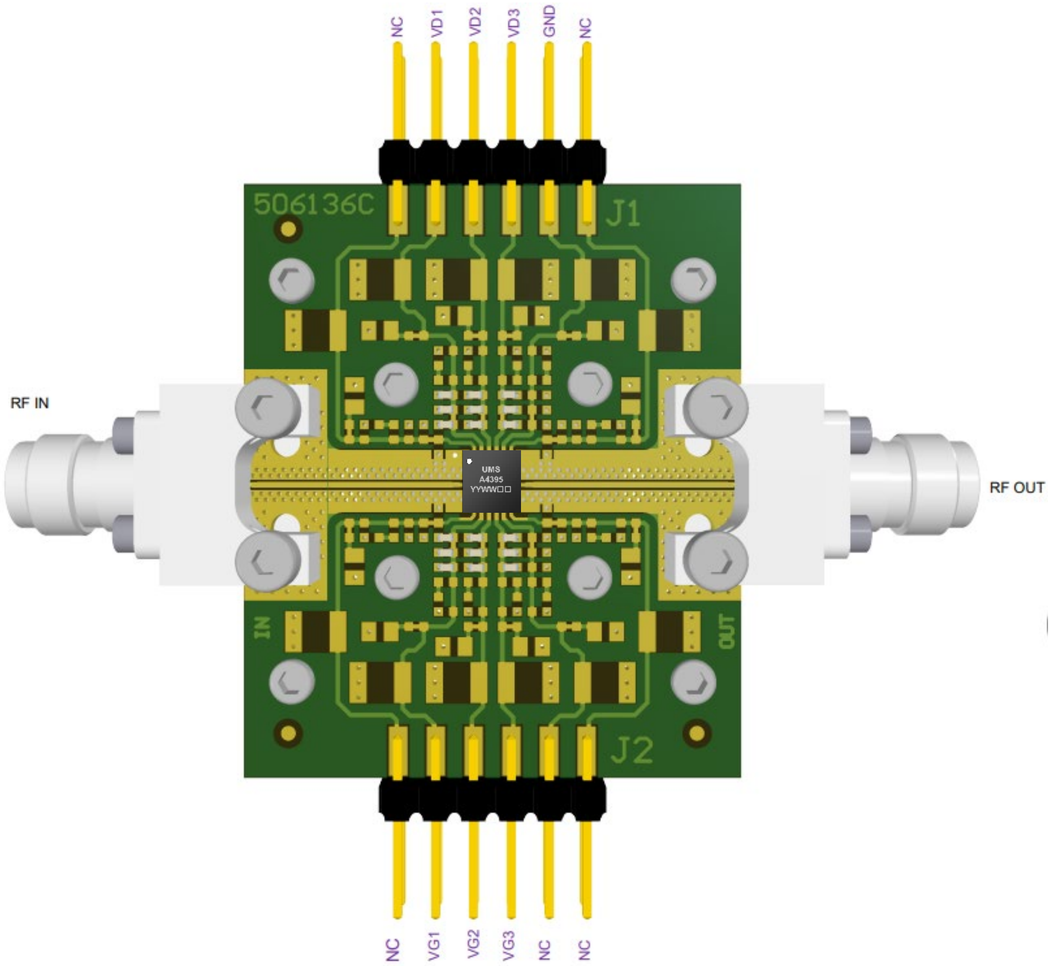
Evaluation board

■ Compatible with the proposed footprint.
■ Based on typically Ro4350B / 8mils or equivalent.
■ Using a micro-strip to coplanar transition to access the package.
■ Recommended for the implementation of this product on a module board.
■ Decoupling capacitors of 120pF ± 10%, 10nF ± 10% & 1 µF ±10% are recommended for all DC access.
■ To ensure safe operation, all measurements must be performed using **shielded cables**, **even for DC bias**.



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Notes

Due to ESD protection circuits on RF input and output, an external capacitance might be requested to isolate the product from external voltage that could be present on each RF access.

ESD protections are also implemented on gate and control access.

The DC connections do not include any decoupling capacitors in the package. Therefore it is mandatory to provide a good external DC decoupling (120pF, 10nF & 1µF) on the PC board as close as possible to the package.

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Recommended package footprint

Refer to the application note AN0017 available at https://www.ums-rf.com/ for package foot print recommendations.

SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017 available at https://www.ums-rf.com/.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at https://www.ums-rf.com/.

Recommended ESD management

Refer to the application note AN0020 available at https://www.ums-rf.com/ for ESD sensitivity and handling recommendations for the UMS package products.

Description of Evaluation Board

Refer to the application note AN0031 available at https://www.ums-rf.com for the description of Evaluation Board for Packaged Die and recommendations for this UMS package product.

Ordering request reference

QFN 4x4 package :	CHA4395-QDG/XY	
	Stick: XY = 20	Tape & reel: XY = 21
Evaluation board :	EVB-CHA4395-QDG	

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