

## 17-24GHz Medium Power Amplifier GaAs Monolithic Microwave IC

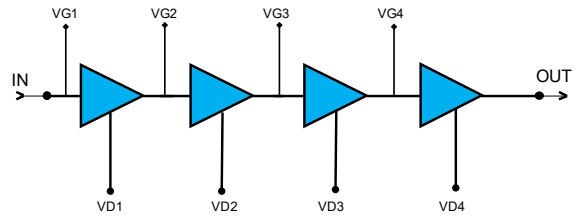
### Description

The CHA4253a98F is a four stage monolithic Medium Power Amplifier.

It is designed for a wide range of applications, from Point To Point Radio and K band to other commercial communication systems.

The circuit is manufactured with a pHEMT process, 0.15µm gate length.

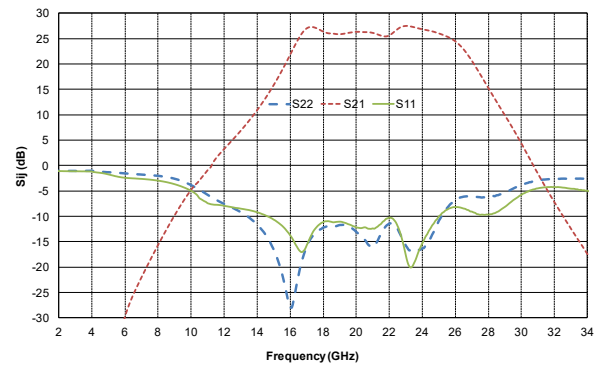
It is available in chip form.



### Main Features

- Broadband performances: 17-24GHz
- 24.5dBm Pout for 1dB gain compression
- 26dB gain
- 32dBm OTOI
- DC bias: Vd= 4.0V, Id= 230mA
- Chip size 2.61x1.66x0.07mm

S-parameters



### Main Electrical Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	17.0		24.0	GHz
Gain	Linear Gain		26		dB
P-1dB	Output Power @1dB comp.		24.5		dBm
OTOI	3 <sup>rd</sup> order Intercept point		32		dBm

## Specifications

Tamb.= +25°C, Vd = +4.0V

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	17.0		24.0	GHz
Gain	Linear Gain		26		dB
$\Delta G$	Gain variation in temperature		-0.04		dB/°C
OTOI	3 <sup>rd</sup> order Intercept point		32		dBm
P <sub>-1dB</sub>	Output power @ 1dB compression		24.5		dBm
Psat	Saturated Output Power		25		dBm
RLin	Input Return Loss		12		dB
RLout	Output Return Loss		13		dB
NF	Noise figure		7.5		dB
Id	Quiescent Drain current		230		mA
Vg	Gate voltage		-0.7		V

These values are representative of test fixture measurements.

### “Power ON” sequence

1. Ground the device
2. Bias MPA gate voltage at Vg low enough (Typically: Vg ≈ -2V)
3. Apply Vds bias voltage (Typically: Vd = 4V)
4. Increase slowly Vgs up to quiescent bias drain current Idq
5. Apply RF signal

### “Power OFF” sequence

1. Turn off RF signal
2. Bias MPA gate voltage at Vg low enough (Typically: Vg ≈ -2V)
3. Turn Vds bias voltage to 0V
4. Turn Vgs bias voltage to 0V

**Absolute Maximum Ratings** <sup>(1)</sup>T<sub>amb.</sub> = +25°C

Symbol	Parameter	Values	Unit
V <sub>d</sub>	Drain bias voltage	6V	V
I <sub>d</sub>	Drain bias quiescent current	370	mA
V <sub>g</sub>	Gate bias voltage	-2 to +0.4	V
V <sub>dg</sub>	External drain-gate excursion	12	V
P <sub>in</sub>	Maximum input power	10	dBm
T <sub>j</sub>	Junction temperature <sup>(2)</sup>	175	°C
T <sub>a</sub>	Operating temperature range	-40 to +95	°C
T <sub>stg</sub>	Storage temperature range	-55 to +150	°C

<sup>(1)</sup> Operation of this device above any one of these parameters may cause permanent damage.

<sup>(2)</sup> See "Thermal device performance" for junction to ground Thermal Resistance

**Recommended Operating Range** <sup>3, 4</sup>

Symbol	Parameter	Values	Unit
V <sub>d</sub>	Drain bias voltage	3.3 to 4	V
I <sub>d</sub>	Drain bias current	180 to 230	mA
V <sub>g</sub>	Gate bias voltage	-1 to 0	V
P <sub>in</sub>	Maximum peak input power overdrive	5	dBm

<sup>(3)</sup> Electrical performances are defined for specified test conditions

<sup>(4)</sup> Electrical performances are not guaranteed over all recommended operating conditions

**Temperature Range**

T <sub>a</sub>	Operating temperature range	-40 to +95	°C
T <sub>stg</sub>	Storage temperature range	-55 to +150	°C

**Typical Bias Conditions**T<sub>amb.</sub> = +25°C

Pad N°	Parameter	Values	Unit
VG1	DC Gate voltage 1 <sup>st</sup> stage	-0.7	V
VG2	DC Gate voltage 2 <sup>nd</sup> stage	-0.7	V
VG3	DC Gate voltage 3 <sup>rd</sup> stage	-0.7	V
VG4	DC Gate voltage 4 <sup>th</sup> stage	-0.7	V
VD1	DC Drain voltage 1 <sup>st</sup> stage	4.0	V
VD2	DC Drain voltage 2 <sup>nd</sup> stage	4.0	V
VD3	DC Drain voltage 3 <sup>rd</sup> stage	4.0	V
VD4	DC Drain voltage 4 <sup>th</sup> stage	4.0	V

## Device thermal performance

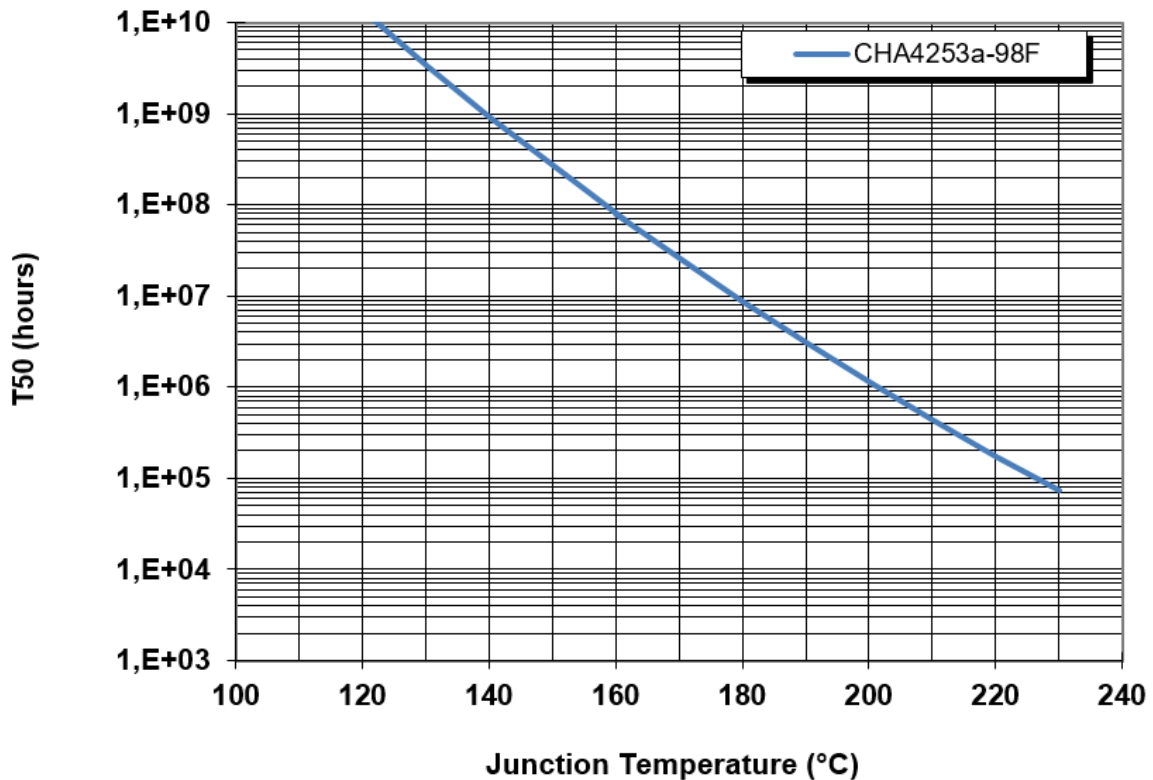
All the figures given in this section are obtained assuming that the bare die is only cooled down by conduction (no convection mode considered).

The temperature is monitored at the die back-side interface (Tb).

The system maximum temperature must be adjusted in order to guarantee that Tjunction remains below the maximum value specified in the Absolute Maximum Ratings table.

So, the system PCB must be designed to comply with this requirement.

Chip backside temperature	Biasing and operational conditions	Tjunction (°C)	RTH junction to Ground (°C/W)	T50 (hours)
Tb=+85°C	Vd=4V/ Id=445mA P <sub>diss</sub> = 1.45W Pin # 2 dBm Pout=24 dBm (OP1dB)	159	50.9	9E+7
Tb=+95°C	Vd=4V/ Id=445mA P <sub>diss</sub> = 1.45W Pin # 2 dBm Pout=24 dBm (OP1dB)	171	52.2	2E+7



**Typical test fixture Sij parameters**

Tamb.= +25°C, Vd = +4.0V, Id = 230mA

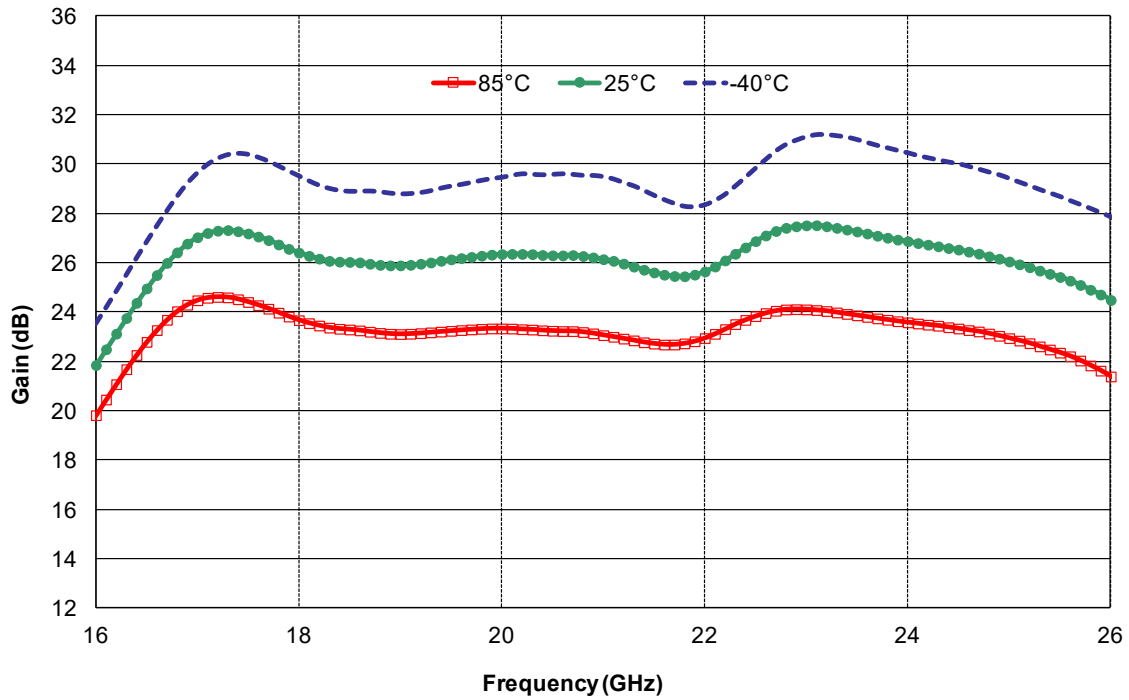
Freq (GHz)	S11 (dB)	PhS11 (°)	S12 (dB)	PhS12 (°)	S21 (dB)	PhS21 (°)	S22 (dB)	PhS22 (°)
2.0	-1.07	51.8	-66.97	-33.1	-64.70	-34.8	-1.07	51.8
3.0	-1.11	-11.8	-64.40	-90.1	-62.75	-92.3	-1.09	-12.7
4.0	-1.15	-77.7	-67.40	-143.8	-70.76	90.0	-1.05	-79.3
5.0	-1.73	-146.3	-68.84	168.0	-60.37	-70.1	-1.34	-148.9
6.0	-2.39	146.1	-83.79	110.7	-29.73	162.8	-1.58	137.4
7.0	-2.61	78.1	-81.63	148.6	-21.97	7.9	-1.81	60.9
8.0	-2.95	9.2	-76.04	-52.5	-15.62	-117.4	-2.05	-17.7
9.0	-3.65	-61.9	-61.40	-134.8	-9.79	124.9	-2.63	-99.4
10.0	-4.96	-141.5	-53.62	147.8	-4.76	7.9	-3.89	173.6
11.0	-7.40	-124.7	-52.69	88.9	-0.90	-82.3	-5.79	81.1
12.0	-7.90	87.3	-49.84	1.0	3.30	157.8	-7.57	-10.6
13.0	-8.47	3.9	-52.16	-59.4	6.86	53.8	-9.16	-94.2
14.0	-9.19	-70.3	-53.98	-99.4	10.94	-46.6	-11.64	-169.4
15.0	-10.63	-139.6	-54.98	-134.9	15.87	-148.3	-16.51	124.2
16.0	-13.72	154.0	-54.40	-171.1	21.86	100.7	-27.84	121.1
17.0	-15.71	132.2	-54.45	147.9	27.04	-36.2	-15.95	127.3
18.0	-11.14	67.4	-54.88	114.7	26.41	-172.5	-12.19	58.3
19.0	-11.04	5.5	-55.21	90.3	25.90	74.9	-11.70	1.6
20.0	-12.17	-39.1	-52.71	54.1	26.36	-37.7	-13.05	-50.1
21.0	-12.37	-68.8	-49.81	20.1	26.15	-151.6	-16.02	-67.7
22.0	-10.23	-108.8	-48.17	-46.8	25.65	104.7	-11.46	-98.3
23.0	-17.62	-163.2	-53.25	-93.9	27.52	-11.7	-15.70	-146.3
24.0	-15.32	-131.2	-52.07	-105.3	26.88	-133.2	-16.27	-145.8
25.0	-9.99	-168.9	-51.79	-141.5	26.06	105.7	-10.91	-160.9
26.0	-8.17	126.0	-49.56	-153.4	24.49	-20.5	-6.82	136.4
27.0	-9.05	45.7	-44.13	166.0	20.66	-148.9	-6.10	52.1
28.0	-9.66	-30.2	-40.51	105.0	15.31	94.2	-6.26	-32.5
29.0	-8.13	-97.8	-38.79	31.6	9.93	-14.0	-5.33	-103.9
30.0	-5.76	-162.0	-41.01	-35.6	4.38	-119.1	-3.89	-166.5
31.0	-4.47	137.5	-44.25	-93.3	-1.54	142.4	-2.98	137.8
32.0	-4.20	78.5	-49.31	-139.5	-7.18	49.5	-2.63	84.9
33.0	-4.54	17.2	-56.22	-165.7	-12.39	-40.7	-2.62	29.5
34.0	-4.94	-45.9	-59.42	-136.5	-17.40	-128.1	-2.57	-28.3
35.0	-5.75	-109.1	-51.36	-101.8	-22.45	149.4	-2.48	-86.5
36.0	-7.06	-172.4	-39.82	-150.9	-28.69	75.1	-2.41	-144.8
37.0	-9.37	126.4	-33.50	114.3	-33.02	34.4	-2.31	161.4
38.0	-15.98	61.3	-35.77	32.6	-36.77	-39.2	-2.17	111.6
39.0	-17.26	175.7	-38.75	-21.1	-49.02	-92.9	-2.27	60.8
40.0	-7.28	106.7	-40.00	-49.6	-44.29	-16.7	-2.56	9.7

## Typical Test Fixture Measurements

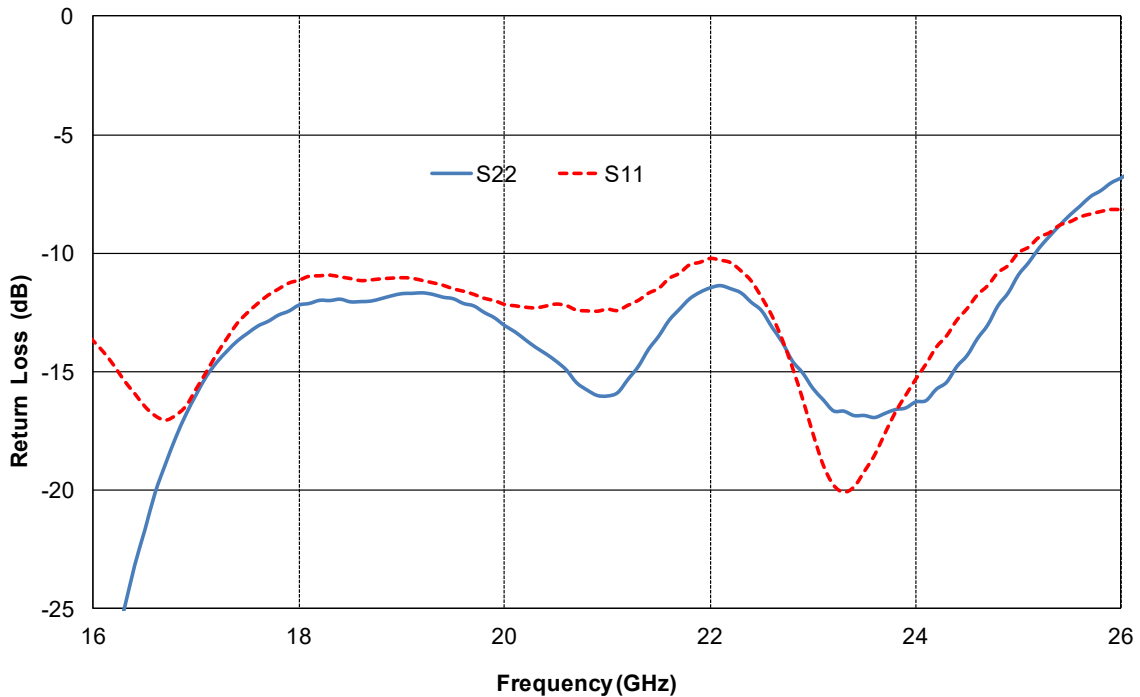
Tamb.= +25°C, Vd = +4.0V, Id = 230mA

These values are representative of test fixture measurements.

### Linear Gain versus Frequency in Temperature



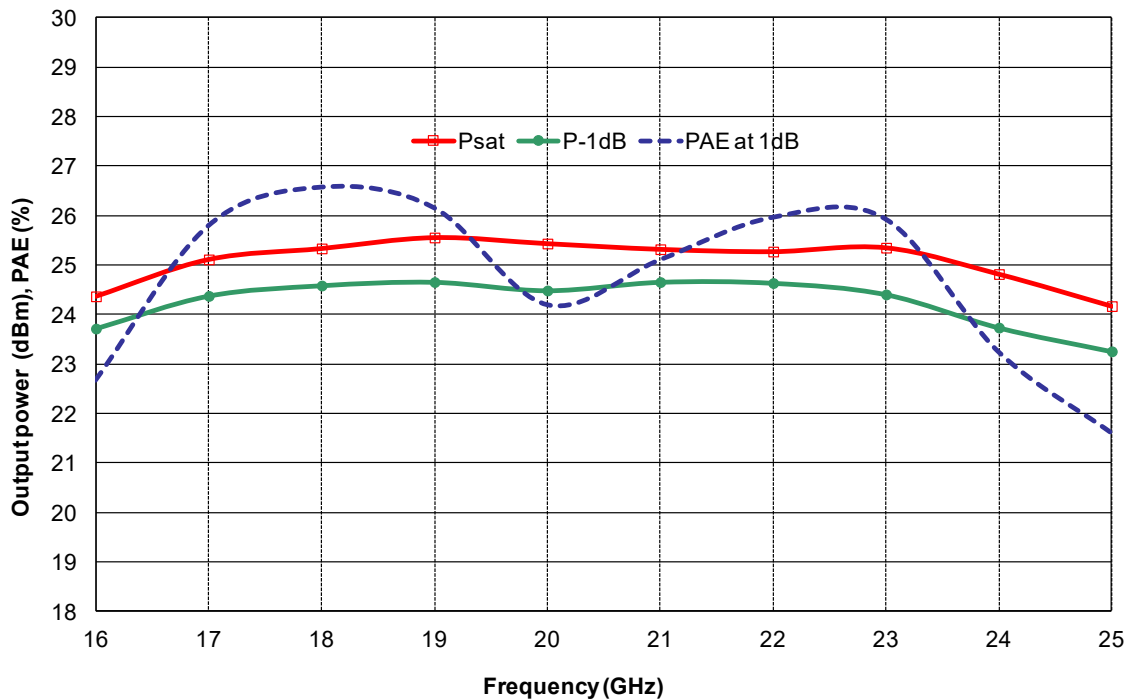
### Return losses versus Frequency



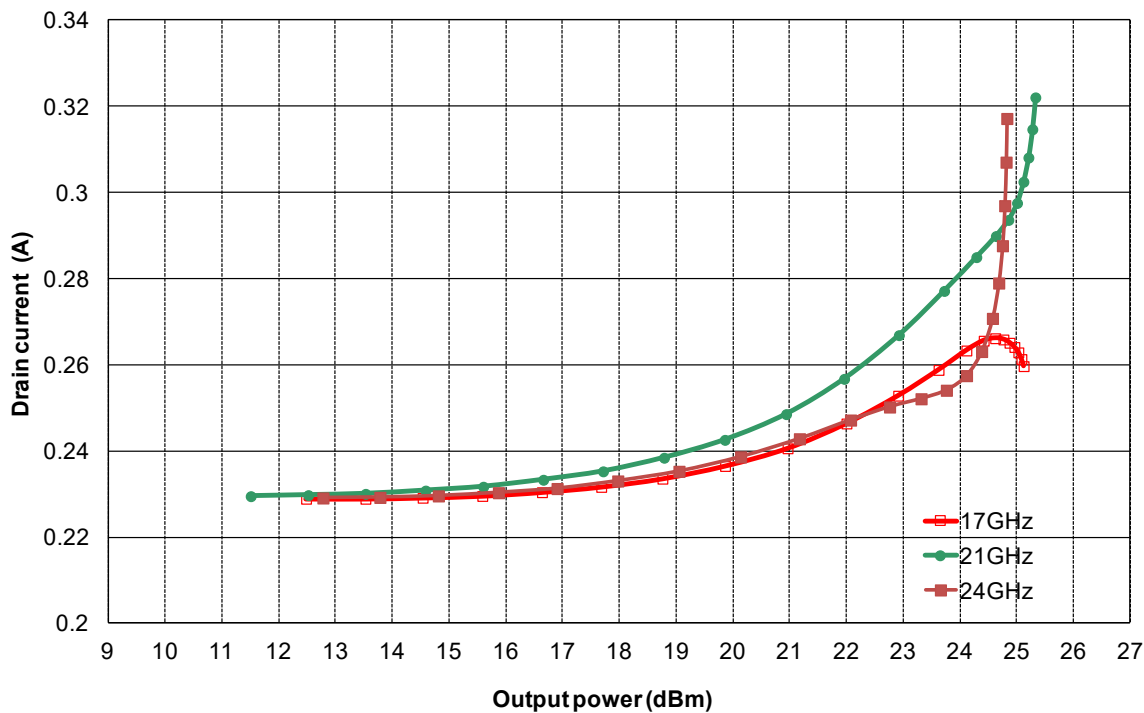
### Typical Board Measurements

Tamb.= +25°C, Vd = +4.0V, Id = 230mA

Output power & PAE versus Frequency



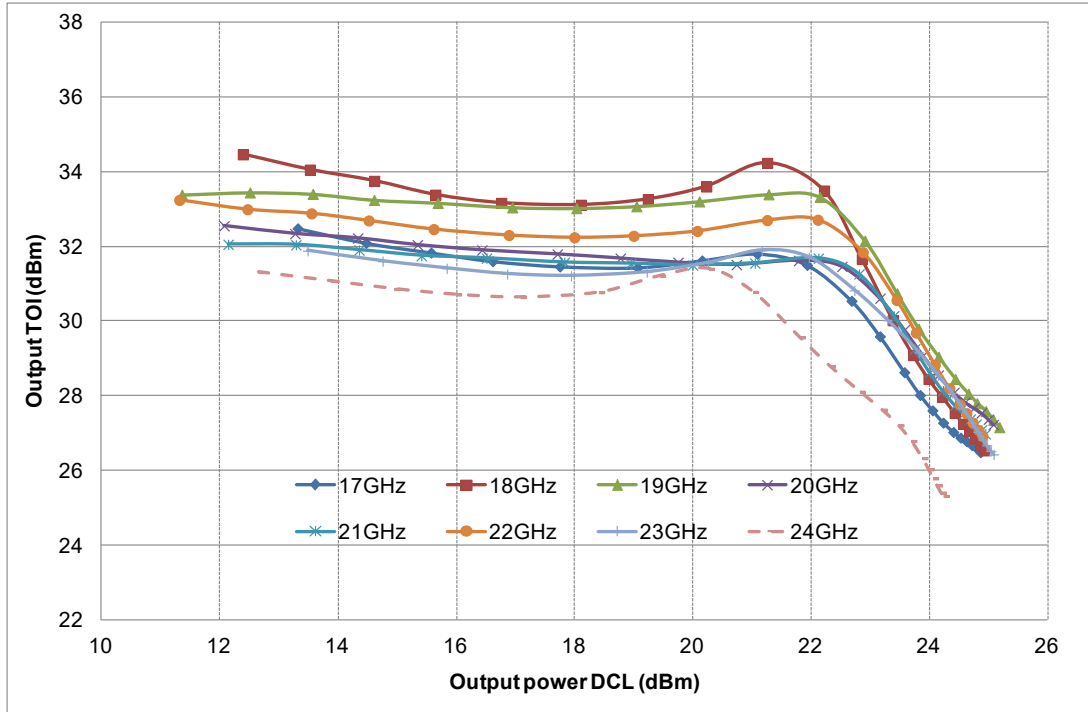
Current versus Output Power



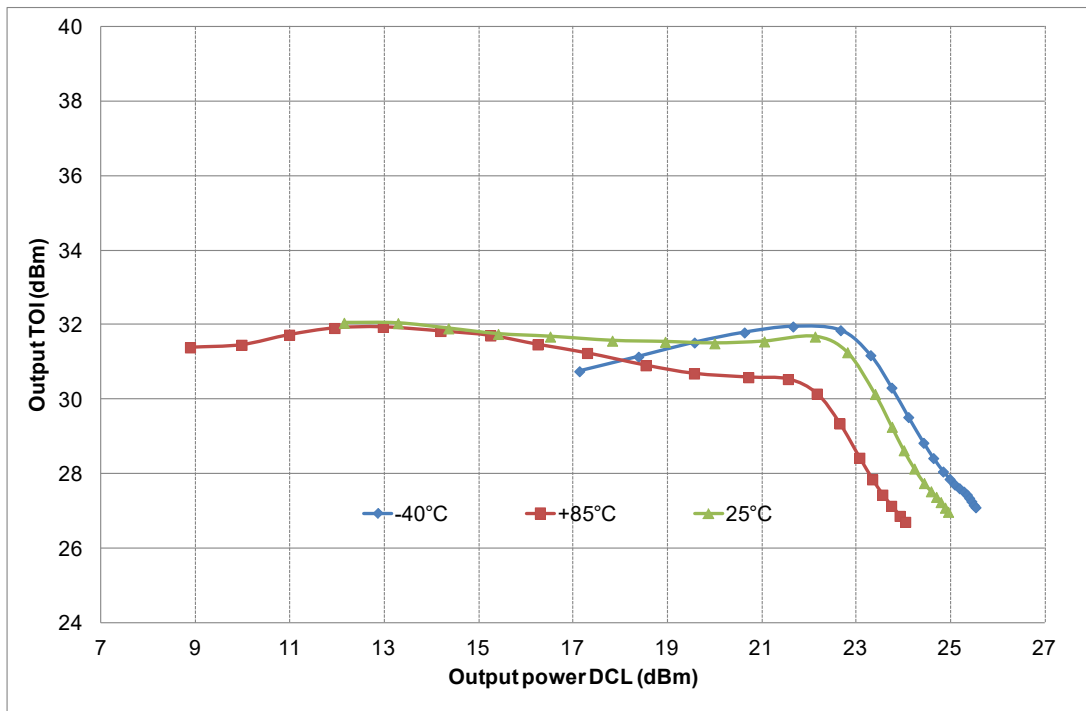
## Typical Board Measurements

Tamb.= +25°C, Vd = +4.0V, Id = 230mA

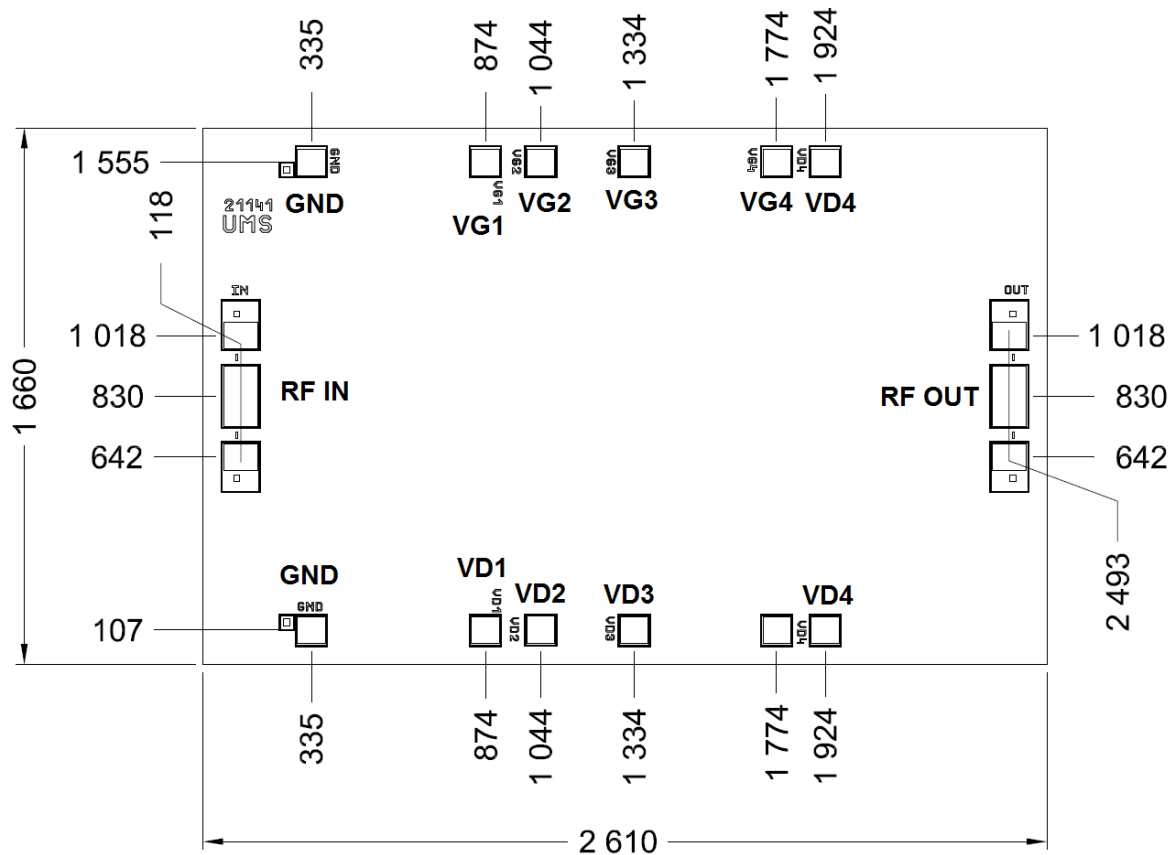
### Output TOI versus Output Power DCL & Frequency



### Output TOI versus Output Power DCL in Temperature at 21GHz

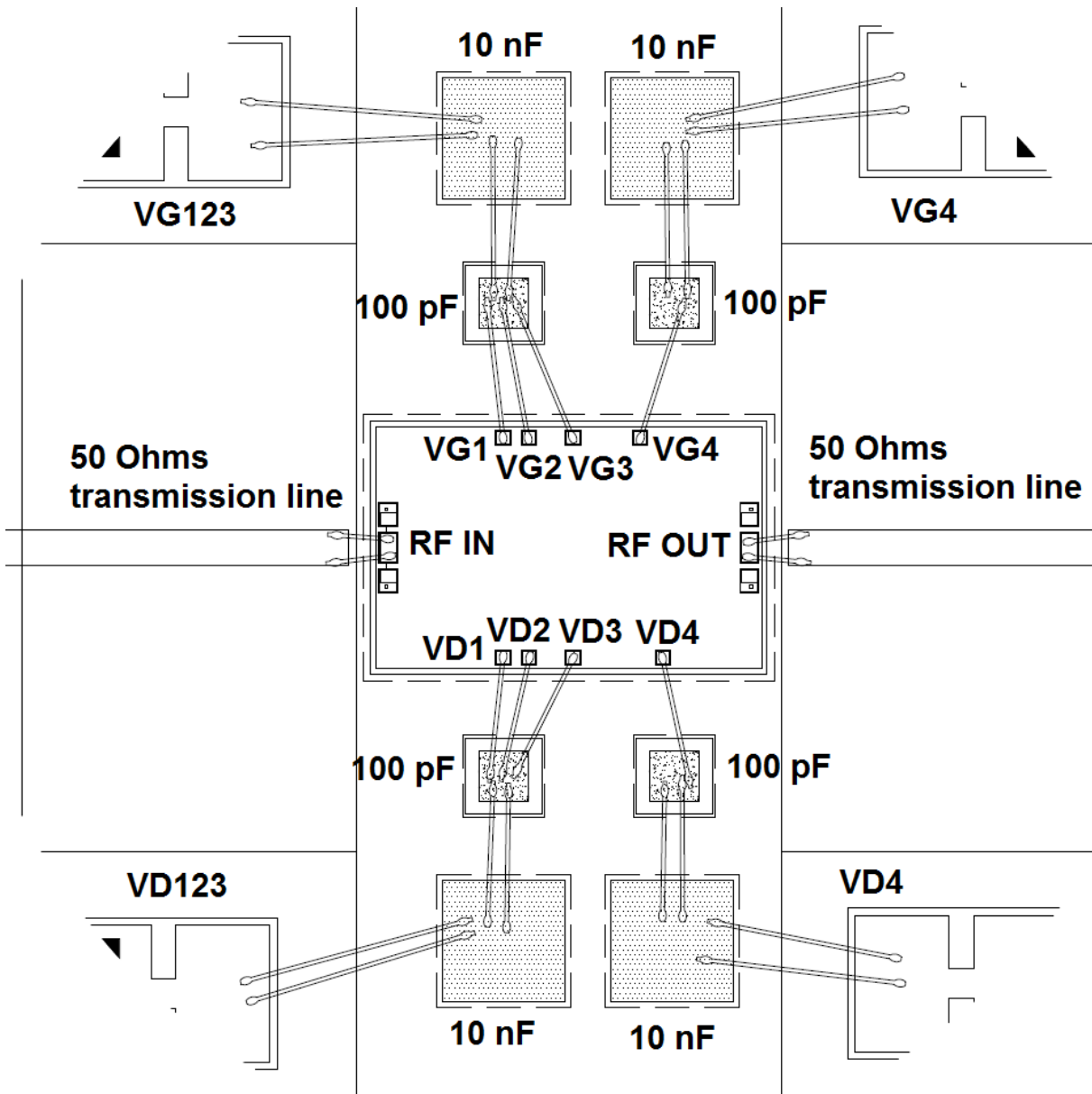


**Mechanical data**



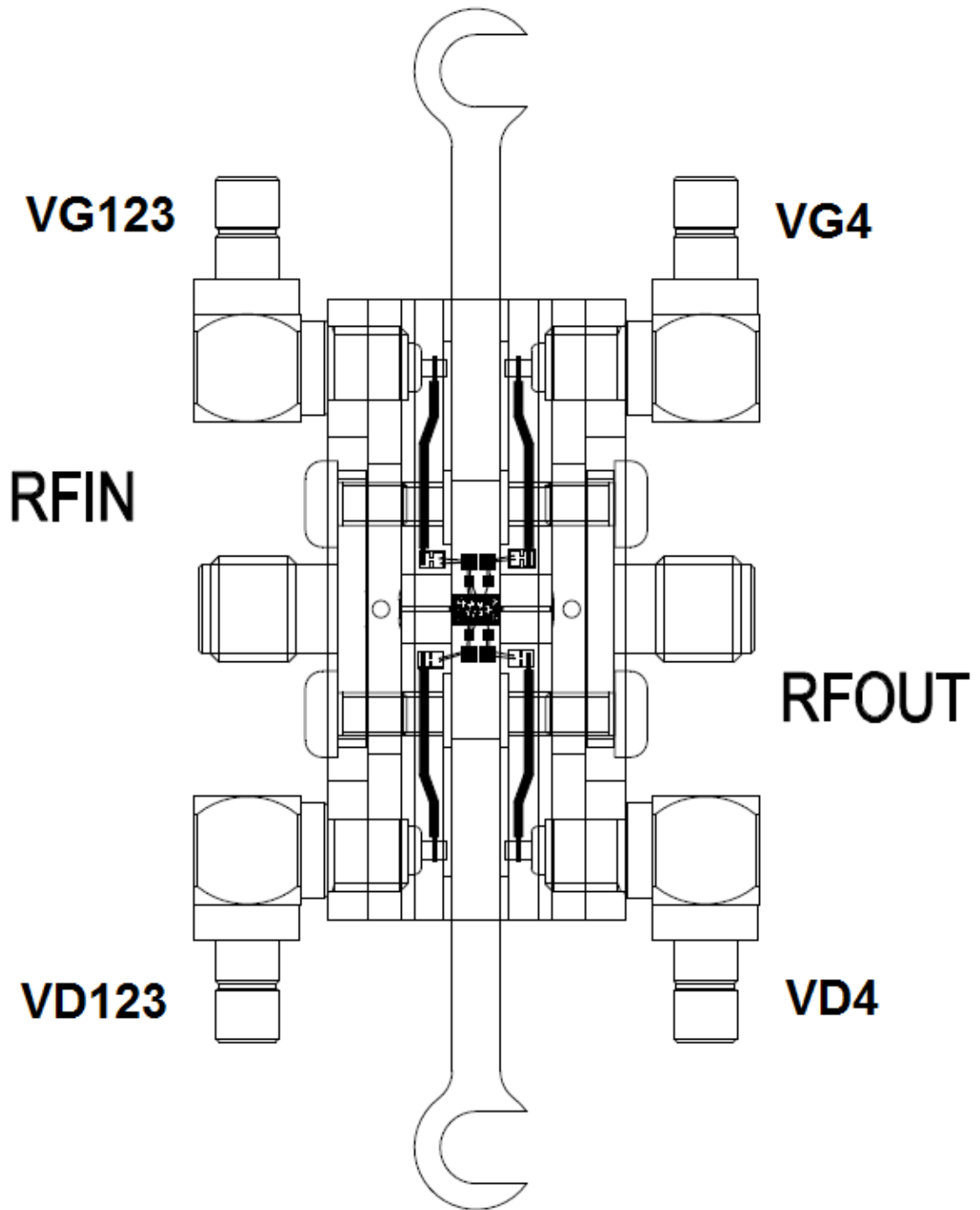
Chip thickness: 70μm.  
 Chip size: 2610x1660 ±35μm  
 All dimensions are in micrometers

## Recommended assembly plan

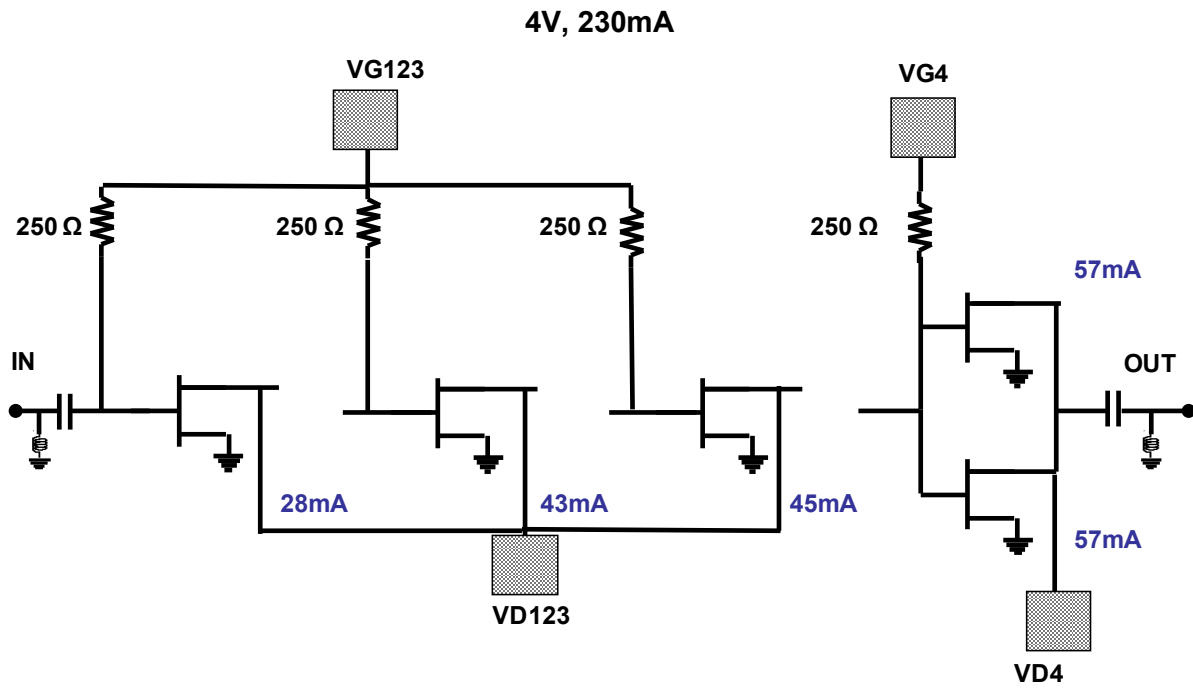


Note: Supply feed should be bypassed. 25µm diameter gold wire is to be preferred.

**Evaluation test fixture**



## DC Schematic



**Notes**

## Recommended reflow process assembly

Refer to the application note AN0001 available at <https://www.ums-rf.com> for die attach.

## Recommended ESD management

Refer to the application note AN0020 available at <https://www.ums-rf.com> for ESD sensitivity and handling recommendations for the UMS products.

## Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACH N°1907/2006. More environmental data are available in the application note AN0019 also available at <https://www.ums-rf.com>.

## Ordering Information

Chip form:

CHA4253a98F/00

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