United Monolithic Semiconductors

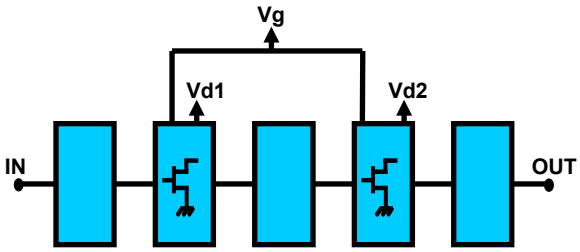
CHA4107-99F

4.5-6.5GHz Medium Power Amplifier

GaAs Monolithic Microwave IC

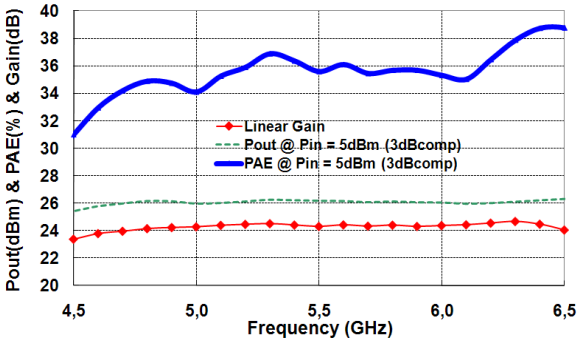
Description

The CHA4107-99F is a monolithic two stage power amplifier designed for C-Band applications.
The MPA provides typically 26dBm output power associated to 35% power added efficiency at 3dBcomp.
The circuit is manufactured with a pHEMT process, 0.25µm gate length, via holes through the substrate, air bridges and electron beam gate lithography. It is available in chip form.



Main Features

- Frequency band: 4.5-6.5GHz
- 26dBm @ 3dBcomp
- 24.5 dB Linear Gain
- High PAE: 35% for +5dBm input power
- Pin max=15 dBm
- DC bias: Vd=8V@Id=115mA
- Chip size 2.37x1.5x0.07mm



Main Characteristics

Vd = 8V, Idq (Quiescent) = 115 mA, Drain Pulse width = 45µs, Duty cycle = 12%

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	4.5		6.5	GHz
Gain	Linear Gain		24.5		dB
NF	Noise Figure		5		dB
Pout	Output Power @ 3dB comp.		26		dBm

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Electrical Characteristics

Vd = 8V, Idq (Quiescent) = 115 mA, Drain Pulse width = 45µs, Duty cycle = 12%

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	4.5		6.5	GHz
Gain	Linear Gain		24.5		dB
NF	Noise Figure		5		dB
RLin	Input Return Loss		13		dB
RLout	Output Return Loss		8		dB
P_1dBc	Output power @ 1dBcomp		25		dBm
P_3dBc	Output power @ 3dBcomp		26		dBm
PAE_3dBc	Power Added Efficiency @ 3dBc		35		%
Id_3dBc	Supply drain current @ 3dBc		130		mA
Vd1, Vd2	Drain supply voltage		8		V
Id	Supply quiescent current (1)		115		mA
Vg	Gate supply voltage		-0.8		V

These values are representative of on-Jig measurements.
(1) Parameter can be adjusted by tuning of Vg.

Recommended Operating Ratings

Tbackside= +25°C

Symbol	Parameter	Values	Unit
Vd	Drain voltage	8	V
Ig	Gate current	10	mA
Tj	Maximum junction temperature	175	°C

Operation of this device above anyone of these parameters may degrade the component lifetime.

Absolute Maximum Ratings (1)

Tbackside= +25°C

Symbol	Parameter	Values	Unit
Cmp	Compression level (2)	6	dB
Vd	Drain voltage	9.5	V
Id	Drain quiescent current	250	mA
Id_sat	Drain current in saturation	350	mA
Vg	Gate voltage	[-3.0; 0]	V
Pin	Maximum peak input power overdrive	15	dBm
Tstg	Storage temperature range	-55 to +150	°C
Top	Operating temperature range	-40 to +85	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.
(2) For higher compression the level limit can be increased by decreasing the voltage Vd using the rate 0.5V/dBcomp.

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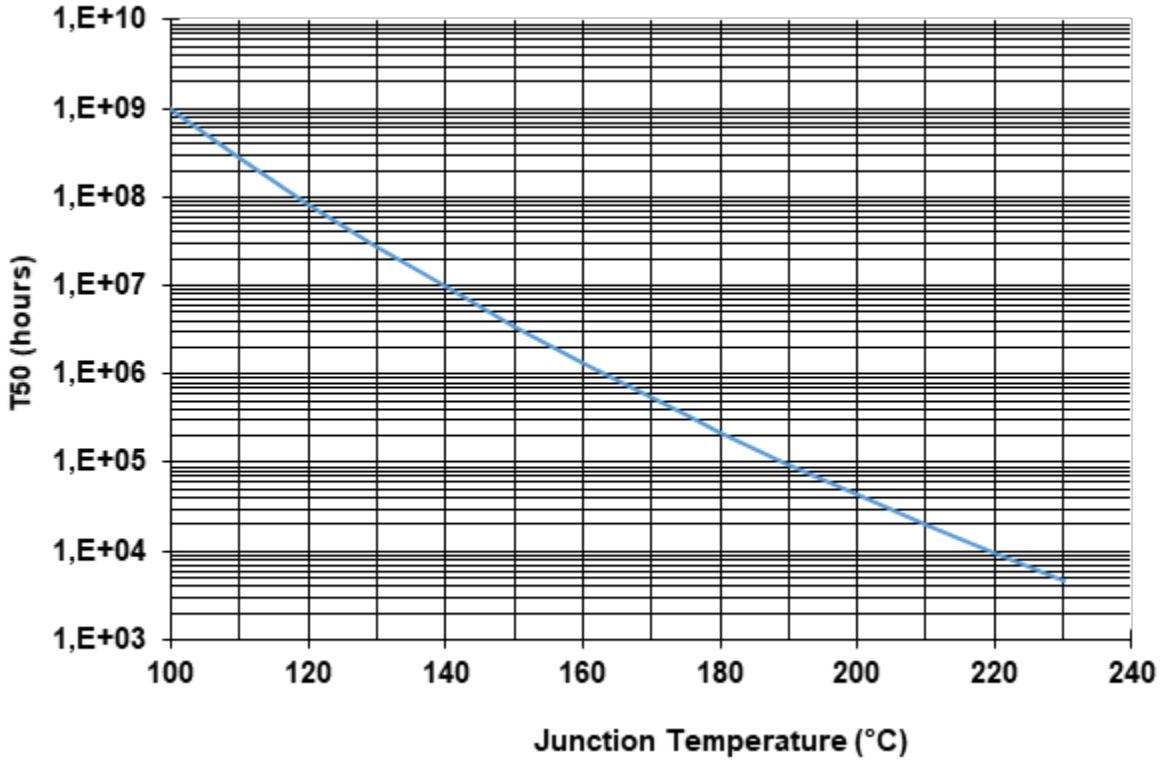
Device Thermal Performance

All the figures given in this section are obtained assuming that the die is only cooled down by conduction through the package case.
The temperature is monitored at the chip backside interface (T_b).
For nominal operation, the system's maximum temperature must be adjusted to ensure that the junction temperature ($T_{junction}$) remains below the maximum value specified in the Recommended Operating Ratings table.

Parameter	Conditions	$T_{junction}$ (°C)	RTH (°C/W)	T50 (hours)
RTH (1) Thermal Resistance (Junction to Case)	CW Mode: Low level input power Vd = 8V, Pdiss=0.8W	166	101	7.71E+05
	Pulse mode (25µs/10%): Low level input power Vd = 8V, Pdiss=0.8W	156	88	1.96E+06
	CW Mode: saturation (3dB gain compression) Vd = 8V, Pdiss=0.71W	160	106	1.34E+06
	Pulse mode (25µs/10%): saturation Vd = 8V, Pdiss=0.71W	153	96	2.62E+06

(1) Assuming 85°C on T_b.



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Typical on-wafer Sij parameters

Tbackside= +25°C, Vd = +8V, Idq = 115mA

Freq (GHz)	S11 (dB)	PhS11 (°)	S12 (dB)	PhS12 (°)	S21 (dB)	PhS21 (°)	S22 (dB)	PhS22 (°)
2.00	-3.71	-43.44	-63.21	-139.00	5.79	166.00	-8.39	31.33
2.40	-3.85	-49.94	-63.68	-72.72	10.38	95.99	-7.92	-25.37
2.80	-4.02	-57.93	-63.92	164.50	12.30	48.66	-10.56	-34.55
3.20	-4.46	-69.48	-48.25	120.80	14.21	11.12	-10.62	-29.96
3.60	-5.24	-83.39	-60.90	170.80	16.68	-23.41	-9.14	-30.55
4.00	-7.12	-97.66	-70.26	-57.20	19.36	-59.84	-8.22	-43.06
4.40	-10.98	-106.30	-52.87	-7.31	21.91	-103.70	-8.02	-56.73
4.80	-13.83	-90.00	-48.62	22.44	23.30	-150.90	-8.67	-68.98
5.20	-12.93	-82.05	-49.80	-23.29	23.52	163.50	-9.11	-79.47
5.60	-13.52	-85.54	-57.81	-65.50	23.52	121.40	-8.78	-92.08
6.00	-14.21	-73.76	-49.52	-124.40	23.65	77.11	-8.20	-113.30
6.40	-11.03	-69.98	-51.47	-177.10	23.16	28.73	-8.47	-141.30
6.80	-8.33	-89.16	-52.36	159.00	21.03	-21.97	-10.46	-173.00
7.20	-7.75	-112.90	-63.26	142.80	17.81	-66.68	-12.94	164.30
7.60	-7.77	-130.30	-69.48	2.62	14.02	-103.70	-14.57	143.70
8.00	-7.68	-148.30	-53.55	121.40	10.28	-136.90	-15.74	130.80
8.40	-7.21	-166.40	-59.68	8.18	6.56	-166.10	-14.85	120.40
8.80	-6.84	175.30	-51.19	138.20	2.62	166.90	-14.71	114.80
9.20	-6.19	159.50	-50.78	-51.15	-1.14	143.70	-13.35	106.30
9.60	-5.86	143.80	-55.03	-47.20	-4.96	122.70	-12.13	98.57
10.00	-5.46	128.60	-52.40	-146.90	-8.67	103.10	-10.43	91.47
10.40	-4.84	116.20	-62.55	-176.60	-12.02	85.93	-9.05	85.73
10.80	-4.77	104.70	-48.22	-131.80	-15.66	70.81	-8.17	78.93
11.20	-3.96	93.63	-48.09	-93.38	-18.84	54.85	-7.21	71.07
11.60	-3.67	87.22	-48.28	55.47	-21.78	41.57	-6.18	62.82
12.00	-3.37	75.38	-59.40	173.70	-25.54	29.73	-5.44	60.08
12.40	-3.35	70.02	-52.11	-103.20	-28.37	20.69	-4.30	52.83
12.80	-3.11	57.48	-43.51	175.10	-31.95	0.60	-3.94	47.00
13.20	-1.64	56.46	-44.50	55.48	-32.32	-8.66	-3.00	35.69
13.60	-1.74	48.11	-45.37	141.30	-37.42	-26.74	-3.14	26.64
14.00	-1.83	43.10	-53.12	119.10	-39.44	-40.94	-2.82	24.77

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Typical on-wafer Sij parameters

Tbackside= +25°C, Vd = +8V, Idq = 115mA

Freq (GHz)	S11 (dB)	PhS11 (°)	S12 (dB)	PhS12 (°)	S21 (dB)	PhS21 (°)	S22 (dB)	PhS22 (°)
14.40	-1.57	41.82	-56.19	59.72	-46.09	-48.43	-1.59	19.73
14.80	-1.17	32.98	-40.02	-169.00	-51.16	-127.00	-1.49	15.50
15.20	-1.84	24.26	-40.17	-71.68	-47.88	-59.04	-2.12	11.99
15.60	-0.89	19.12	-51.96	-16.02	-49.10	-76.69	-1.77	4.34
16.00	-1.09	26.33	-54.17	-178.80	-42.14	-83.60	-0.50	2.88
16.40	-1.09	9.86	-51.44	174.50	-50.02	157.60	-1.75	-3.97
16.80	-0.36	8.65	-44.47	-19.29	-45.84	-16.49	-0.61	-10.70
17.20	-0.85	6.22	-44.09	60.04	-53.59	50.86	-0.66	-9.31
17.60	-0.31	-2.44	-46.94	8.43	-48.01	97.35	-1.29	-18.54
18.00	-0.86	-0.40	-47.33	-162.90	-48.23	69.86	-0.66	-20.51

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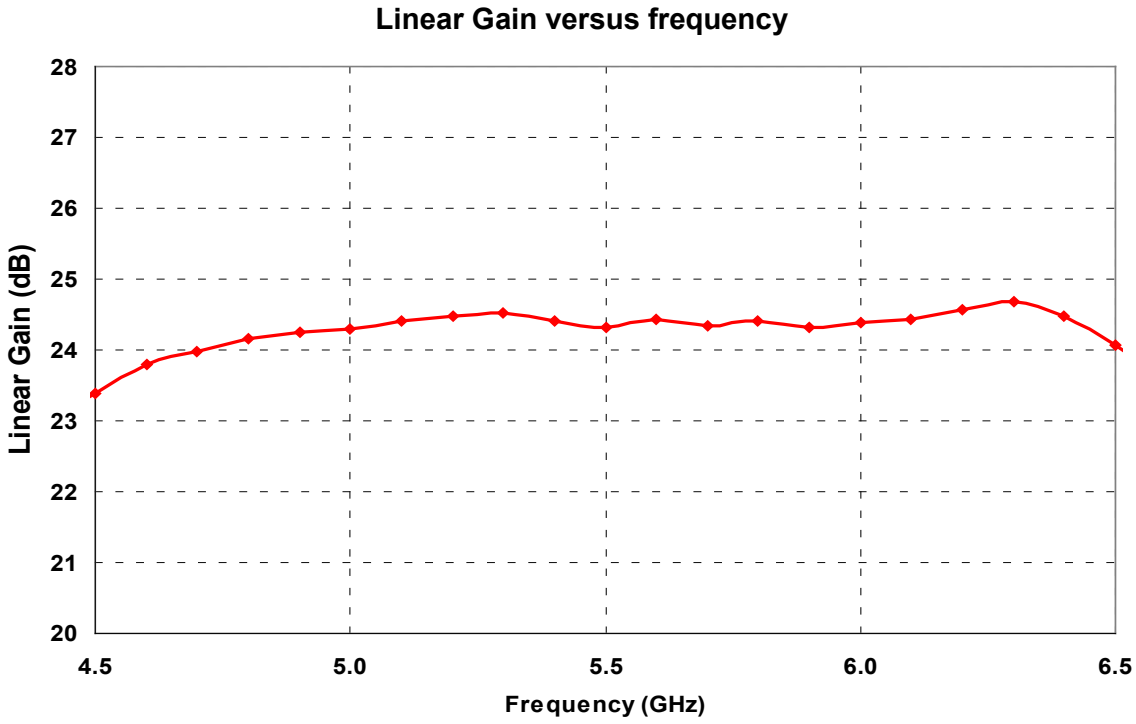
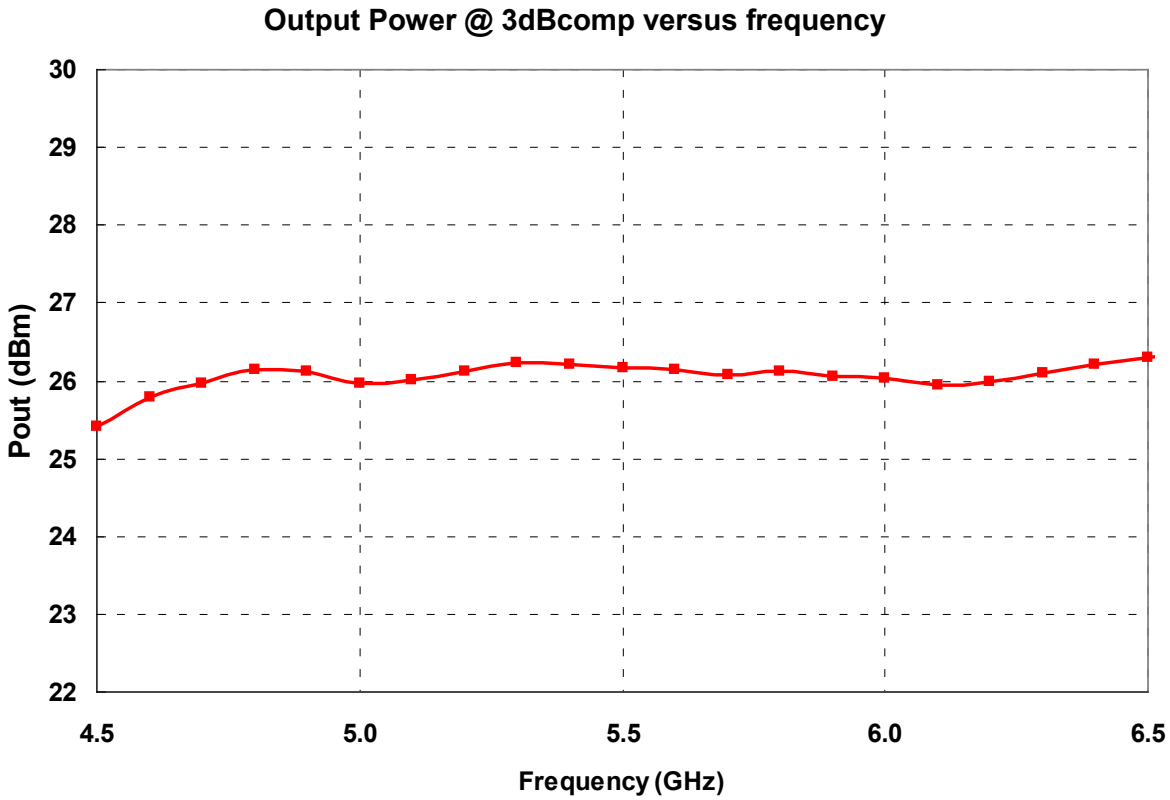
Typical on Jig Measurements

Tbackside= +25°C,
Vd = 8V, Idq (Quiescent) = 115mA, Drain Pulse width = 45µs, Duty cycle = 12%





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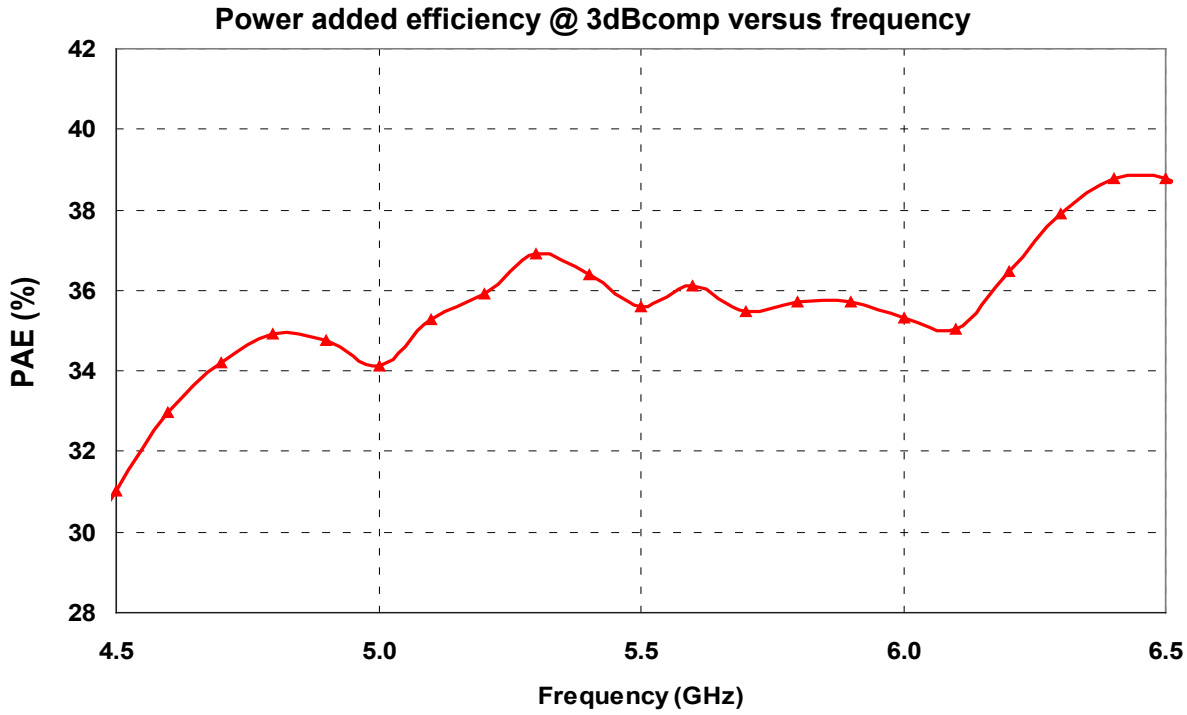

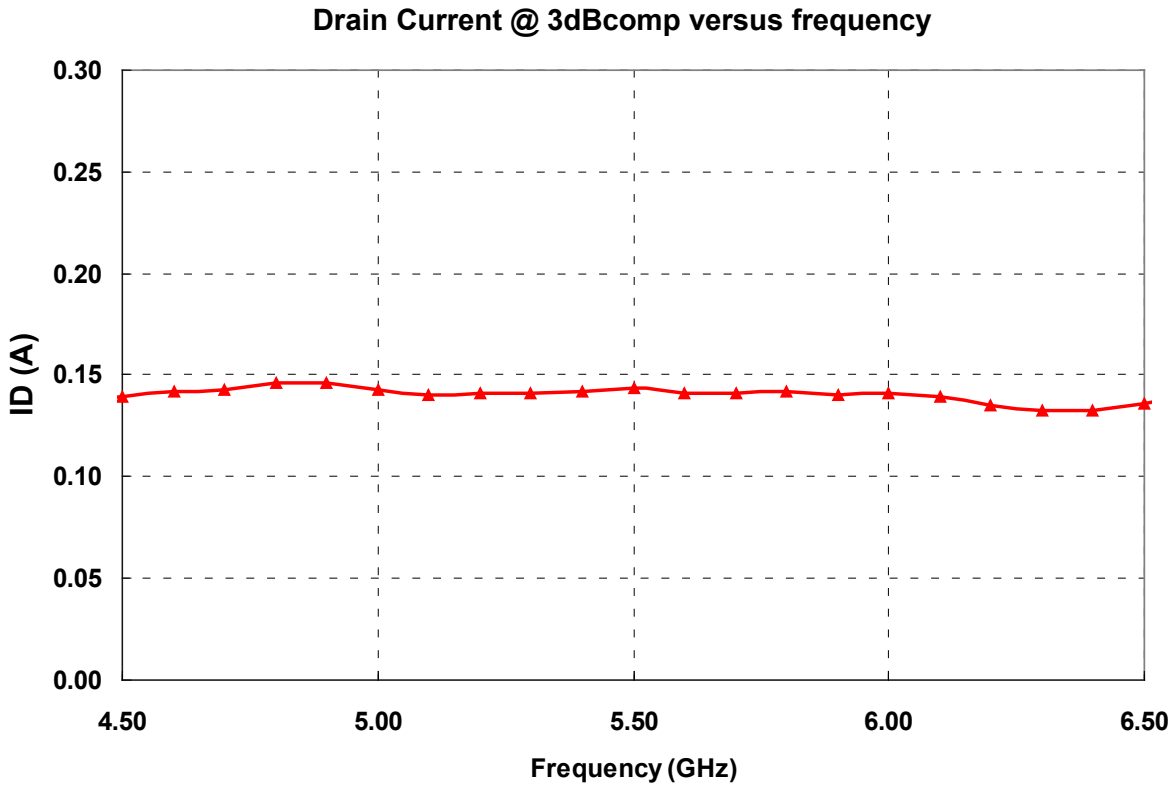

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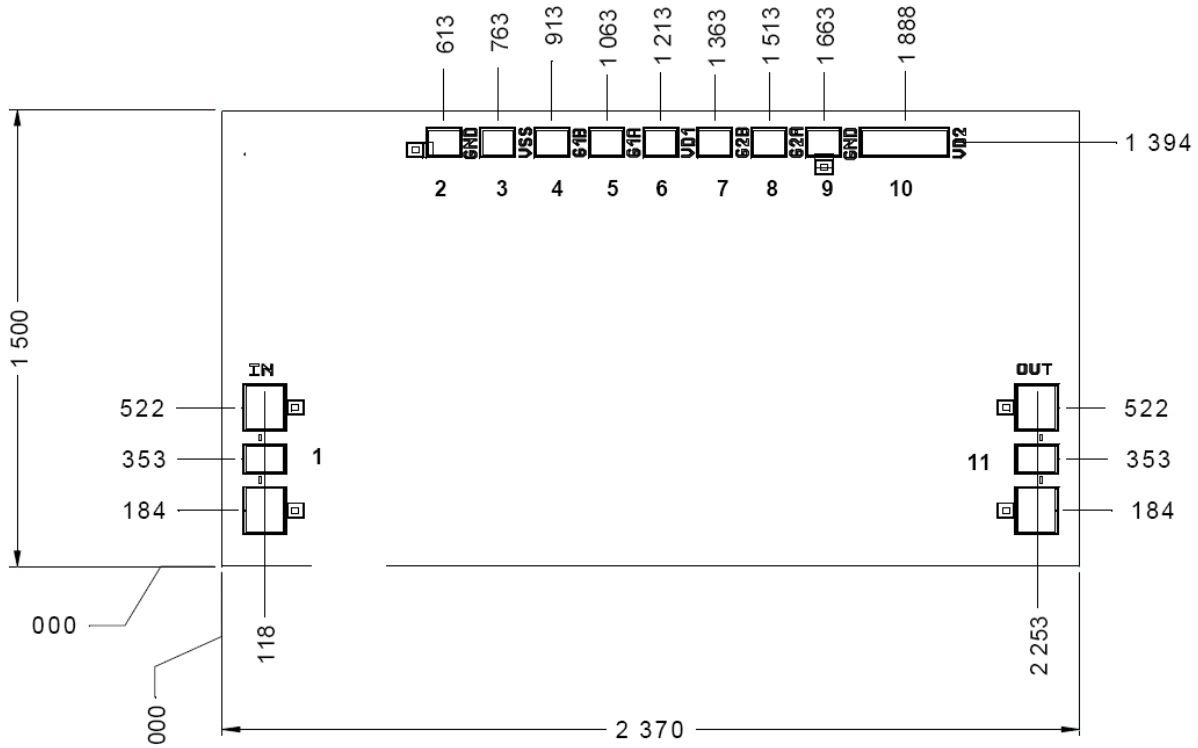
Mechanical data



UNITS : µm
Tol : ± 35µm

All dimensions are in micrometers
Chip size = 1500x2370 ±35µm
Chip thickness = 70µm ±10µm
RF pads (1, 12) = 100 x 122µm²
DC pads (3, 6, 8, 11) = 100 x 100µm²
Chip width and length are given with a tolerance of ±35µm

Pin number	Pin name	Description
1	IN	RF Input
3, 4, 7, 8	Vss, G1B, G2B, G2A	NC
5	G1A	Vg
2, 9	GND	NC
6, 10	VD1, VD2	Vd
11	OUT	RF Output

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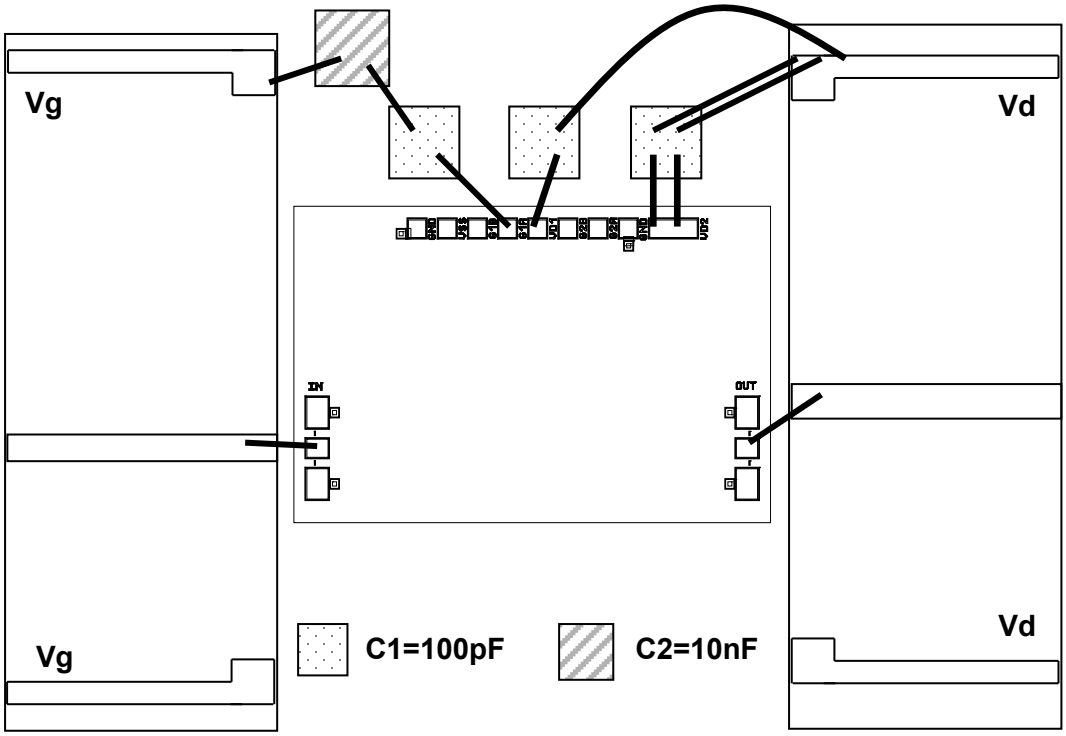
Recommended assembly plan



Pads G1A (pin 5) & G2A (pin 8) are connected inside the chip, The CHA4107 could be used without G2A bias. There is a resistor bridge inside the chip. This one generates the correct value of G1A Bias. Equivalent RF Wire Bonding: 0.2nH (typical length of 200µm for a 25µm diameter wire).

For a Drain pulse configuration:

On Drain access: 100pF is requested on Vd1 pad and 100pF requested on Vd2 pad

On Gate access: 100pF and 10 nF are requested on Vg1A Pad. Additional 1µF capacitor may be needed for stability purpose, depending on customer configuration.

Bonding recommendations

Port	Connection	External capacitor
IN	Inductance (Lbonding) = 0.2nH 1 gold wire with diameter of 25µm	
OUT	Inductance (Lbonding) = 0.2nH 1 gold wire with diameter of 25µm	
Vg	Inductance ≤ 1nH	C1 ~ 100pF, C2 ~ 10nF
Vd	Inductance ≤ 1nH	C1 ~ 100pF

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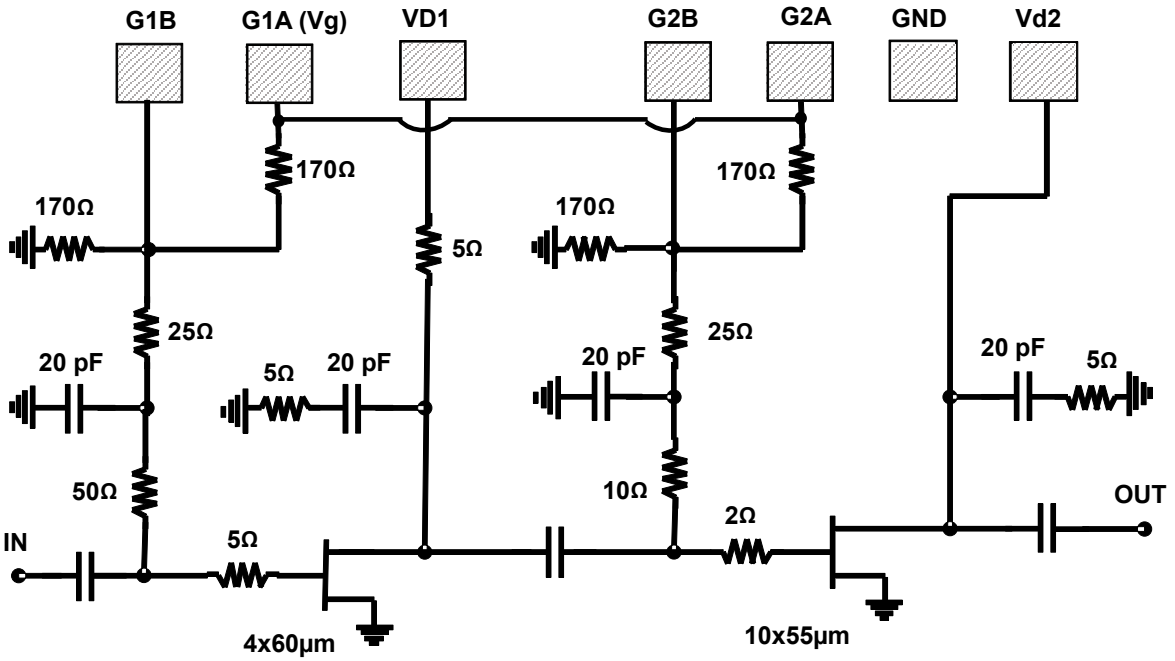
DC Schematic

Medium Power Amplifier: 8V, 115mA



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Notes

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Recommended ESD management

Refer to the application note AN0020 available at https://www.ums-rf.com for ESD sensitivity and handling recommendations for the UMS products.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at https://www.ums-rf.com.

Ordering Information

Chip form:	CHA4107-99F/00

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