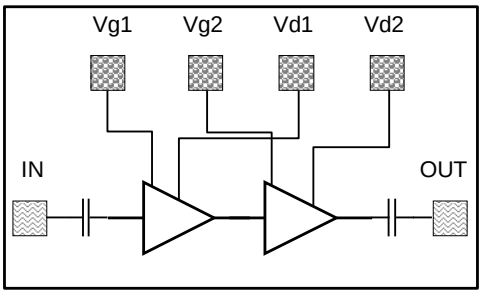
CHA3218-99F

2-18GHz Low Noise Amplifier

GaAs Monolithic Microwave IC

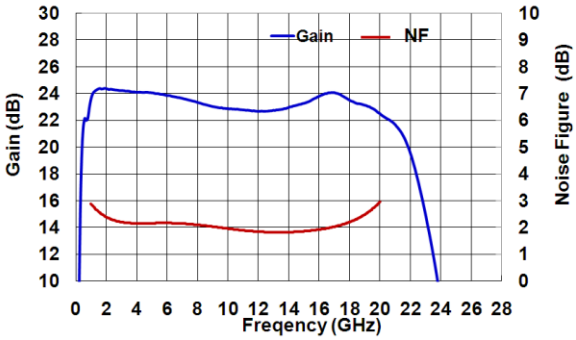
Description

The CHA3218-99F is a two stage very wide band Low Noise Amplifier.
The wide frequency band associated to a 2dB low noise figure makes this circuit very versatile for very high performance systems.
It is designed for a wide range of applications, from military to commercial communication systems.
The circuit is manufactured with a pHEMT process, 0.15µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.
It is available in chip form.



Main Features

- Broadband performances: 2-18GHz
- Noise figure : 2dB
- Output power: 15dBm @ 1dBcomp
- Linear gain: 24dB
- High linearity: 25dBm
- Quiescent bias point: Vd=4V, Id=120mA
- Chip size 3.07x1.57x0.1mm



Main Electrical Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	2		18	GHz
Gain	Linear Gain		24		dB
NF	Noise Figure		2		dB
Pout	Output Power @1dB comp.		15		dBm

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Electrical Characteristics

Tamb.= +25°C, Vd = +4V

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Operating frequency	2		18	GHz
G	Small Signal Gain		24		dB
S11	Input Return Loss from 2GHz to 16GHz Input Return Loss from 16GHz to 18GHz		8 4		dB
S22	Output Return Loss		12		dB
NF	Noise Figure		2		dB
P1dB	Output power at 1dB gain compression		15		dBm
OIP3	Output 3rd order intercept point		25		dBm
Vd	Positive supply voltage		4		V
Vg	Negative supply voltage		-0.45V		V
Id	Positive supply DC current		120		mA

These values are representative of measurements made in test fixture that are made with bonding wires at the RF ports.

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Absolute Maximum Ratings (1)

Tamb.= +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	6V	V
Id	Drain bias current	200	mA
Vg	Gate bias voltage	-2 to -0.3	V
Tj	Junction temperature (2)	175	°C
Ta	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +150	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.

Typical Bias Conditions

Tamb.= +25°C

Symbol	Pad Nº	Parameter	Values	Unit
Vd	VD1, VD2	Drain supply voltage	4	V
Vg	VG1, VG2	Gate supply voltage	-0.45	V

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Typical on-wafer Sij parameters

Tamb.= +25°C, Vd = +4.0V, Id = 120mA

Freq (GHz)	S11 (dB)	PhS11 (°)	S12 (dB)	PhS12 (°)	S21 (dB)	PhS21 (°)	S22 (dB)	PhS22 (°)
1.0	-6.54	-68.84	-66.51	120.80	20.22	9.61	-10.57	-165.20
1.5	-8.65	-90.41	-69.52	59.25	23.39	-18.22	-12.10	150.90
2.0	-8.98	-101.30	-66.71	-70.17	24.52	-44.21	-13.55	114.90
2.5	-8.81	-111.50	-66.45	-6.78	24.62	-67.98	-14.29	98.03
3.0	-8.84	-121.30	-63.63	31.22	24.81	-90.89	-15.82	82.15
3.5	-8.62	-130.40	-76.10	35.29	24.79	-110.50	-15.54	69.41
4.0	-8.41	-138.90	-82.38	120.20	24.83	-129.90	-15.35	54.40
4.5	-8.34	-146.60	-69.61	170.60	24.85	-149.10	-15.29	43.06
5.0	-8.15	-152.90	-80.83	-158.00	24.88	-167.80	-15.14	31.56
5.5	-8.01	-160.10	-70.41	-142.20	24.93	173.20	-15.48	17.93
6.0	-7.93	-166.70	-76.72	-100.20	24.90	154.10	-15.44	9.39
6.5	-7.88	-173.60	-66.20	-167.50	24.90	135.30	-15.84	1.16
7.0	-7.83	179.50	-74.37	141.10	24.86	116.40	-16.10	-8.84
7.5	-7.77	172.40	-68.59	83.30	24.80	97.70	-16.15	-13.36
8.0	-7.81	164.70	-61.56	22.11	24.76	78.88	-16.93	-19.65
8.5	-7.93	156.50	-74.50	-79.14	24.68	59.95	-17.15	-26.74
9.0	-8.14	148.10	-60.72	13.83	24.58	41.21	-17.41	-28.81
9.5	-8.45	138.90	-61.33	-160.50	24.50	22.53	-17.58	-28.73
10.0	-8.78	129.40	-57.71	61.63	24.40	3.86	-17.91	-30.03
10.5	-9.20	119.60	-66.95	135.60	24.32	-14.76	-17.34	-30.37
11.0	-9.69	109.00	-67.69	-46.82	24.24	-33.33	-17.57	-24.55
11.5	-10.20	98.09	-56.04	116.50	24.17	-51.94	-17.25	-32.41
12.0	-10.67	86.43	-63.65	139.60	24.14	-70.65	-16.07	-28.71
12.5	-10.97	73.94	-63.23	87.11	24.16	-89.46	-16.07	-26.83
13.0	-10.98	61.87	-69.79	-23.20	24.17	-108.70	-15.26	-31.21
13.5	-10.85	49.90	-58.09	26.48	24.25	-128.30	-14.55	-31.53
14.0	-10.26	36.84	-60.33	-45.50	24.32	-148.50	-13.76	-35.57
14.5	-9.52	25.18	-56.67	87.72	24.39	-169.30	-12.82	-38.97
15.0	-8.66	13.53	-56.17	82.83	24.40	169.50	-12.14	-43.52
15.5	-7.37	1.83	-55.80	131.80	24.40	147.50	-11.62	-47.52
16.0	-6.31	-9.73	-68.50	-19.80	24.29	125.20	-10.99	-50.85
16.5	-5.12	-19.29	-54.25	141.00	24.17	102.50	-10.17	-56.71
17.0	-4.21	-30.54	-52.76	-4.26	23.98	79.88	-9.57	-59.52
17.5	-3.42	-40.79	-49.86	-28.50	23.81	56.73	-9.61	-67.15
18.0	-2.70	-50.34	-55.04	163.50	23.55	33.18	-9.34	-75.01
18.5	-2.01	-59.27	-57.27	-112.00	23.28	8.48	-9.76	-77.78
19.0	-1.40	-67.90	-55.13	-111.50	22.96	-17.05	-10.46	-80.96
19.5	-0.89	-76.81	-59.46	52.25	22.21	-40.98	-9.23	-78.01
20.0	-0.44	-84.70	-47.07	-60.90	21.91	-60.36	-8.24	-93.21

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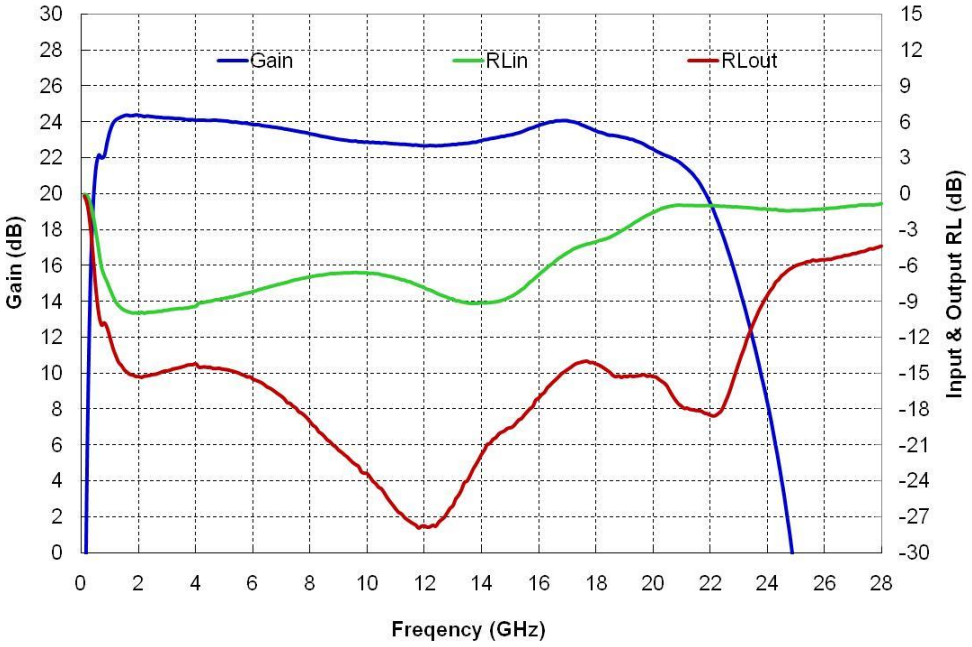
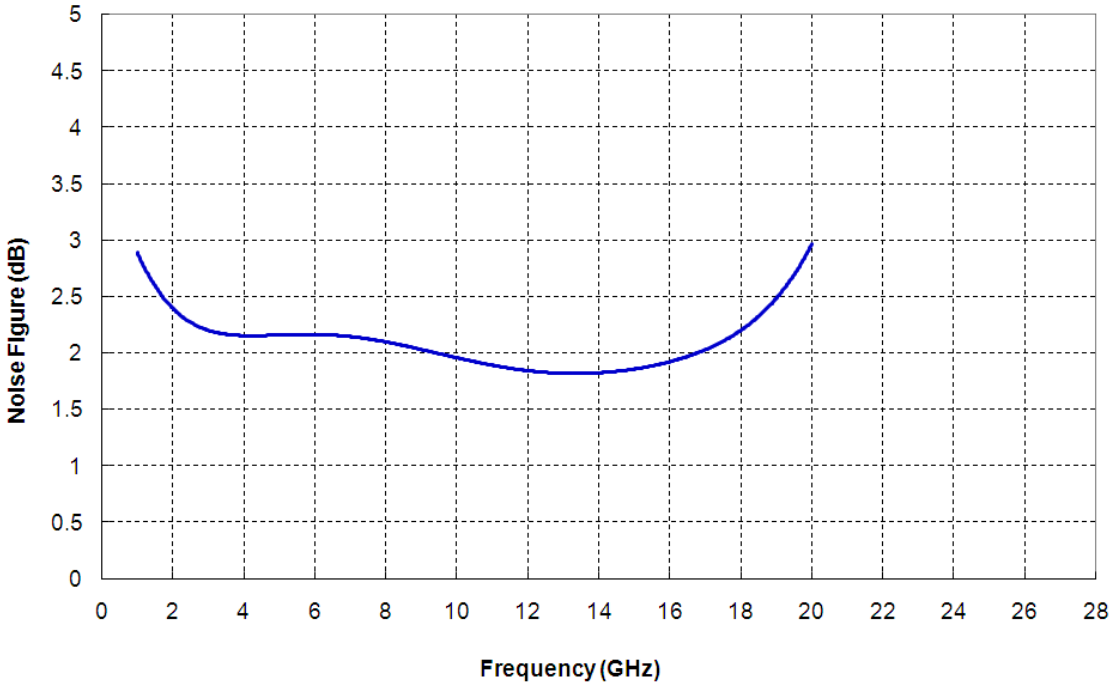
Typical Board Measurements

Tamb.= +25°C, Vd = +4V, Id = 120mA

[S] parameters & Noise Figure





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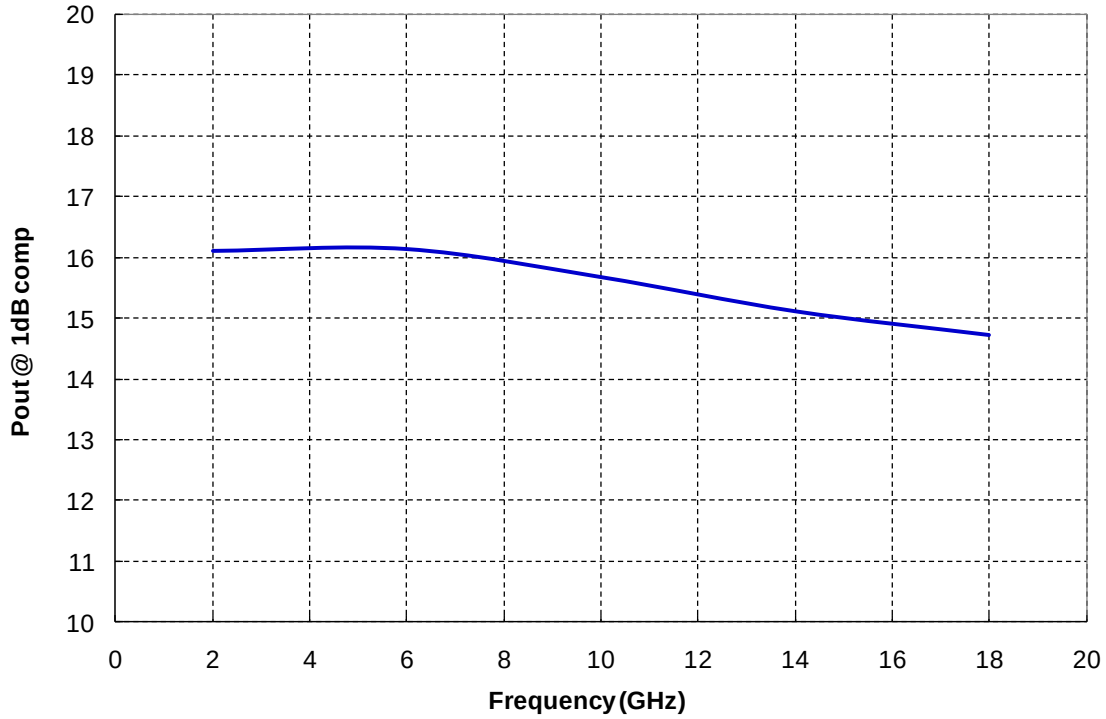
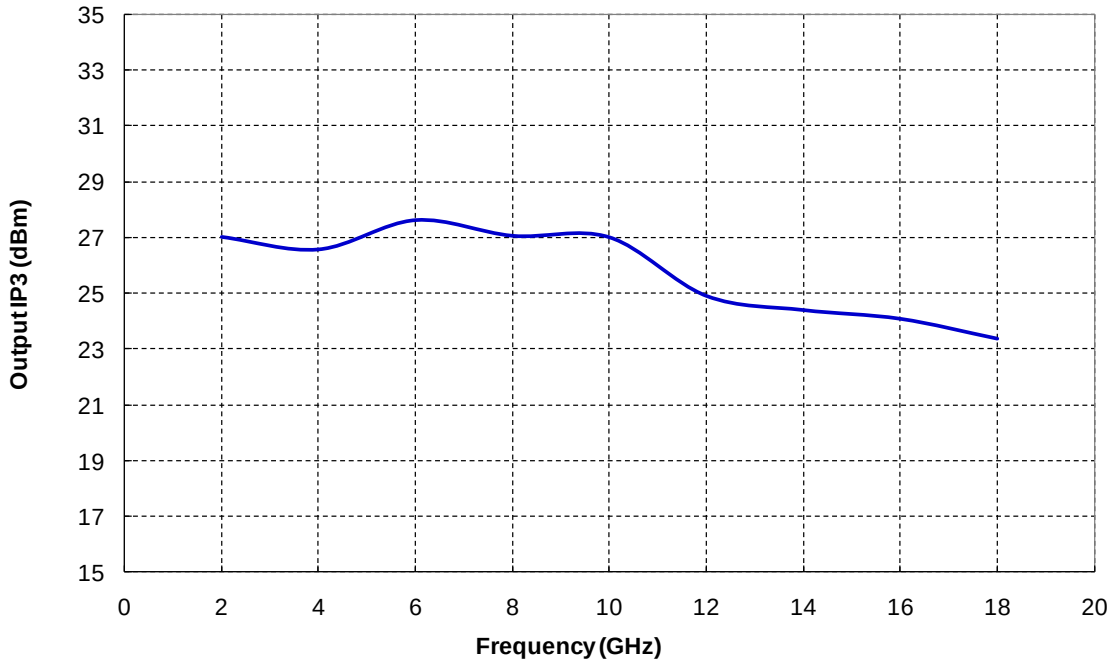
Typical Board Measurements

Tamb.= +25°C, Vd = +4V, Id = 120mA

Output Power @ 1dBcomp versus Frequency



Output Power IP3 versus Frequency



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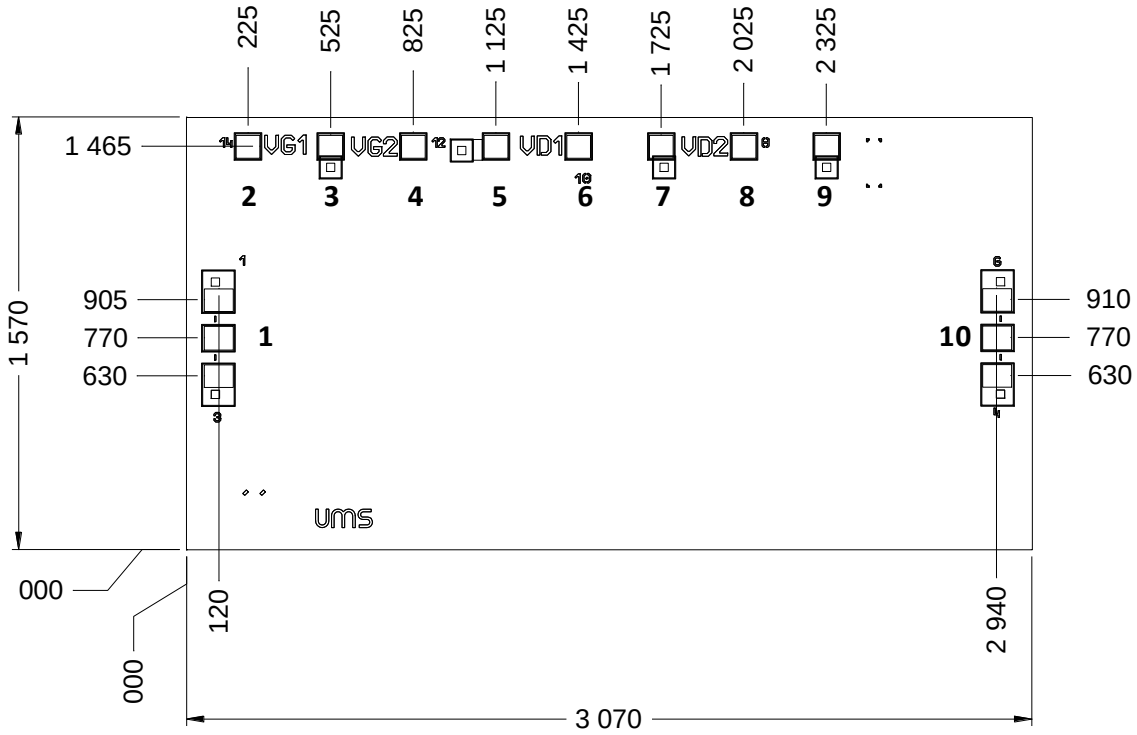
Mechanical data



Chip thickness: 100µm.
Chip size: 3070x1570 ±35µm
All dimensions are in micrometers

RF pads (1, 10) = 100 x 122µm²
DC pads (2, 4, 6, 8) = 100 x 100µm²

Pin number	Pin name	Description
1	IN	Input RF
2, 4,	VG1, VG2	Gate supply voltage
6, 8	VD1, VD2	Drain supply voltage
3, 5, 7, 9	GND	Ground (no bonding required)
10	OUT	Output RF

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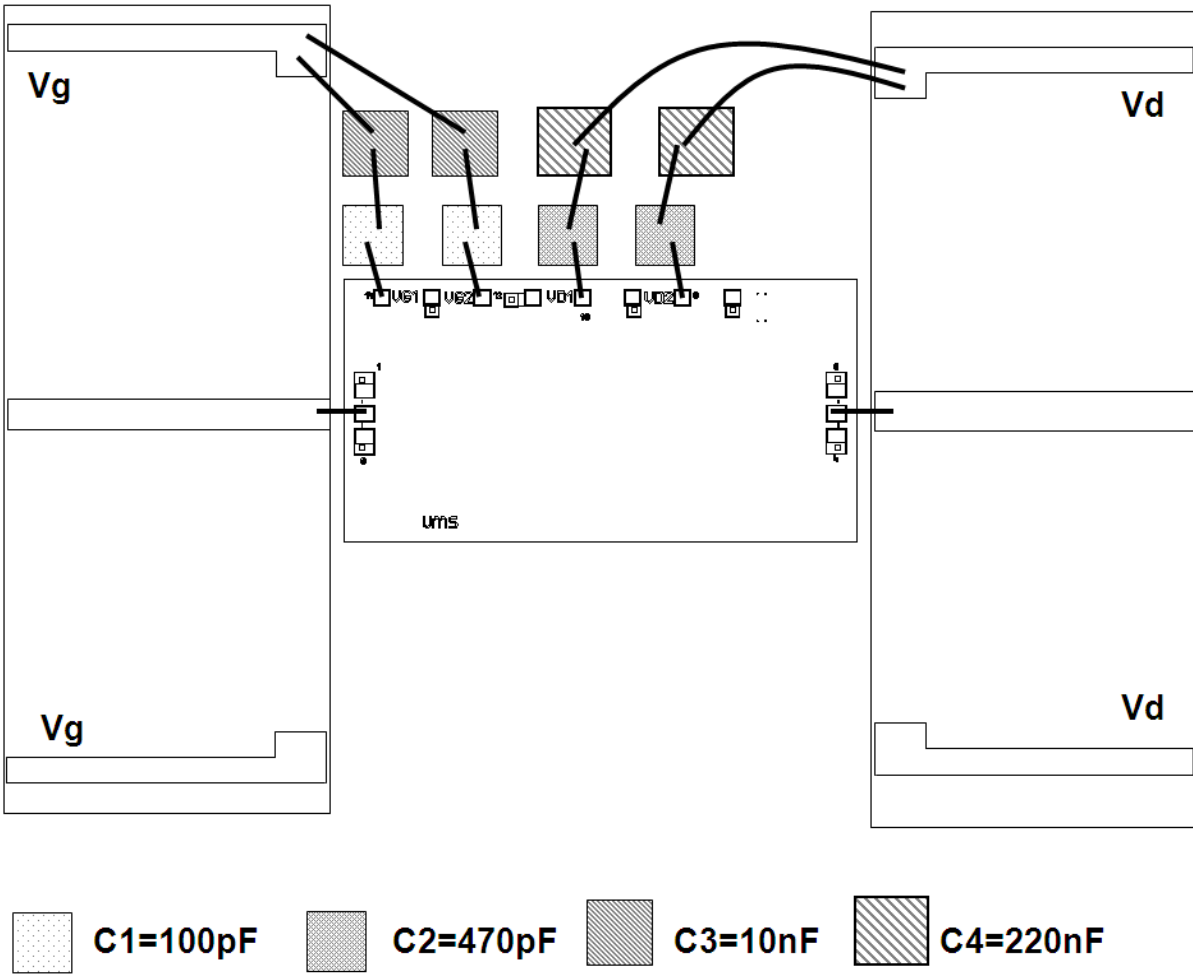
Recommended assembly plan



25µm wedge bonding is preferred

Recommended circuit bonding table

Label	Type	Decoupling	Comment
VD1, VD2	Vd	470pF & 220nF	Drain supply voltage
VG1, VG2	Vg	100pF & 10nF	Gate supply voltage

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Recommended ESD management

Refer to the application note AN0020 available at https://www.ums-rf.com for ESD sensitivity and handling recommendations for the UMS products.

Ordering Information

Chip form:	CHA3218-99F/00

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