

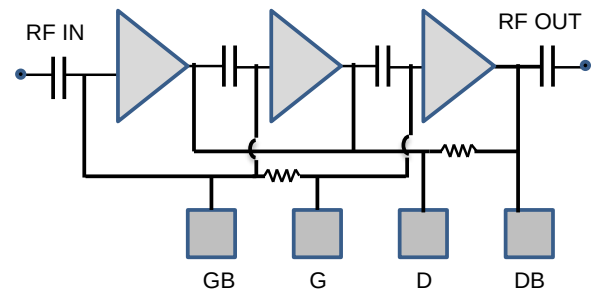
26-40 GHz Low Noise Amplifier GaAs Monolithic Microwave IC

Description

The CHA2362-99F is a wide band Low Noise Monolithic Amplifier which integrates three amplification stages that produces 22dB gain associated to 2dB Noise Figure.

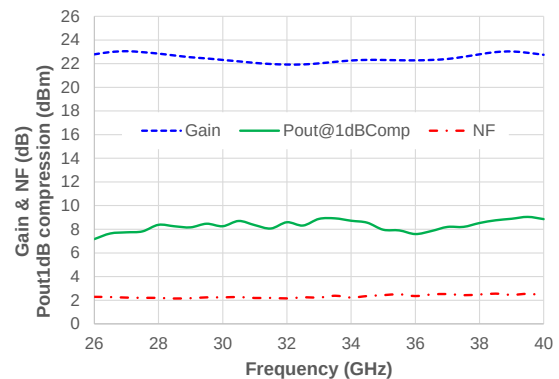
It is designed for a wide range of applications, from military to commercial communication systems. The circuit is manufactured with a pHEMT process.

It is available in chip form.



Main Features

- Frequency : 26-40 GHz
- 22dB linear gain
- 2dB Noise Figure
- 8dBm output power at 1dB gain compression
- 20dBm OIP3
- DC bias: Vd=4 V / Idq= 65 mA
- Chip size : 3x1.68x0.07 mm



Typical Gain, NF, P1dB with Vd=4V, Idq=65mA

Main Electrical Characteristics

T_{backside} = 25°C, Vd = 4.0V

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	26		40	GHz
Gain	Linear Gain		22		dB
NF	Noise Figure		2		dB
Pout	Output Power @1dB comp.		8		dBm

Specifications

$T_{\text{backside}} = 25^{\circ}\text{C}$, $V_d = 4.0\text{V}$; GB set in order to get $I_{dQ} = 65\text{mA}$

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	26		40	GHz
Gain	Linear Gain		22		dB
NF	Noise Figure		2		dB
S11	Input Return loss		15		dB
S22	Output Return loss		13		dB
P1dB	Output power at 1dB gain compression		8		dBm
OIP3	Output power at 3rd order intercept point		20		dBm
Vd	Drain supply voltage		4		V
Id	Drain supply current		65		mA
Vg	Gate supply voltage		-1		V
Ig	Gate supply current		1.3		mA

These values are representative of onboard measurements as defined on the drawing in paragraph "Evaluation board".

Absolute Maximum Ratings ⁽¹⁾ $T_{\text{backside}} = 25^{\circ}\text{C}$

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	6	V
Id	Maximum drain current	115	mA
Vg	Gate bias voltage	-3.5 to +0.15	V
Pin	Maximum peak input power	+15	dBm
Tj	Maximum junction temperature	175	°C

⁽¹⁾ Operation of this device above anyone of these parameters may cause permanent damage.

Recommended Operating Range

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	3 to 4	V
Idq	Quiescent current	50 to 70	mA
Vg	Gate bias voltage	-3.0 to +0.10	V
Pin	Maximum peak input power	+6	dBm
Tj	Maximum junction temperature	175	°C

Temperature Range

T _{backside}	Operating temperature range	-40 to +95	°C
Tstg	Storage temperature range	-55 to +150	°C

Typical Bias ConditionsT_{backside} = 25°C

Symbol	Pad N°	Parameter	Values	Unit
D & DB	7,8	DC drain voltage	4.0	V
GB	10	DC gate voltage	-1	V

“Power ON” sequence

1. Bias LNA gate voltage at Vg close to Vpinch-off (Typically: Vg ≈ -3.0V)
2. Apply Vd bias voltage (Typically: Vd = 4.0V)
3. Increase gate voltage Vg up to quiescent bias drain current Idq
4. Apply RF signal

“Power OFF” sequence

1. Turn off RF signal
2. Bias LNA gate voltage at Vg close to Vpinch-off (Typically: Vg ≈ -3.0V)
3. Check that quiescent bias drain current Idq is close to 0mA
4. Turn Vd bias voltage to 0V
5. Check that quiescent bias drain current Idq is close to 0mA
6. Turn Vg bias voltage to 0V

Typical on-wafer Sij parametersT_{backside} = 25°C, V_d = 4.0V, I_{dq} = 65mA

Freq (GHz)	S11 (dB)	PhS11 (°)	S12 (dB)	PhS12 (°)	S21 (dB)	PhS21 (°)	S22 (dB)	PhS22 (°)
0.50	-0.27	-18.21	-79.13	37.46	-41.59	-146.41	-0.74	-32.15
2.00	-0.99	-66.56	-95.05	-70.89	-39.27	57.84	-1.52	-107.05
3.00	-1.51	-92.01	-72.44	-46.53	-42.60	38.08	-2.47	-143.25
8.00	-2.31	-167.37	-76.88	-160.56	-41.61	4.96	-12.61	147.36
9.00	-2.28	-178.13	-81.46	-120.67	-34.30	1.29	-13.20	154.62
10.00	-2.27	171.38	-73.67	-166.25	-29.11	-13.67	-12.98	155.41
11.00	-2.28	160.78	-69.91	160.92	-25.00	-26.21	-12.98	152.92
12.00	-2.37	150.20	-65.68	151.74	-20.85	-35.98	-13.22	149.59
13.00	-2.41	138.43	-65.49	115.65	-16.45	-47.01	-12.94	144.60
14.00	-2.52	125.99	-64.51	84.00	-11.70	-61.10	-12.87	136.77
15.00	-2.67	112.54	-63.02	78.62	-6.86	-79.63	-13.07	126.04
16.00	-3.07	98.16	-66.60	67.89	-2.31	-102.48	-13.41	113.86
17.00	-3.71	83.13	-72.67	105.54	1.87	-129.23	-14.03	99.41
18.00	-4.44	67.41	-67.72	155.42	5.41	-157.95	-15.03	80.11
19.00	-5.25	50.94	-60.10	133.34	8.56	172.98	-16.06	55.35
20.00	-6.10	31.95	-56.53	112.82	11.51	143.67	-16.94	24.10
21.00	-6.93	10.11	-53.14	85.35	14.29	113.60	-17.08	-13.33
22.00	-7.68	-14.41	-50.66	70.96	16.89	82.02	-16.08	-50.29
23.00	-8.57	-43.78	-48.88	44.11	19.24	48.42	-15.26	-82.36
24.00	-9.40	-77.72	-47.37	18.87	21.17	12.77	-15.06	-109.91
25.00	-10.13	-114.49	-46.32	-7.76	22.54	-23.93	-15.73	-130.41
26.00	-10.94	-150.06	-46.51	-41.85	23.31	-60.23	-17.10	-137.26
27.00	-11.70	174.07	-46.44	-68.32	23.61	-94.84	-17.34	-136.58
27.50	-11.90	157.53	-47.02	-74.64	23.63	-111.18	-16.67	-139.01
28.00	-12.29	143.24	-46.81	-94.89	23.60	-126.77	-15.84	-140.43
29.00	-12.82	114.49	-47.89	-120.05	23.51	-156.51	-14.52	-152.66
30.00	-13.59	86.30	-49.08	-143.53	23.32	175.20	-14.16	-167.21
31.00	-14.17	58.25	-49.21	-169.71	23.19	148.18	-14.40	172.80
32.00	-14.26	34.04	-49.00	167.42	23.03	122.29	-14.94	151.31
33.00	-14.47	11.70	-49.44	145.78	22.95	96.72	-16.39	122.12
34.00	-14.75	-4.69	-48.69	121.31	22.88	71.51	-17.25	88.12
35.00	-15.07	-19.98	-48.81	104.17	22.84	46.29	-16.51	49.21
36.00	-15.14	-32.58	-49.05	90.88	22.78	21.34	-14.78	15.33
37.00	-15.42	-39.74	-48.44	75.84	22.77	-3.87	-13.00	-12.54
38.00	-16.27	-44.09	-47.10	55.03	22.86	-29.24	-11.67	-35.00
39.00	-16.12	-44.55	-46.45	39.31	22.88	-56.30	-10.84	-53.79
40.00	-15.95	-40.00	-46.47	19.63	23.02	-84.39	-10.83	-68.08
41.00	-14.33	-33.13	-47.15	1.80	23.17	-116.09	-12.16	-73.39
42.00	-11.91	-29.04	-46.61	-24.80	22.89	-154.02	-13.01	-49.86

Device thermal performances

All the figures given in this section are obtained assuming that the die is only cooled down by conduction through the chip backside.

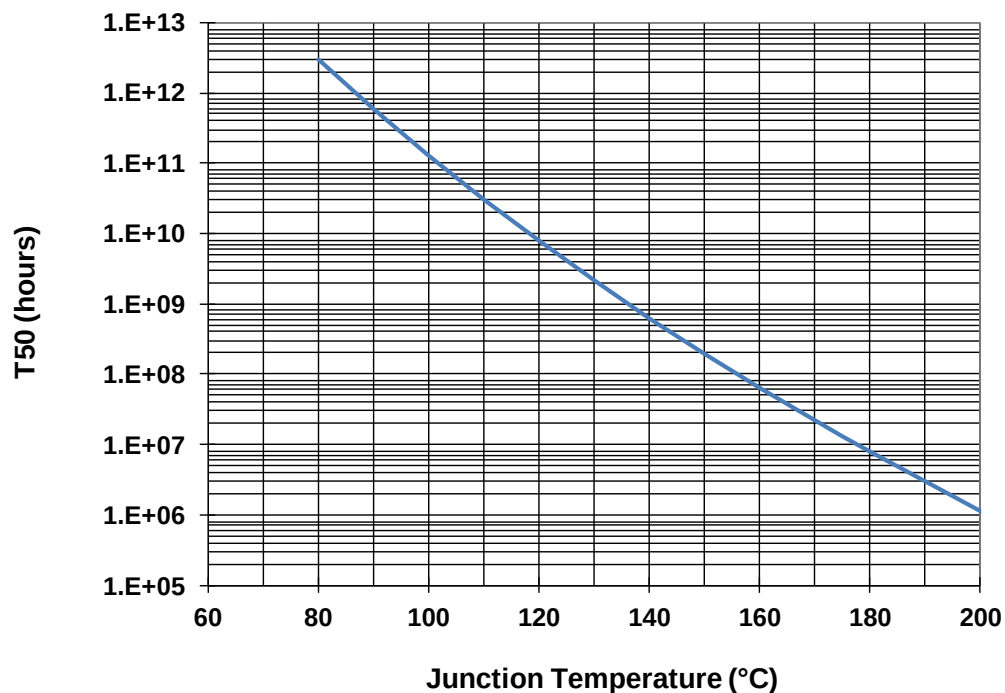
The temperature is monitored at the chip back-side interface (T_{backside}).

For nominal operating, the system maximum temperature must be adjusted in order to guarantee that T_{junction} remains below the maximum value specified in the Recommended Operating Ratings table.

So, the system PCB must be designed to comply with this requirement.

Parameter	Biasing conditions	T_{junction} (°C)	R_{TH} (°C/W)	T_{50} (hours)
$R_{\text{th}}^{(1)}$ Thermal Resistance	$V_d = 4\text{V}$ $I_{dQ} = 65\text{mA}$ Dissipated power = 0.26W	125	153.2	$4.1\text{E}10^9$

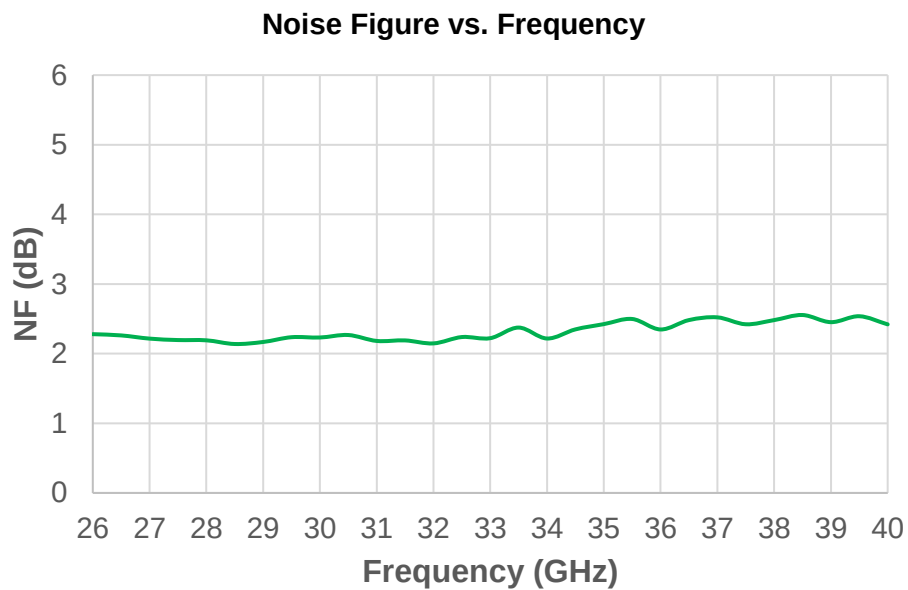
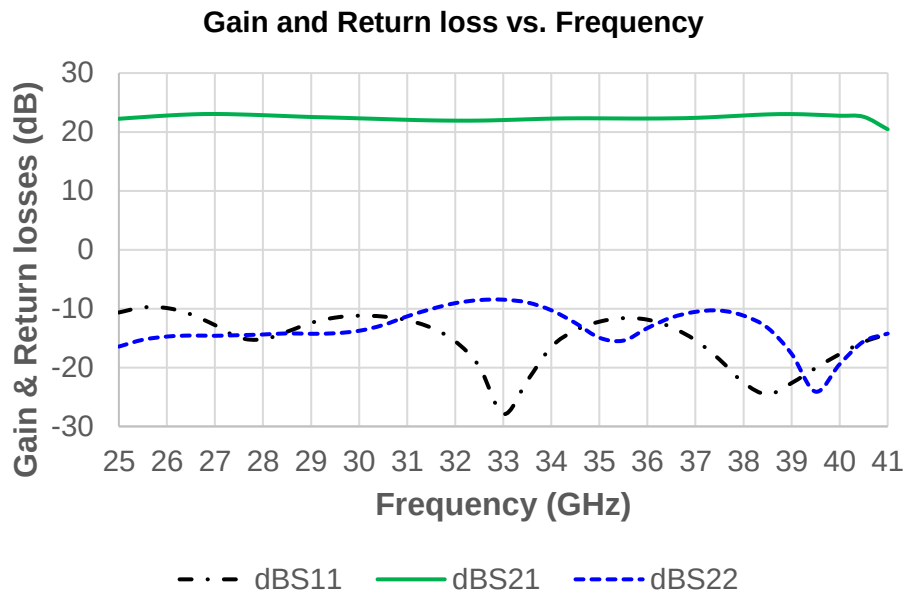
¹ Assuming 85°C T_{backside}



Typical Board Measurements

$T_{\text{backside}} = 25^{\circ}\text{C}$, $V_d = 4\text{V}$, $I_{dq} = 65\text{mA}$

The following values are representative of on board measurements, on die access reference planes.

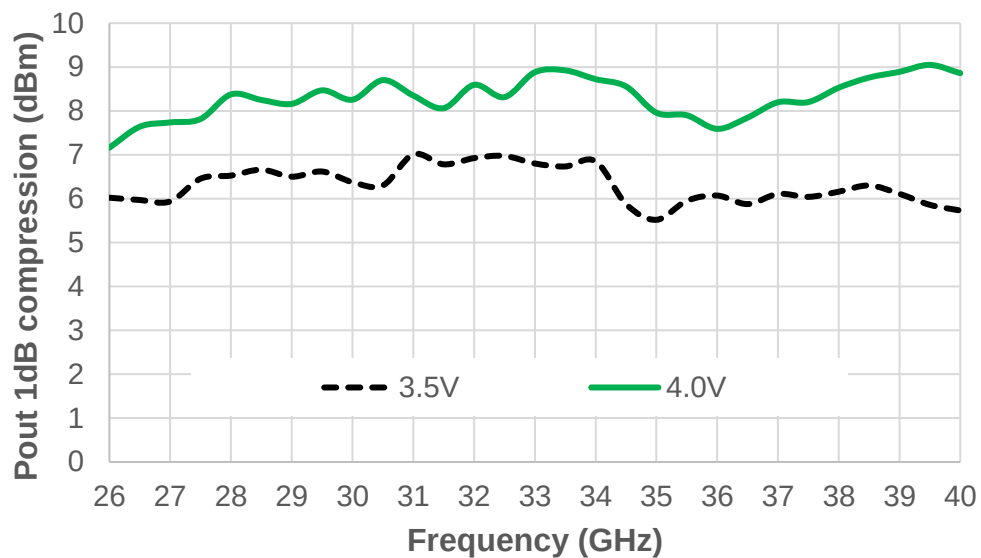


Typical Board Measurements

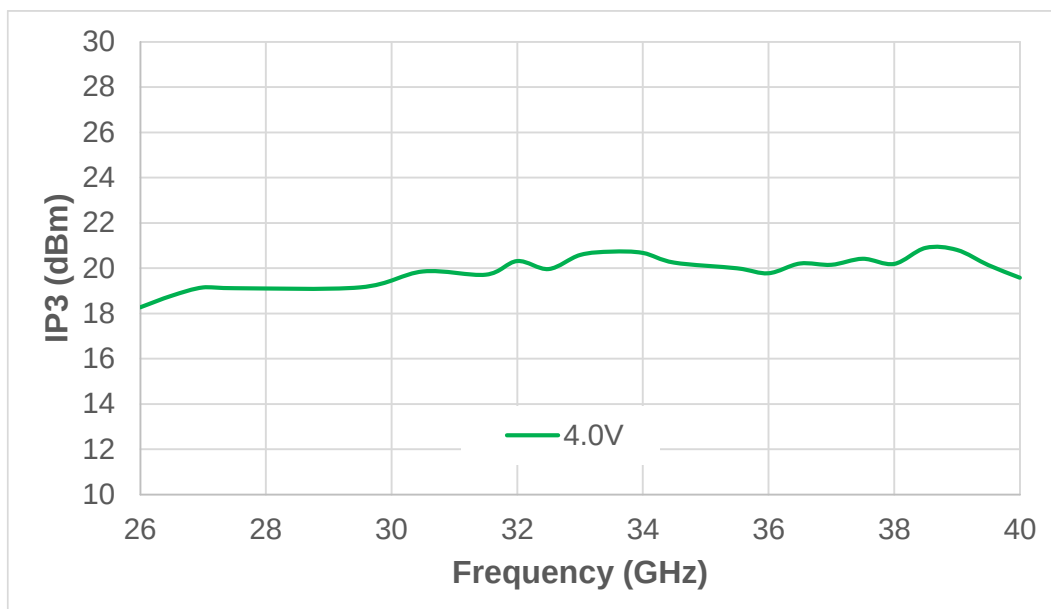
$T_{\text{backside}} = 25^{\circ}\text{C}$, $V_d = 3.5\text{V}$ & 4.0V , $I_{dQ} = 65\text{mA}$

The following values are representative of on board measurements, on die access reference planes.

Output power at 1 dB gain compression vs. Frequency



Output IP3 vs. Frequency

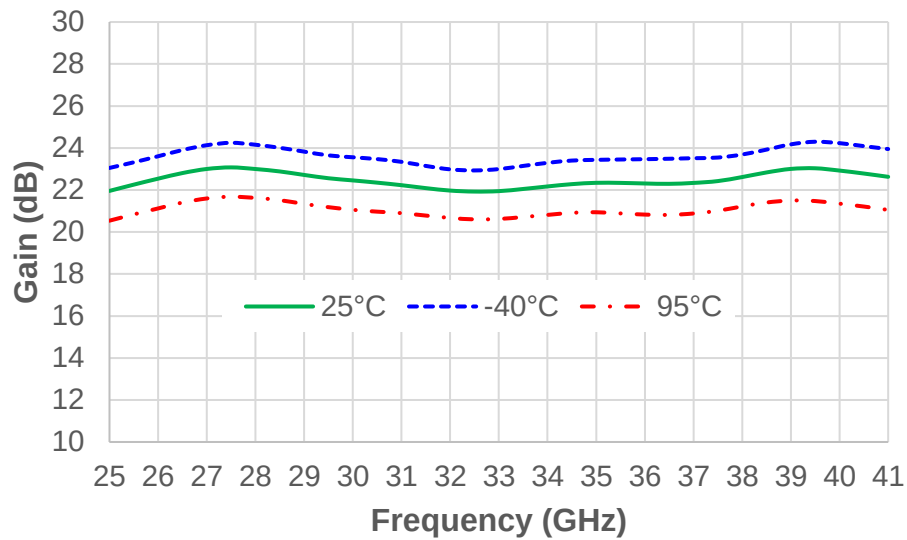


Typical Board Measurements

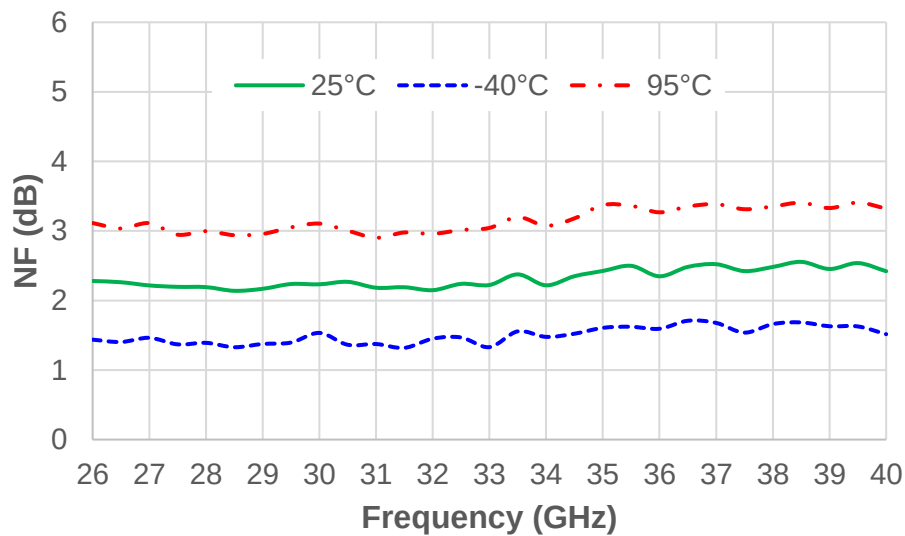
$T_{\text{backside}} = 25^{\circ}\text{C}$, $V_d = 4.0\text{V}$, $I_{dq} = 65\text{mA}$

The following values are representative of on board measurements, on die access reference planes.

Linear Gain vs. Temperature



Noise Figure vs. Temperature

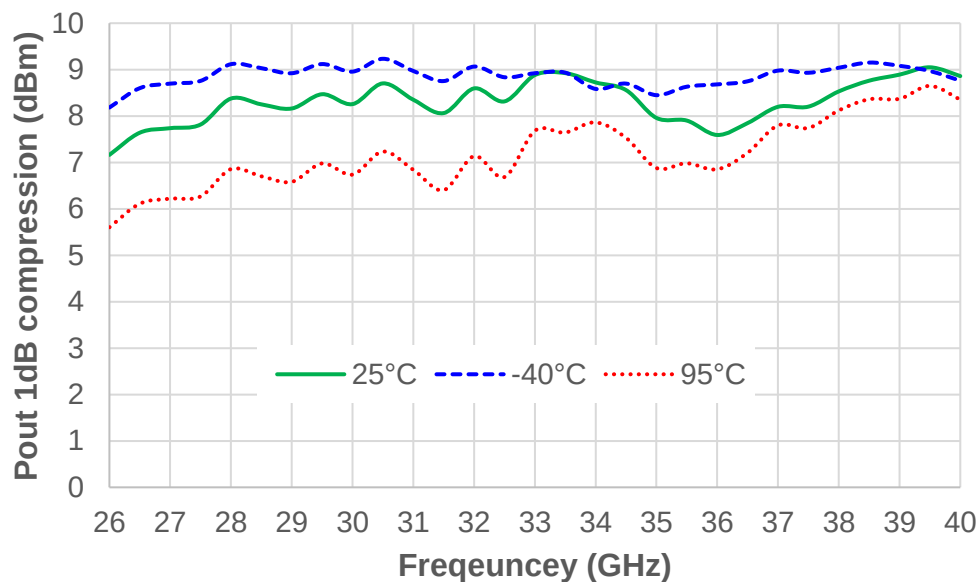


Typical Board Measurements

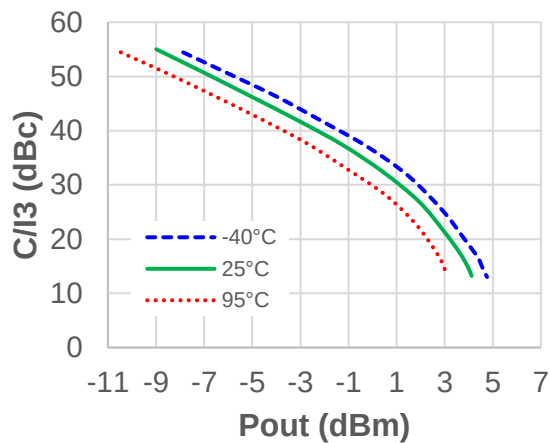
$T_{\text{backside}} = 25^{\circ}\text{C} / -40^{\circ}\text{C} / 95^{\circ}\text{C}$, $V_d = 4.0\text{V}$, $I_{dq} = 65\text{mA}$

The following values are representative of on board measurements, on die access reference planes.

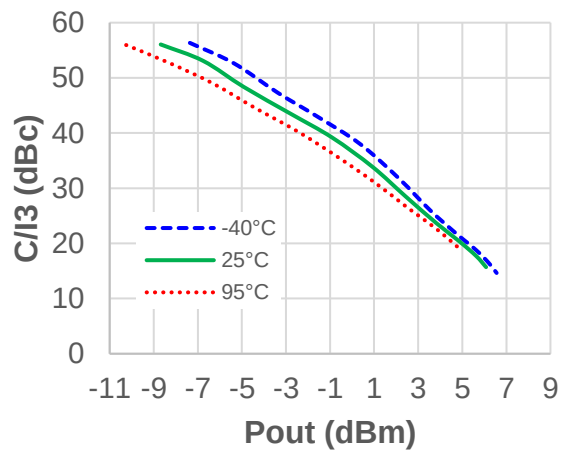
Output power at 1dB compression vs. Temperature



Output C/I3 at 26GHz versus temperature at 65mA



Output C/I3 at 40GHz versus temperature at 65mA

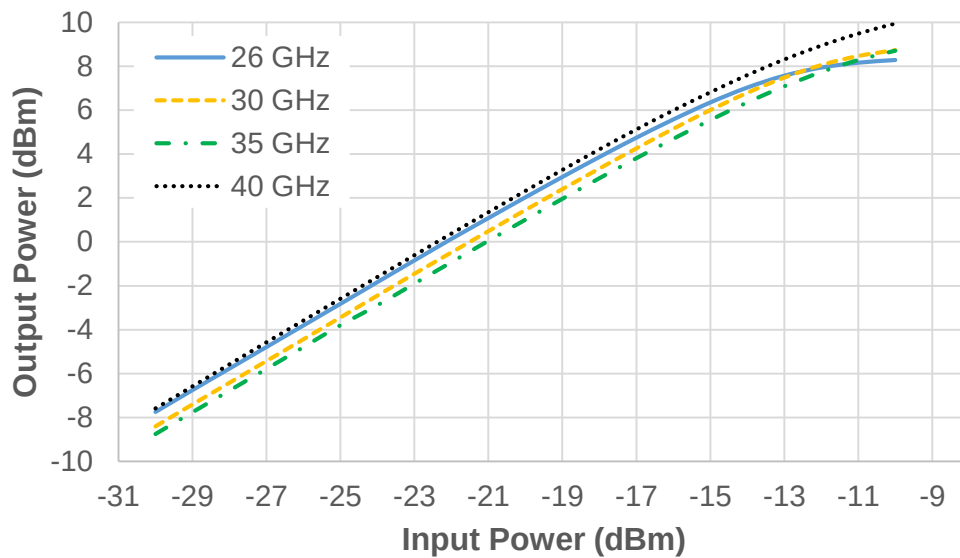


Typical Board Measurements

$T_{\text{backside}} = 25^{\circ}\text{C}$, $V_d = 4.0\text{V}$, $I_{dq} = 65\text{mA}$

The following values are representative of on board measurements, on die access reference planes.

Output power vs. Input power

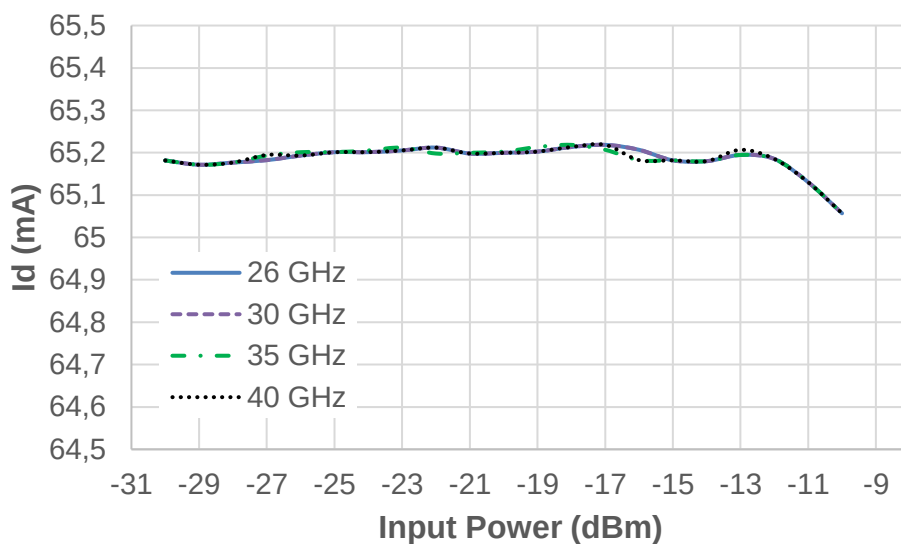


Typical Board Measurements

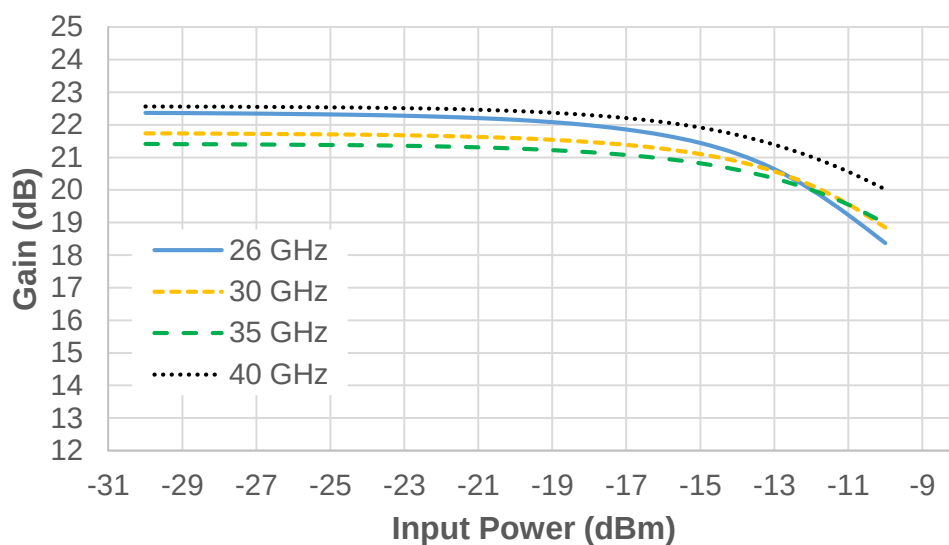
$T_{\text{backside}} = 25^{\circ}\text{C}$, $V_d = 4.0\text{V}$, $I_{Dq} = 65\text{mA}$

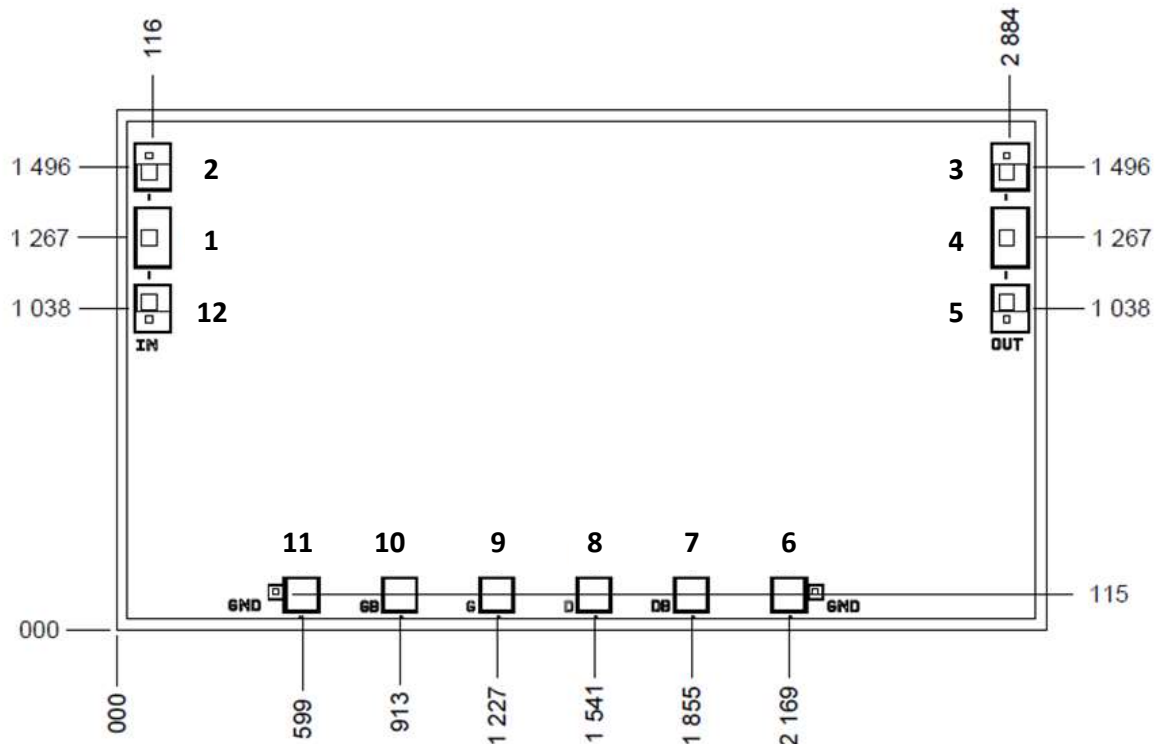
The following values are representative of on board measurements, on die access reference planes.

I_d vs. Input power



Gain vs. Input power



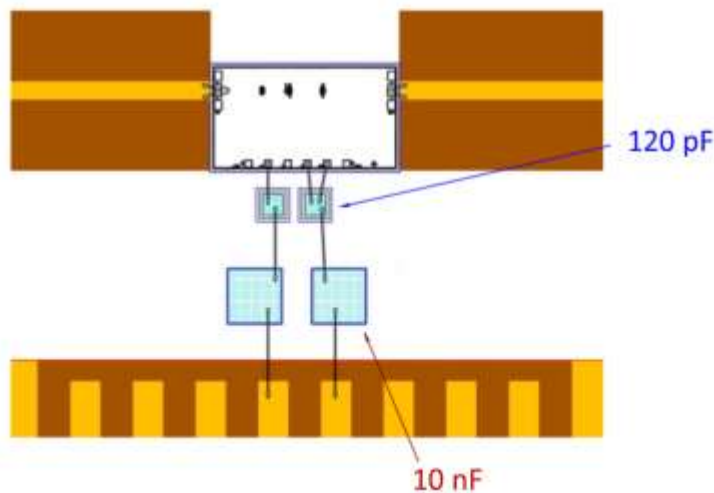
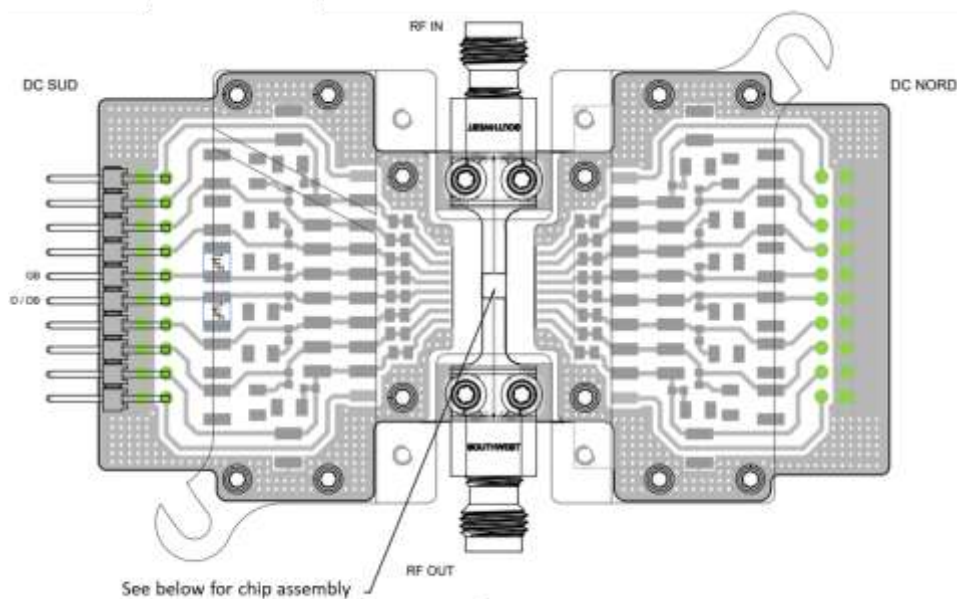
Mechanical dataChip thickness: 70 μm Chip size: 3000/1680 $\pm 35\mu\text{m}$

All dimensions are in micrometers

RF Pads (1,2) = 192 x 114 μm DC Pads = 106 x 106 μm

PAD Number	Name	Description
1	RF IN	Input RF port
4	RF OUT	Output RF port
2,3,5,6,11,12	GND	Ground
10	GB	DC Gate voltage
7,8	DB, D	DC Drain voltage
9	G	Not Connected

Evaluation board



Total of 3 levels of decoupling capacitor have been used, 2 levels on the tab and 1 level on the board. The first level is composed of 120 pF chip capacitors, the second level is composed of 10nF chip capacitors, the third level is composed of 1 μ F. The first two levels should be as close as possible to the die.

Note



Recommended reflow process assembly

Refer to the application note AN0001 available at <https://www.ums-rf.com> for die attach.

Recommended ESD management

Refer to the application note AN0020 available at <https://www.ums-rf.com> for ESD sensitivity and handling recommendations.

Recommended Evaluation board assembly

Refer to the application note AN0030 available at <https://www.ums-rf.com> Evaluation board.

Ordering Information

Die form	CHA2362-99F/00
Evaluation board	EVB-CHA2362-99F

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