United Monolithic Semiconductors

CHA2362-98F

26-40GHz Low Noise Amplifier

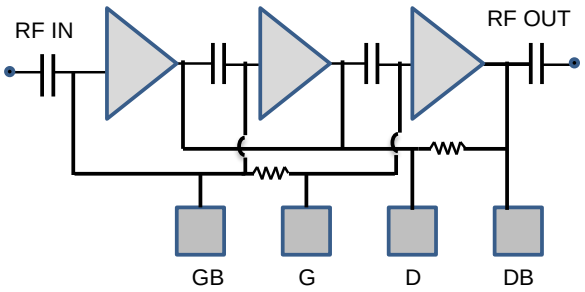
GaAs Monolithic Microwave IC

Description

The CHA2362-98F is a wide band Low Noise Monolithic Amplifier which integrates three amplification stages that produces 22dB gain associated to 2dB Noise Figure.

It is designed for a wide range of applications, from military to commercial communication systems. The circuit is manufactured with a pHEMT process with a me protection.

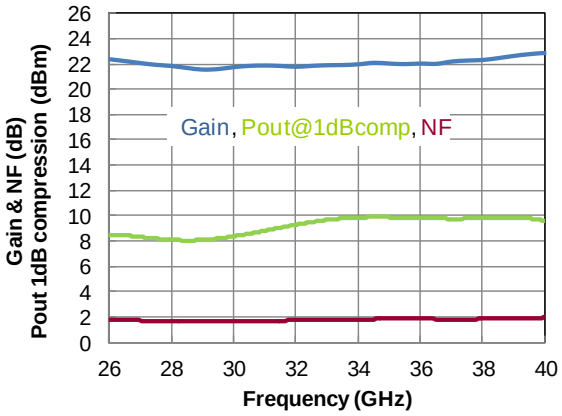
It is available in chip form.



Main Features

- Frequency : 26-40 GHz
- 22dB Linear Gain
- 2dB Noise Figure
- 9dBm output power at 1dB gain compression
- 21dBm OIP3
- DC bias: Vd=4 Volt@ Idq= 65 mA
- Chip size 3x1.68x0.07mm

Typical Gain, NF, P1dB with Vd=4V, Idq=65mA



Main Electrical Characteristics

$T_{backside}$= 25°C, Vd = 4.0V

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	26		40	GHz
Gain	Linear Gain		22		dB
NF	Noise Figure		2		dB
Pout	Output Power @1dB comp.		9		dBm

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Electrical Characteristics

$T_{backside}$ = 25°C, Vd = +4V; GB set in order to get Idq = 65mA

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	26		40	GHz
Gain	Linear Gain		22		dB
ripple	Ripple pic/pic in the frequency range		1.4		dB
NF	Noise Figure		2		dB
S11	Input Return loss		13		dB
S22	Output Return loss		13		dB
P1dB	Output power at 1dB gain compression		9		dBm
OIP3	Output power at3rd order intercept point		21		dBm
Vd	Drain supply voltage		4		V
Idq	Quiescent current		65		mA
Vg	Gate supply voltage		-1		V
Ig	Gate supply current		1.3		mA

These values are representative of onboard measurements as defined on the drawing in paragraph "Evaluation board".

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Absolute Maximum Ratings (1)

$T_{backside}$= 25°C

Symbol	Parameter	Max rating	Unit
Vd	Drain bias voltage	6	V
Id	Drain bias current	115	mA
Vg	Gate bias voltage	-3.5 to +0.15	V
Pin	Maximum peak input power overdrive	+15	dBm
Tj	Junction temperature	175	°C
Tstg	Storage temperature range	-55 to +150	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.

Recommended Operating Range

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	3 to 4	V
Idq	Quiescent current	50 to 70	mA
Vg	Gate bias voltage	-3.0 to +0.10	V
Pin	Maximum peak input power	+6	dBm
Tj	Maximum junction temperature	175	°C

Temperature Range

Ta	Operating temperature range	-40 to +95	°C
Tstg	Storage temperature range	-55 to +150	°C

Typical Bias Conditions

$T_{backside}$ = 25°C

Symbol	Pad Nº	Parameter	Values	Unit
D & DB	V1	DC drain voltage	4	V
GB	V2	DC gate voltage	-1	V

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Temperature Range

$T_{backside}$	Operating temperature range	-40 to +95	°C
Tstg	Storage temperature range	-55 to +150	°C

Typical Bias Conditions

$T_{backside}$= 25°C

Symbol	Pad Nº	Parameter	Values	Unit
D & DB	7,8	DC drain voltage	4	V
GB	10	DC gate voltage	-1	V

"Power ON" sequence

1. Bias LNA gate voltage at Vg close to Vpinch-off (Typically: Vg ≈ -3.0V)
2. Apply Vd bias voltage (Typically: Vd = 4.0V)
3. Increase gate voltage Vg up to quiescent bias drain current Idq = 65 mA
4. Apply RF signal

"Power OFF" sequence

1. Turn off RF signal
2. Bias LNA gate voltage at Vg close to Vpinch-off (Typically: Vg ≈ -3.0V)
3. Check that quiescent bias drain current Idq is close to 0mA
4. Turn Vd bias voltage to 0V
5. Check that quiescent bias drain current Idq is close to 0mA
6. Turn Vg bias voltage to 0V

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Typical on-wafer Sij parameters

$T_{backside}$ = 25°C, Vd = +4.0V, Idq = 65mA

Freq (GHz)	S11 (dB)	PhS11 (°)	S12 (dB)	PhS12 (°)	S21 (dB)	PhS21 (°)	S22 (dB)	PhS22 (°)
0.50	-0.25	-18.95	-60.88	-47.06	-30.86	-150.56	-0.78	-32.67
2.00	-0.90	-68.60	-60.89	57.43	-38.24	52.12	-1.41	-108.11
3.00	-1.39	-94.03	-70.94	-66.56	-43.60	34.29	-2.30	-143.49
8.00	-2.18	-167.89	-63.13	162.14	-40.42	2.32	-11.73	152.33
9.00	-2.22	-178.56	-62.47	-131.95	-33.98	-1.81	-12.13	157.50
10.00	-2.16	171.29	-64.49	-53.74	-28.79	-16.80	-11.92	157.15
11.00	-2.20	161.50	-64.91	116.50	-24.65	-30.93	-11.83	154.94
12.00	-2.32	150.74	-59.38	103.18	-20.42	-41.87	-12.11	150.19
13.00	-2.30	139.35	-59.01	174.78	-15.90	-53.78	-11.91	145.07
14.00	-2.46	127.43	-61.77	-133.31	-11.09	-69.05	-11.88	137.00
15.00	-2.62	114.23	-62.97	157.18	-6.32	-89.15	-12.25	125.75
16.00	-3.06	99.57	-79.62	39.67	-1.96	-112.67	-12.68	113.95
17.00	-3.69	84.55	-65.89	-56.73	2.13	-139.67	-13.54	98.88
18.00	-4.45	68.11	-59.31	85.52	5.68	-168.20	-14.81	78.65
19.00	-5.16	50.56	-61.46	120.60	8.92	162.64	-16.19	53.56
20.00	-6.28	30.05	-58.09	105.87	11.97	132.59	-17.75	18.90
21.00	-6.96	5.50	-48.08	96.41	14.91	101.35	-17.94	-26.31
22.00	-8.26	-21.12	-50.55	61.00	17.40	68.15	-16.91	-65.54
23.00	-8.80	-55.89	-45.80	39.45	19.75	32.90	-15.87	-98.20
24.00	-9.56	-90.88	-53.03	-46.26	21.48	-4.14	-15.50	-124.12
25.00	-10.22	-128.34	-48.73	-15.16	22.59	-41.67	-16.50	-138.11
26.00	-10.56	-159.44	-42.19	-52.34	23.19	-77.72	-17.49	-143.57
27.00	-11.56	165.50	-47.73	-71.09	23.41	-111.53	-15.78	-143.84
27.50	-12.11	152.98	-47.28	-102.79	23.44	-127.59	-15.28	-148.10
28.00	-11.47	140.12	-48.01	-115.54	23.42	-143.24	-15.02	-151.28
29.00	-13.51	112.84	-52.40	-93.72	23.33	-173.54	-14.03	-167.17
30.00	-13.50	83.25	-54.55	-108.05	23.10	158.11	-14.04	173.87
31.00	-15.42	59.26	-51.76	156.73	22.95	130.67	-14.56	153.41
32.00	-16.08	33.99	-50.69	159.52	22.85	104.27	-15.43	129.73
33.00	-16.58	11.85	-46.23	111.96	22.73	77.91	-16.15	98.60
34.00	-16.40	-2.00	-46.40	130.47	22.67	52.51	-16.98	60.99
35.00	-17.29	-22.26	-46.02	123.80	22.61	26.45	-15.77	21.56
36.00	-17.01	-31.66	-46.33	69.90	22.57	0.65	-14.42	-3.17
37.00	-17.91	-34.37	-49.77	17.23	22.64	-25.75	-13.04	-29.22
38.00	-18.01	-40.52	-45.07	54.96	22.75	-52.57	-11.88	-45.11
39.00	-15.90	-33.11	-47.67	16.24	22.80	-82.04	-12.60	-56.70
40.00	-15.08	-28.84	-47.46	-8.27	22.90	-115.34	-12.81	-52.83
41.00	-12.31	-36.07	-48.50	-22.07	22.23	-155.67	-9.69	-31.33
42.00	-11.07	-40.01	-46.36	-106.34	19.26	159.20	-4.76	-41.41

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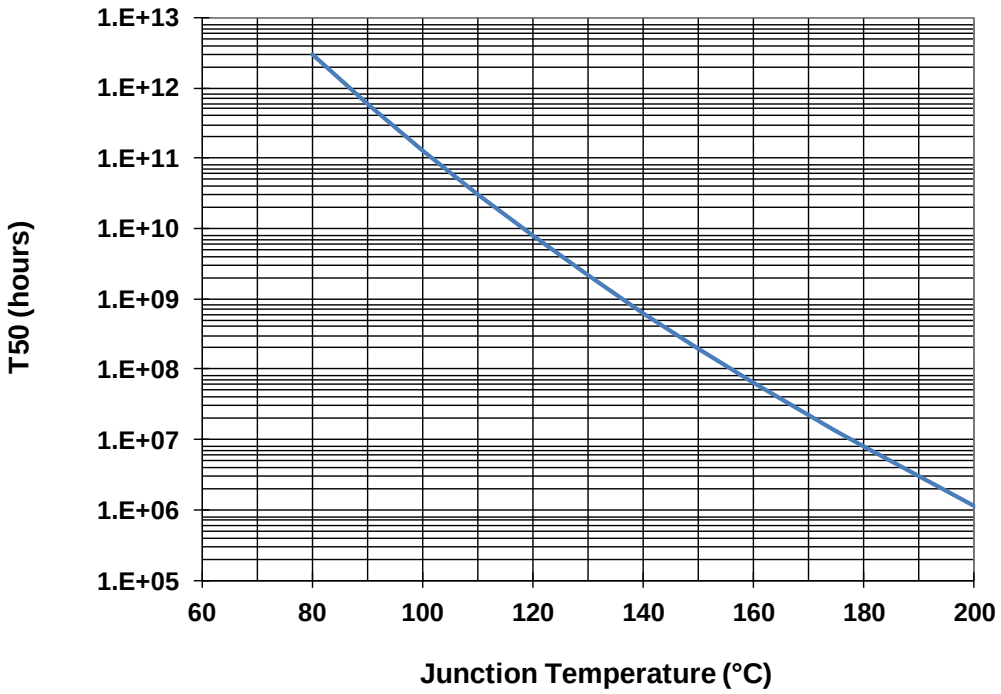
Device thermal performance

All the figures given in this section are obtained assuming that the die is only cooled down by conduction through the chip backside.
The temperature is monitored at the chip back-side interface ($T_{backside}$).
For nominal operating, the system maximum temperature must be adjusted in order to guarantee that Tjunction remains below the maximum value specified in the Recommended Operating Ratings table.
So, the system PCB must be designed to comply with this requirement.

Parameter	Biasing conditions	Tjunction (°C)	R_{TH} (°C/W)	T50 (hours)
R_{TH} (1) Thermal Resistance (Junction to Case)	Vd= 4V Id= 65mA Dissipated power = 0.26W	125	153.2	$4.1E10^{9}$

(1) Assuming 85°C $T_{backside}$



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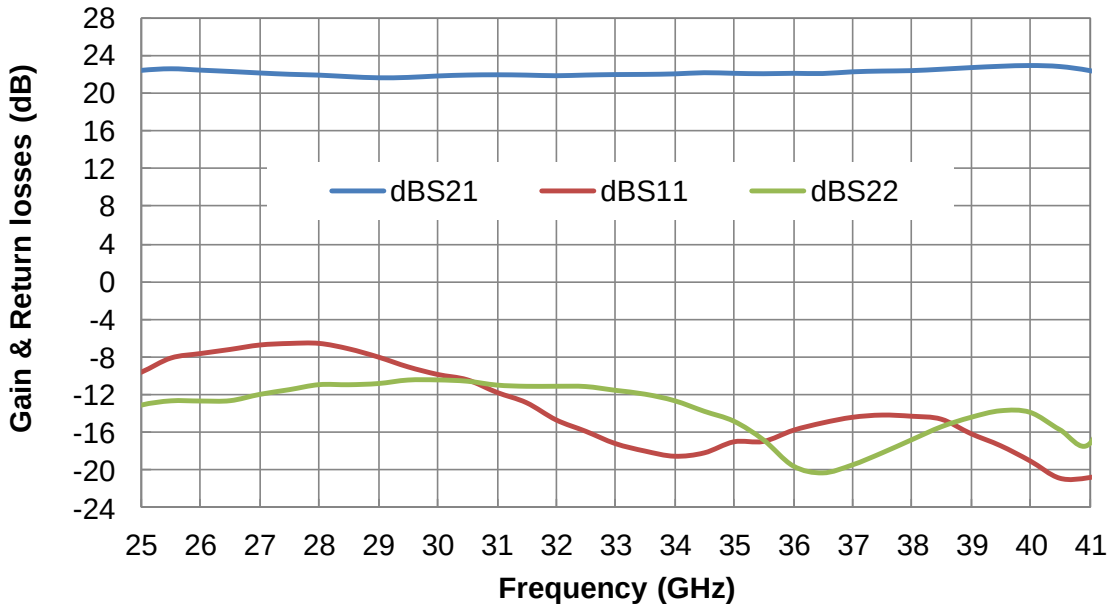
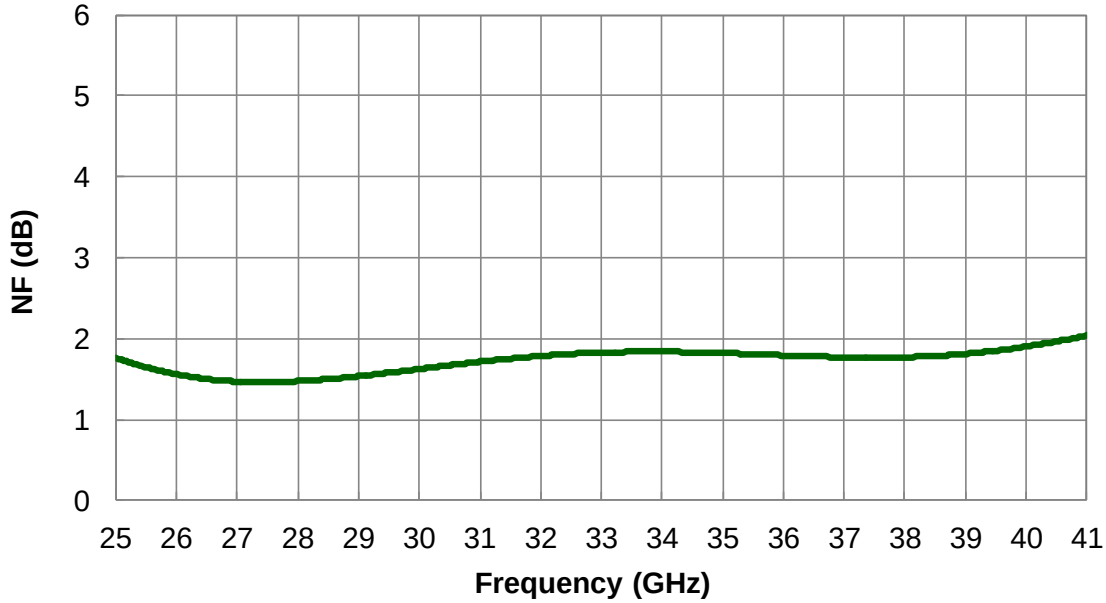
Typical Board Measurements

$T_{backside}$ = 25°C, Vd = 4V, Idq = 65mA
The following values are representative of on board measurements, on die access reference planes.

Gain and Return losses vs. Frequency



Noise Figure vs. Frequency



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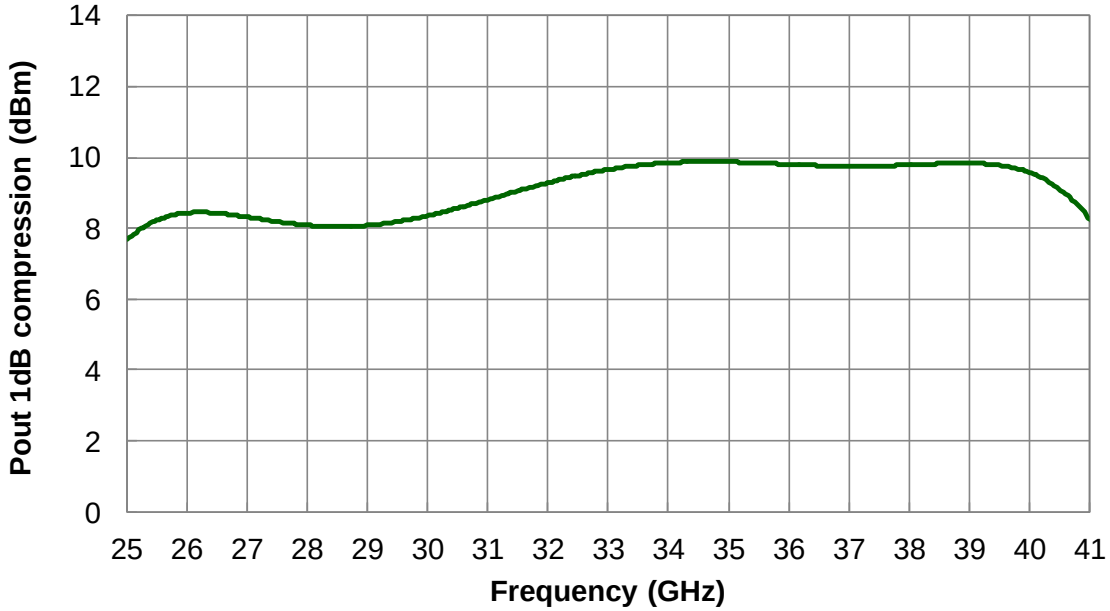
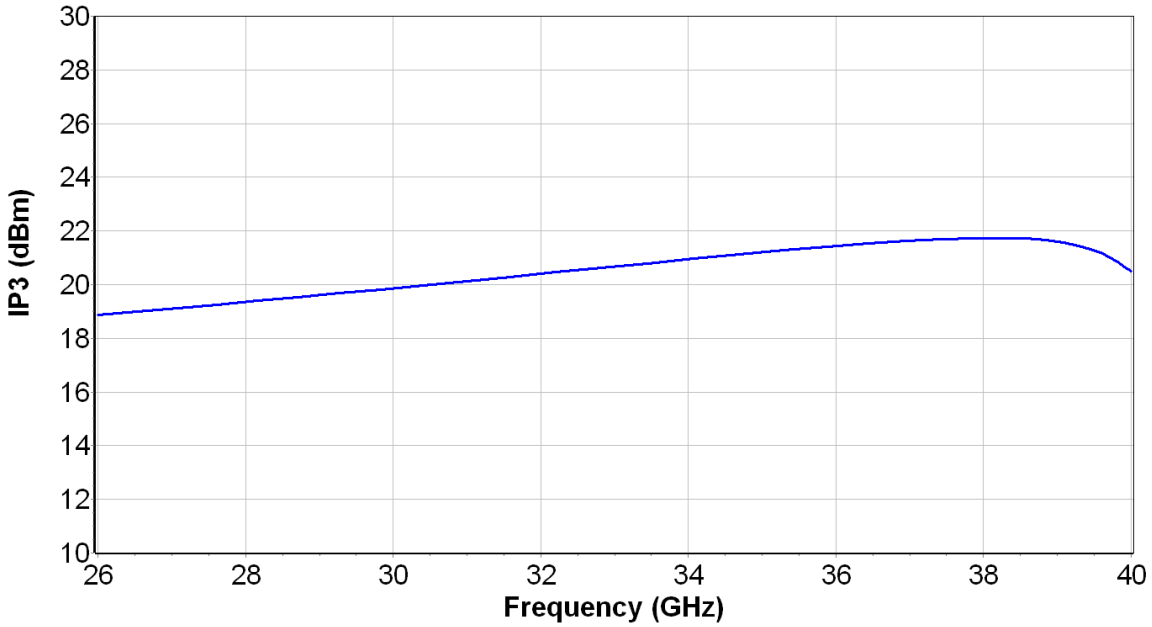
Typical Board Measurements at ambient temperature

$T_{backside}$ = 25°C, Vd = 4V, Idq = 65mA
The following values are representative of on board measurements, on die access reference planes.

Output power at 1 dB gain compression vs. Freqeuncy



Output IP3 vs. Frequency



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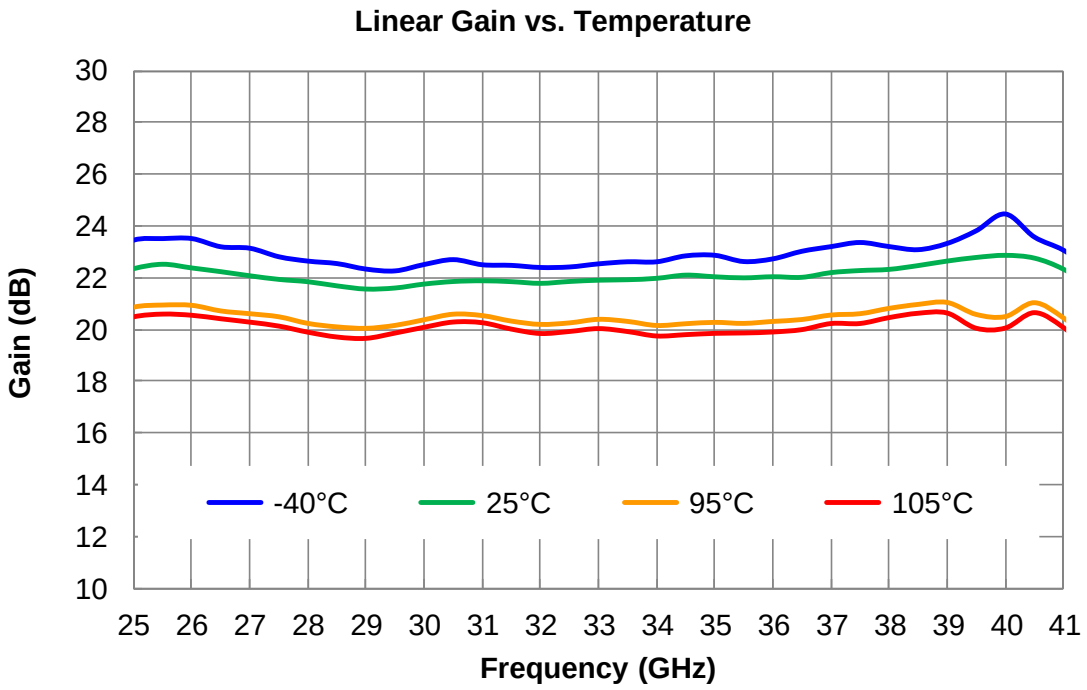
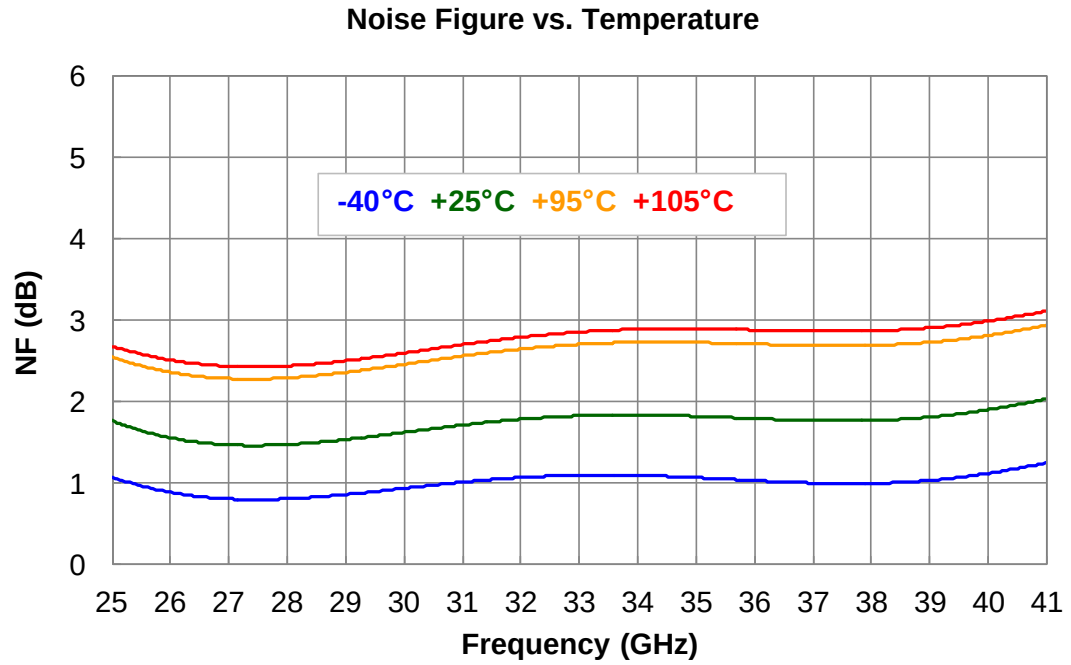
Typical Board Measurements

$T_{backside}$ = 25°C, Vd = 4V, Idq = 65mA
The following values are representative of on board measurements, on die access reference planes.





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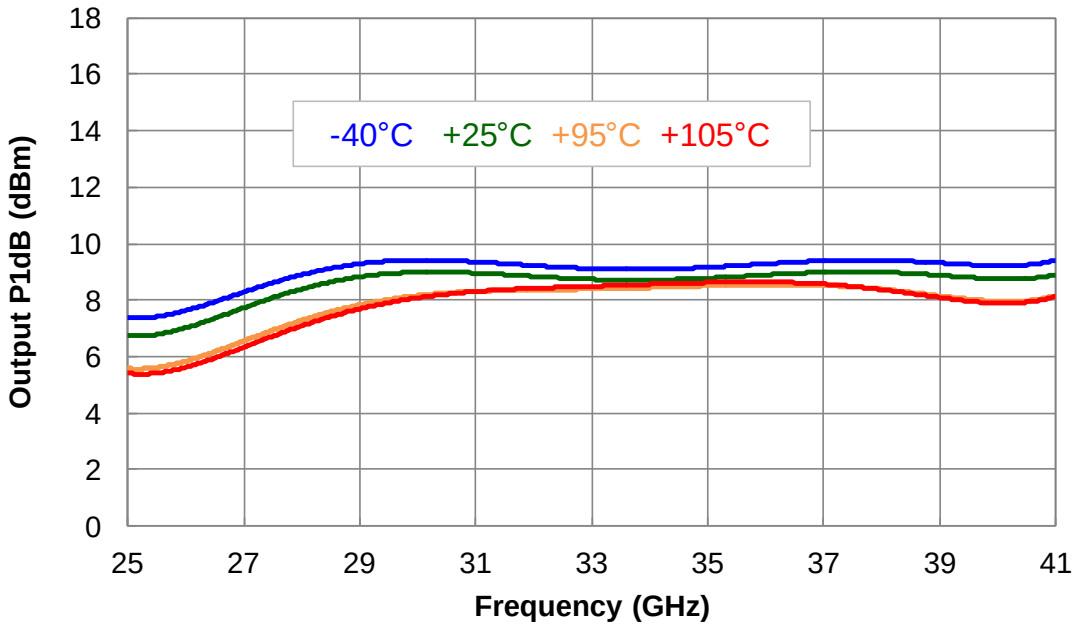
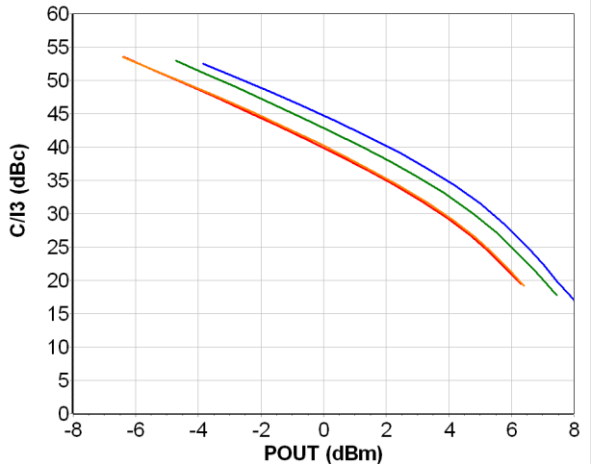
Typical Board Measurements versus temperature

$T_{backside}$ = 25°C / -40°C / 95°C / 105°C, Vd = 4.0V, Idq = 65mA
The following values are representative of on board measurements, on die access reference planes.

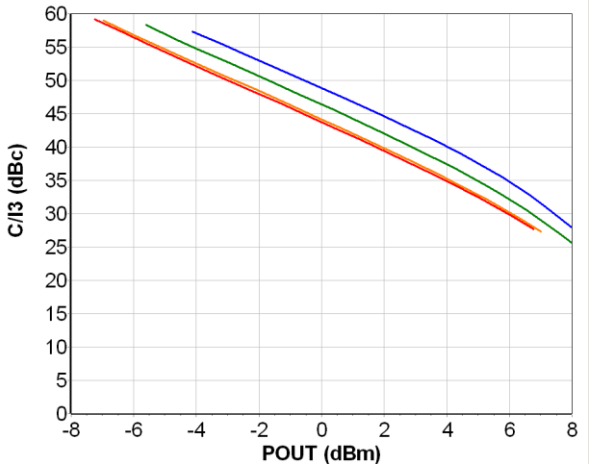
Output power at 1dB compression vs. Temperature



Output C/I3 at 26GHz vs. Temperature at 65mA



Output C/I3 at 40GHz vs. Temperature at 65mA



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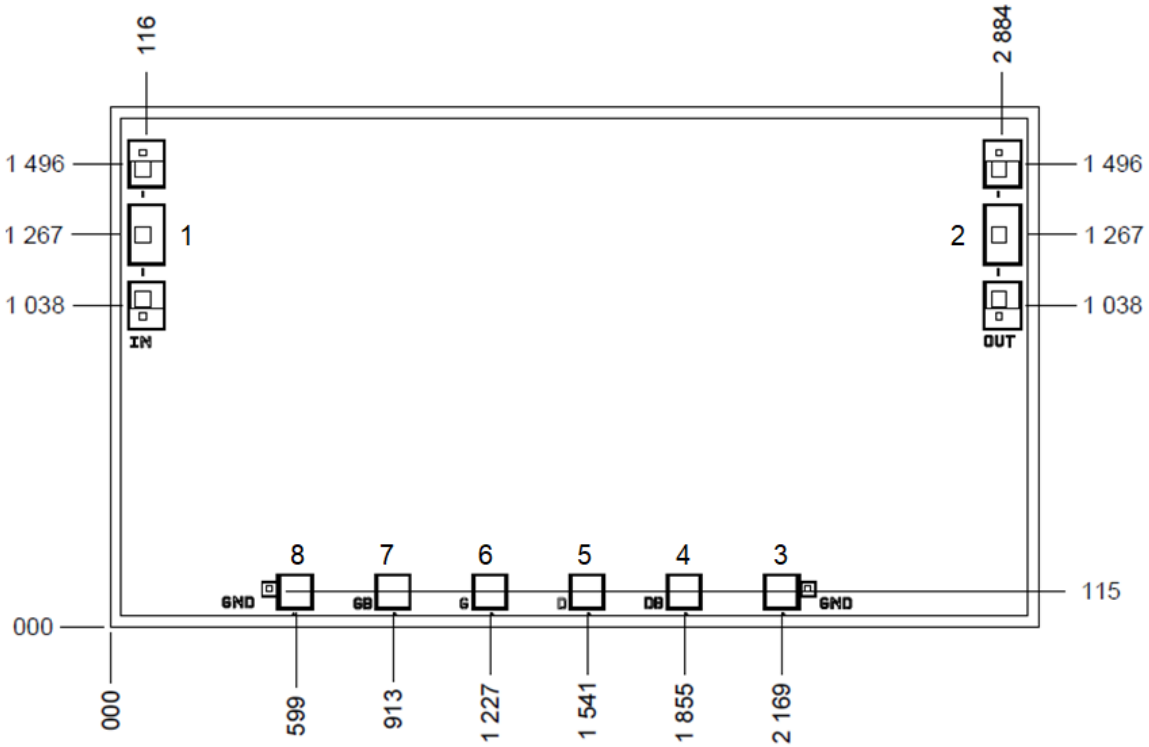
Mechanical data



Chip thickness: 70µm.
Chip size:3000/1680 ±35µm
All dimensions are in micrometers

RF Pads (1,2) = 186 x 105 (BCB opening)
DC Pads = 100 x 100 (BCB opening)

PAD Number	Name	Description
1	RF IN	Input RF port
2	RF OUT	Output RF port
3, 8	GND	ground
7	GB	DC Gate voltage(1)
4, 5	DB, D	DC Drain voltage

(1) Pad number 6: G is not used

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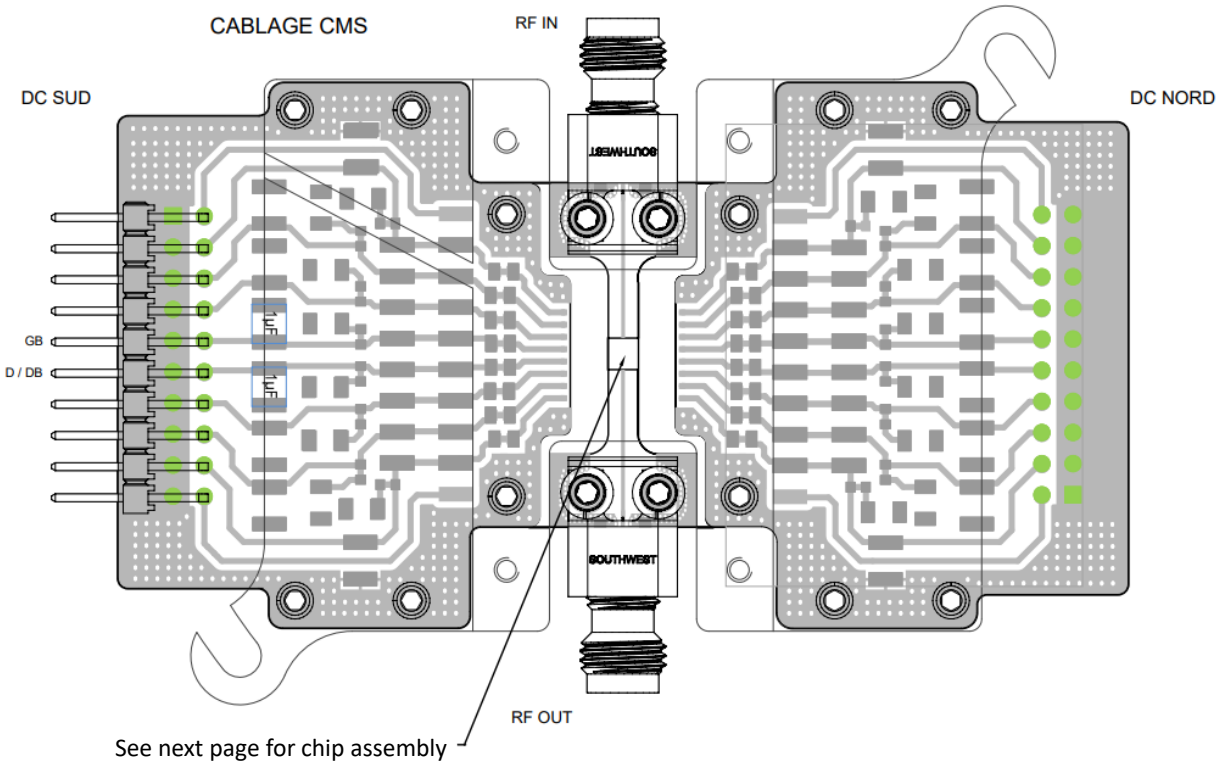
Evaluation board



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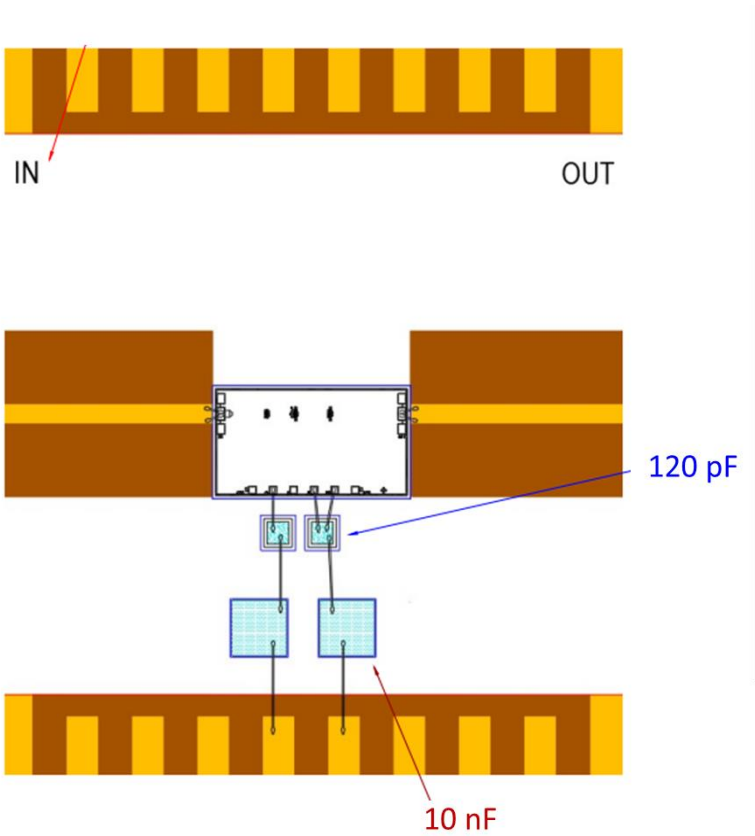
Chip Assembly



Total of 3 levels of decoupling capacitor have been used, 2 levels on the tab and 1 level on the board. The first level is composed of 120 pF chip capacitors, the second level is composed of 10nF chip capacitors, the third level is composed of 1µF. The first two levels should be as close as possible to the die.

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Recommended reflow process assembly

Refer to the application note AN0001 available at https://www.ums-rf.com for die attach.

Recommended ESD management

Refer to the application note AN0020 available at https://www.ums-rf.com for ESD sensitivity and handling recommendations.

Recommended Evaluation board assembly

Refer to the application note AN0030 available at https://www.ums-rf.com Evaluation board.

Ordering Information

Die form	CHA2362-98F/00
Evaluation board	EVB-CHA2362-98F

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