46 - 52 GHz Low Noise Amplifier with Adjustable Gain Control

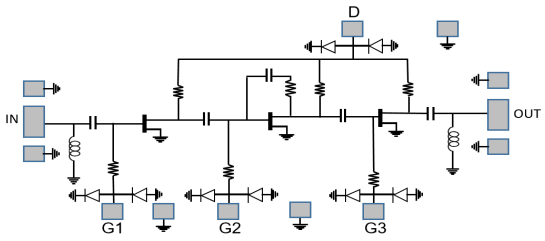
GaAs Monolithic Microwave IC

Description

The CHA2353-99F is a three stage monolithic Low Noise Amplifier, producing 24dB linear gain with 30dB Adjustable Gain Control (AGC) and 3.5dB Noise Figure in the frequency band 46-52GHz. It includes ESD protections on each RF access and DC pads.

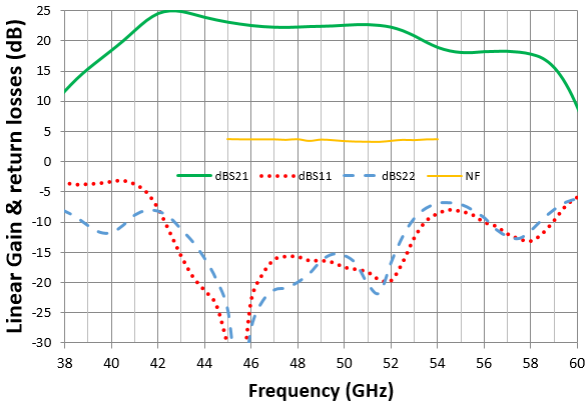
This amplifier is designed for a wide range of applications, from Commercial to Space communication systems.

It is manufactured with a GaAS pHEMT process successfully evaluated for Space and is available in bare die.



Main Features

- Frequency band: 46-52GHz
- 3.5dB Noise Figure
- 24dB small signal gain
- 30dB Adjustable Gain Control
- P_{1dB}: 9dBm
- P_{sat}: 11dBm
- OIP3: 20dBm
- Typical DC bias: Vd = 3.3V@Id = 55mA
- Chip size 1.97x1.17x0.07mm



Typical S parameters and Noise Figure

Main Electrical Characteristics

$T_{backside}$= +25°C, Vd = +3.3V , VG(G1=G2=G3) set in order to get Idq = 55mA (≈0V)
($T_{backside}$: Die backside temperature)

Symbol	Parameter	Min	Typ	Max	Unit
Frequency	Frequency range	46		52	GHz
Gain	Small signal Gain		24		dB
NF	Noise Figure		3.5		dB
Id	Drain bias current		55		mA

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Electrical Characteristics

$T_{backside}$= +25°C, Vd = +3.3V , VG (G1=G2=G3) set in order to get Idq = 55mA (≈0V)
($T_{backside}$: Die backside temperature)

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	46		52	GHz
Gain	Small Signal Gain		24		dB
NF	Noise Figure		3.5		dB
IRL	Input return loss		-13		dB
ORL	Output return loss		-15		dB
Gain ctrl	Gate control voltage to gain sensitivity		30		dB
IP-1dB	Input power at 1dB gain compression		-13		dBm
OP-1dB	Output power at 1dB gain compression		9		dBm
Vd	Drain bias voltage		3.3		V
Id	Drain bias current		55		mA

These values are representative of on-board measurements as defined on the drawing in paragraph "Evaluation board".

Absolute Maximum Ratings (1)

$T_{backside}$ = +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	4.2V	V
Vg	Gate bias voltage	-2 to +0.4	V
Pin	Maximum peak input power overdrive	-2	dBm
Tj	Junction temperature	175	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.

Recommended Operating Range (2), (3)

$T_{backside}$ = +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	3 to 4	V
Vg	Gate bias voltage	-0.5 to +0.1	V
Pin	Input power range	-20 to -5	dBm

(2) Electrical performances are defined for specified test conditions
(3) Electrical performances are not guaranteed over all recommended operating conditions

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Typical Bias Conditions

$T_{backside}$ = +25°C

Symbol	Parameter	Value	Unit
VG1, VG2, VG3	Gate bias voltage tuned for Id = 55mA	0	V
VD	Drain bias voltage	3.3	V

"Power ON" sequence

1. Ground the device
2. Set the gate voltage close to Vpinch-off (-1.5V)
3. Apply the drain voltage Vd (typically +3.3V)
4. Increase Vg up to quiescent bias drain current Id
5. Apply RF signal

"Power OFF" sequence

1. Turn off RF signal
2. Decrease the gate voltage to -1.5V
3. Decrease the drain voltage to 0V
4. Turn off Vd supply
5. Turn off Vg supply

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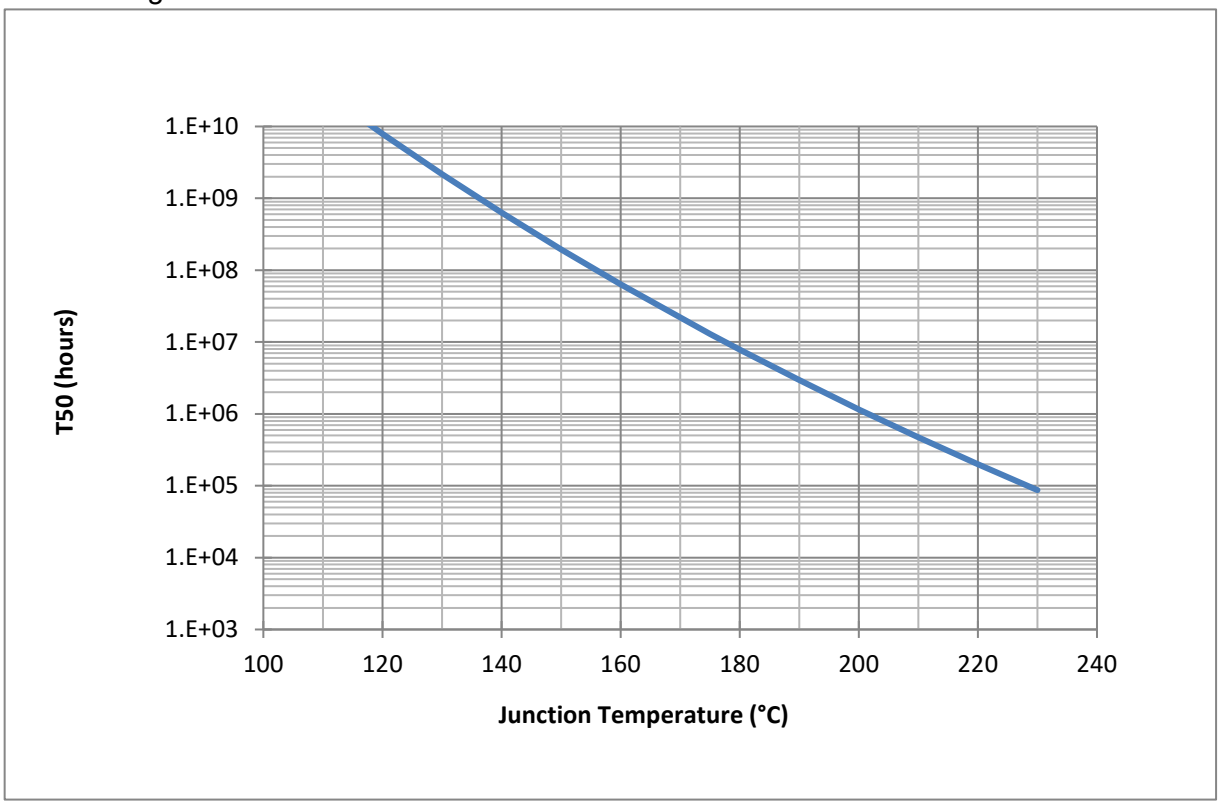
Device thermal performance

All figures given in this section are obtained assuming the chip backside is only cooled down by the conduction through the test board (no convection mode is considered).
The temperature is monitored at the chip backside ($T_{backside}$).
The system maximum temperature must be adjusted in order to guarantee that T_J remains below the maximum value specified in the Recommended Operating Range table.
The system PCB must be designed to comply with this requirement.

Parameter	Biasing conditions	Tjunction (°C)	RTH (°C/W)	T50 (hours)
R_{TH} (1) Thermal Resistance (Junction to Case)	Vd = 3.3V Id = 75mA P_{diss} = 0.25W	143	230	$4.4x10^8$
	Vd = 3.3V Id = 55mA P_{diss} = 0.18W	130	250	$2.2x10^9$

(1) Assuming 85° $T_{backside}$



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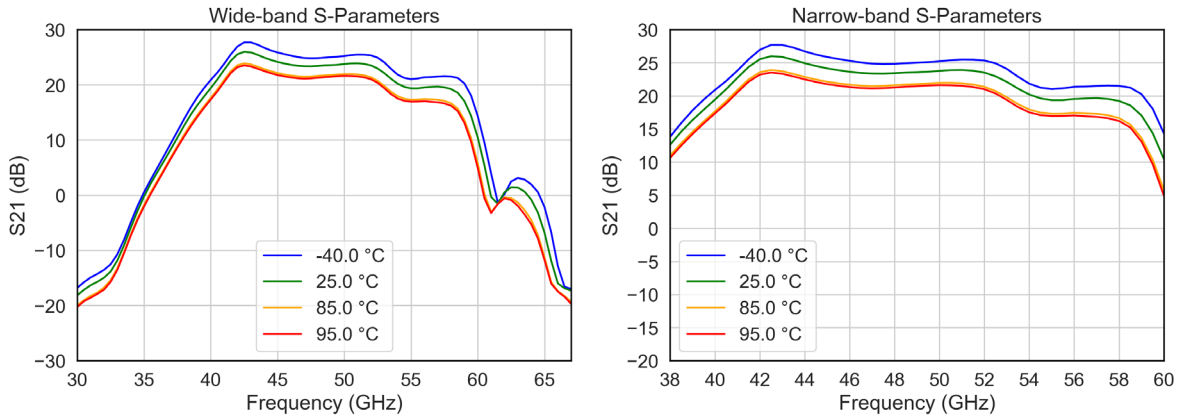
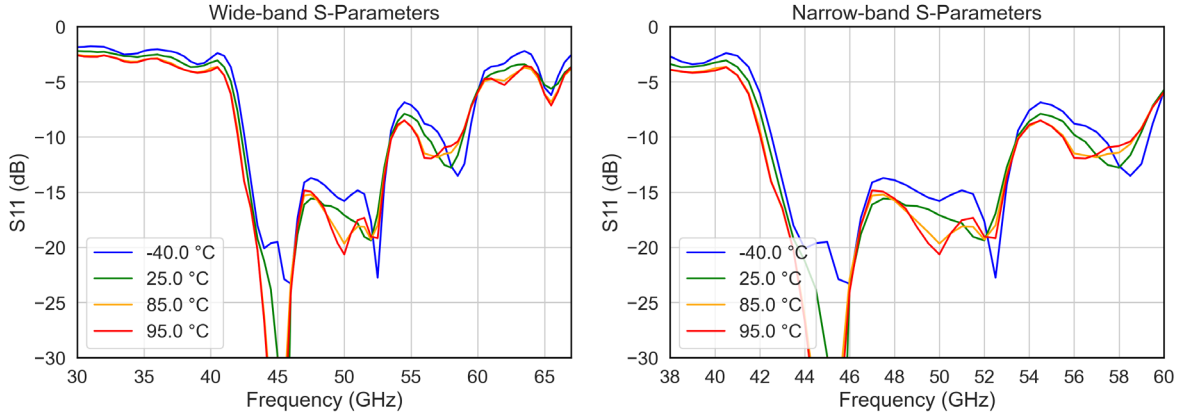
Typical on Board Measurements

Test conditions : $T_{backside}$ = -40°C/+25°C/85°C/95°C, Vd = 3.3V, Id = 55mA
Board losses are de-embedded. Measurements are given in the die access plans.

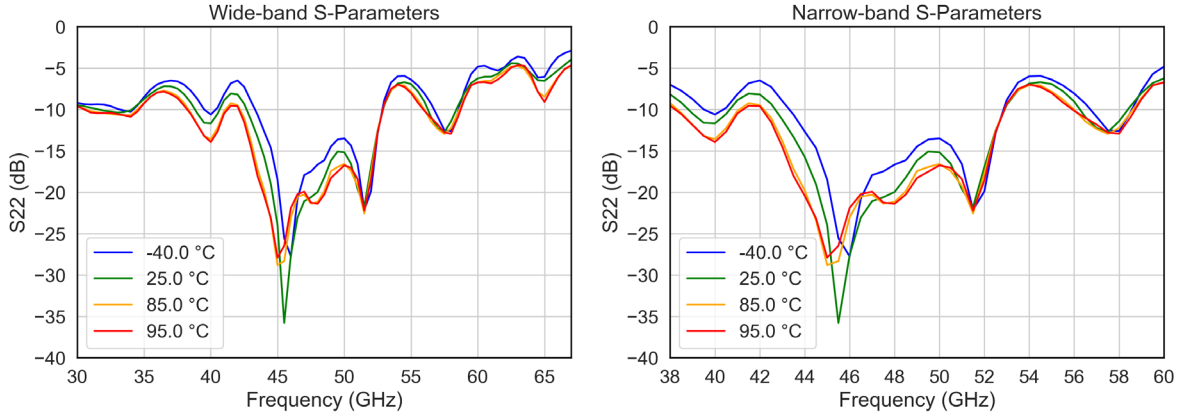
Linear Gain vs. Frequency & Temperature



Input Return Loss vs. Frequency & Temperature



Output Return Loss vs. Frequency & Temperature



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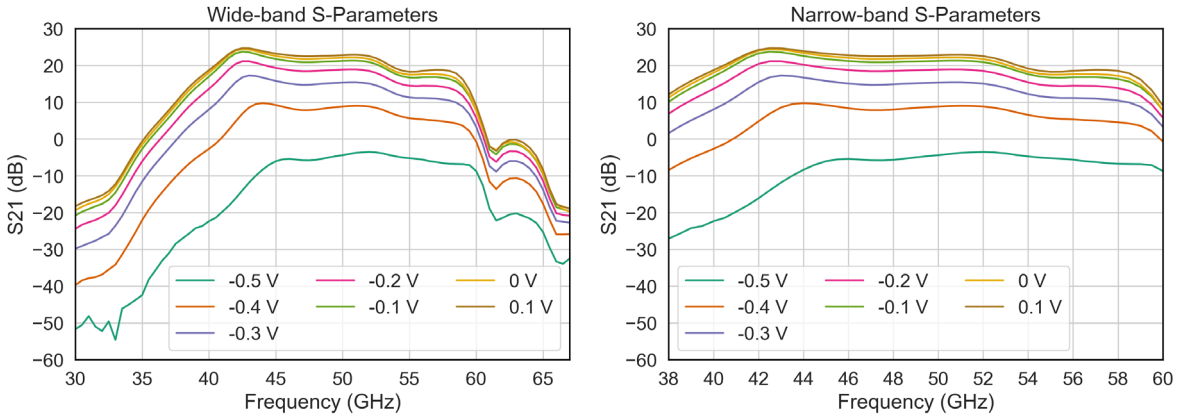
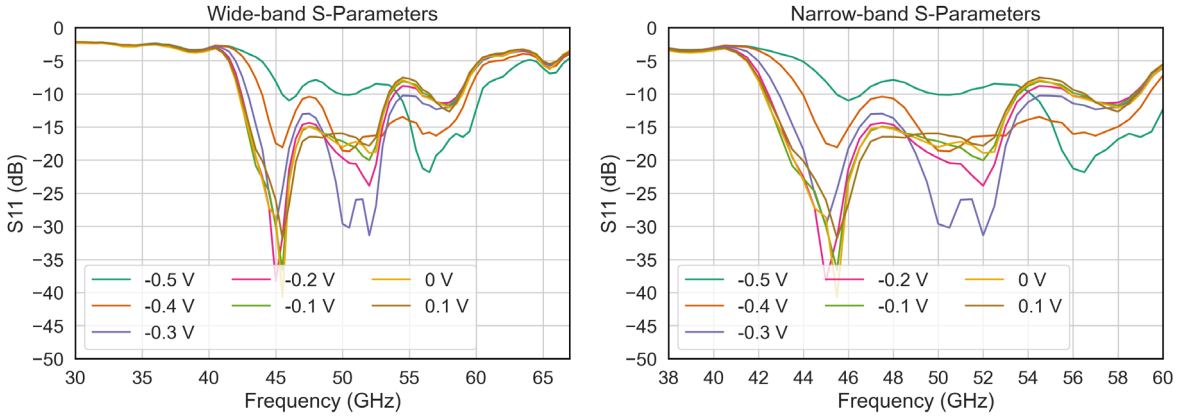
Typical on Board Measurements

Test conditions : $T_{backside}$ = +25°C, Vd = 3.3V, Vg = -0.5 to +0.1V
Board losses are de-embedded. Measurements are given in the die access plans.

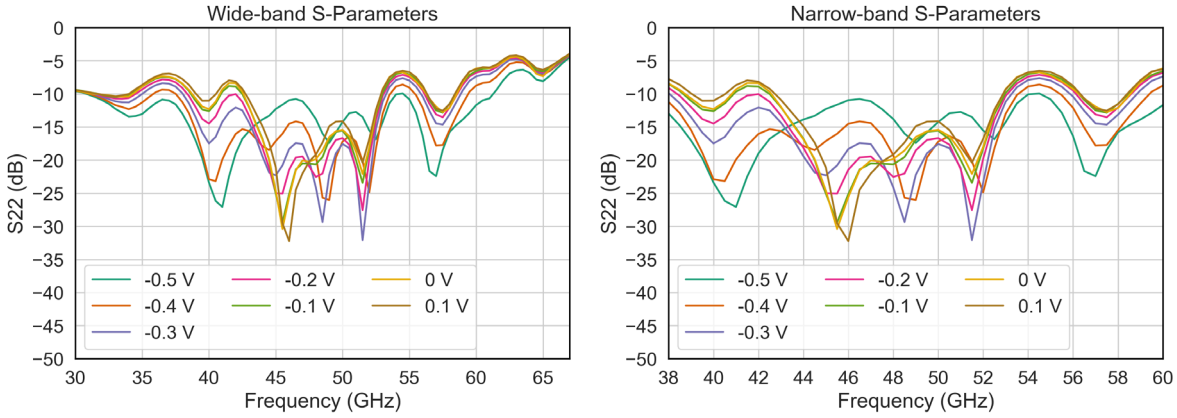
Linear Gain vs. Frequency & Gate voltage



Input Return Loss vs. Frequency & Gate voltage



Output Return Loss vs. Frequency & Gate voltage



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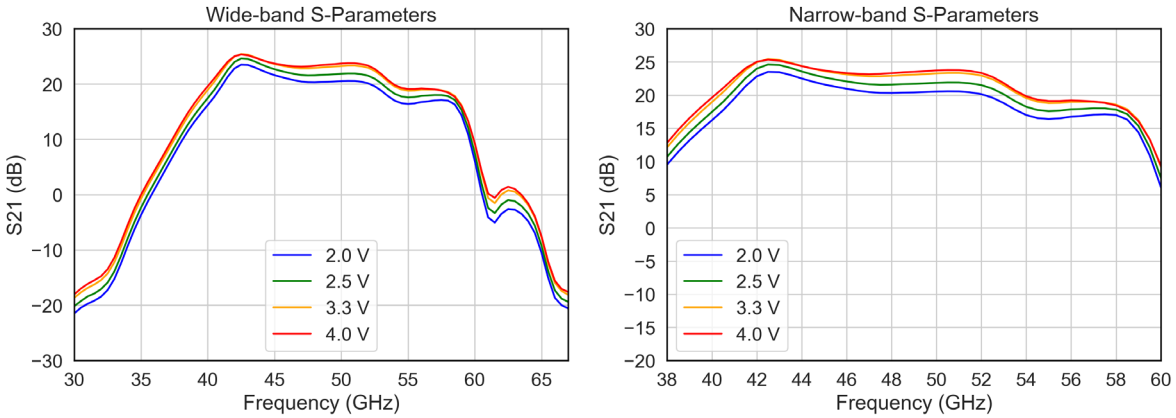
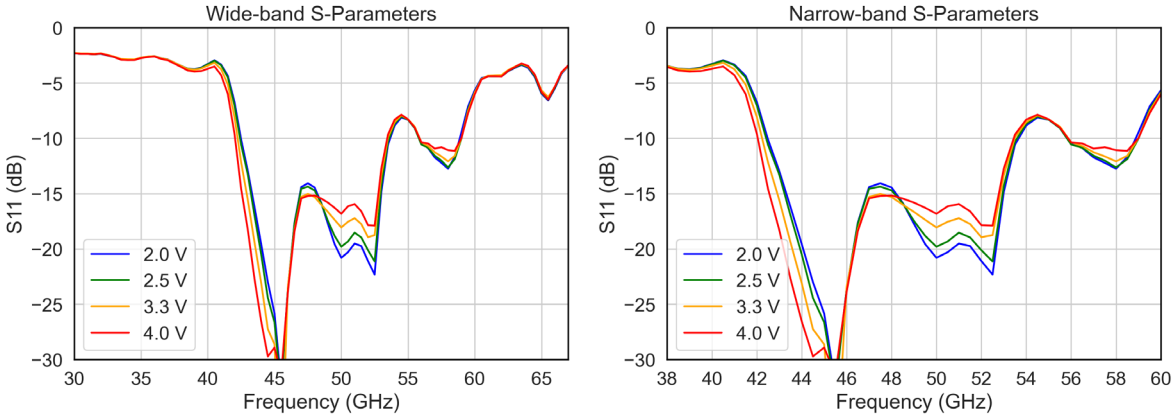
Typical on Board Measurements

Test conditions : $T_{backside}$ = +25°C, Vd = 2/2.5/3.3/4V, Id =40/45/55/65mA (Vg≈0V)
Board losses are de-embedded. Measurements are given in the die access plans.

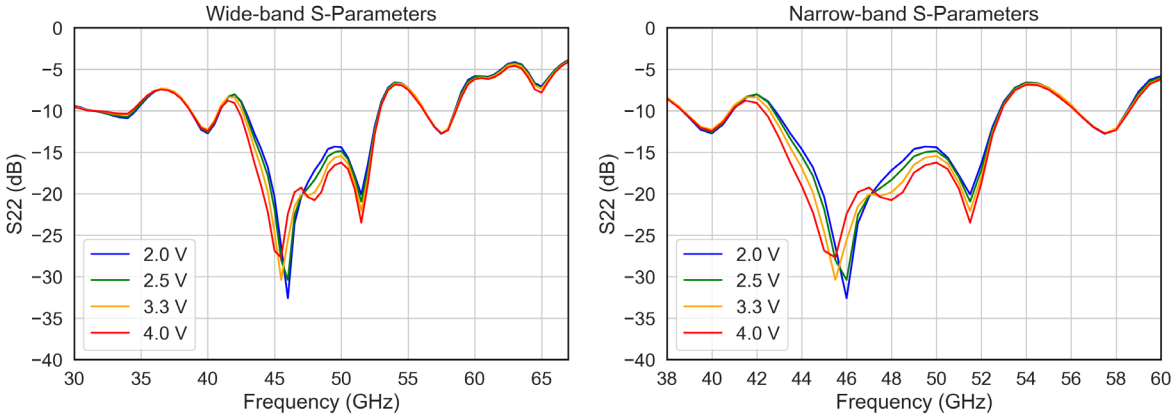
Linear Gain vs. Frequency & Drain voltage



Input Return Loss vs. Frequency & Drain voltage



Output Return Loss vs. Frequency & Drain voltage



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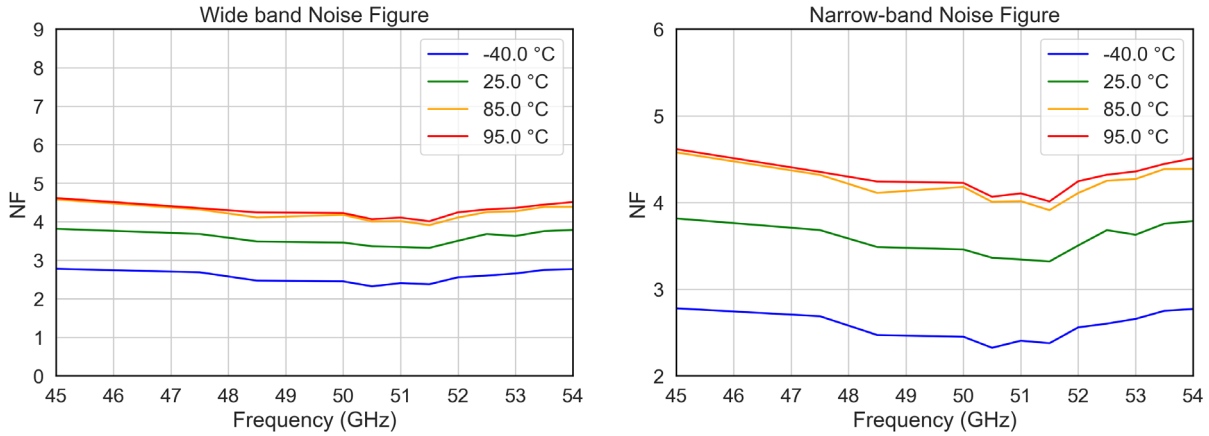
Typical on Board Measurements

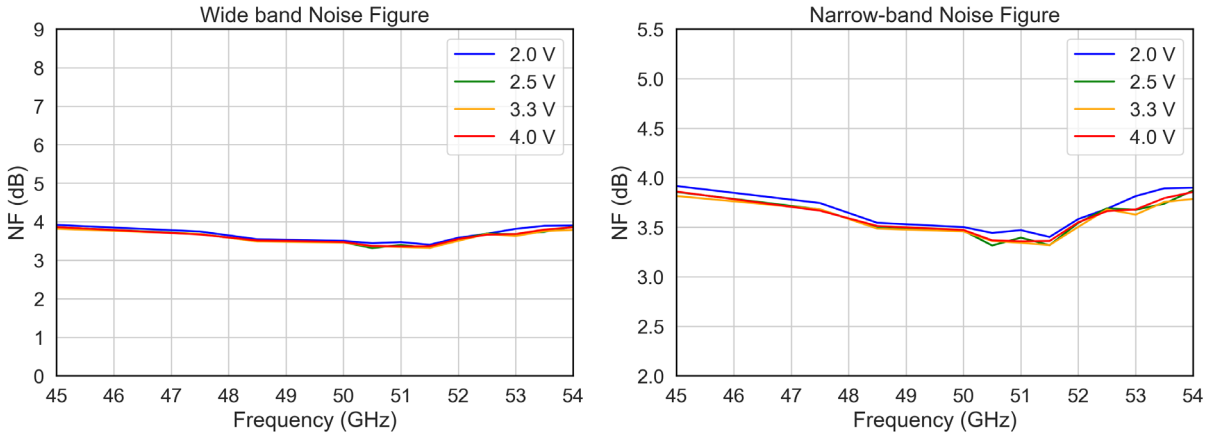
Test conditions : $T_{backside}$ = -40°C/+25°C/85°C/95°C, Vd = 3.3V, Id = 55mA
Board losses are de-embedded. Measurements are given in the die access plans.

Noise Figure vs. Frequency & Temperature



Test conditions : $T_{backside}$ = +25°C, Vd = 2/2.5/3.3/4V, Id =40/45/55/65mA
Board losses are de-embedded. Measurements are given in the die access plans.

Noise Figure vs. Frequency & Drain voltage & Tbackside = 25°C



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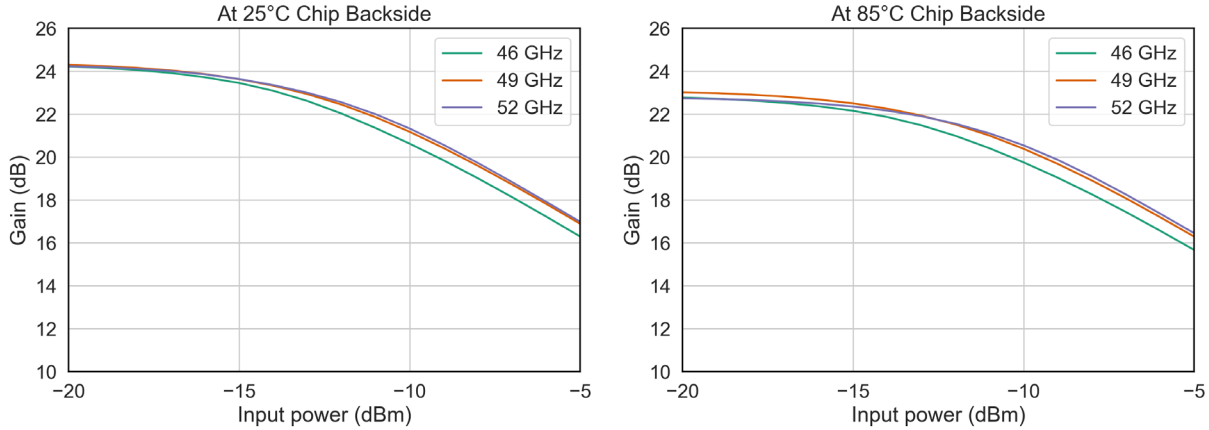
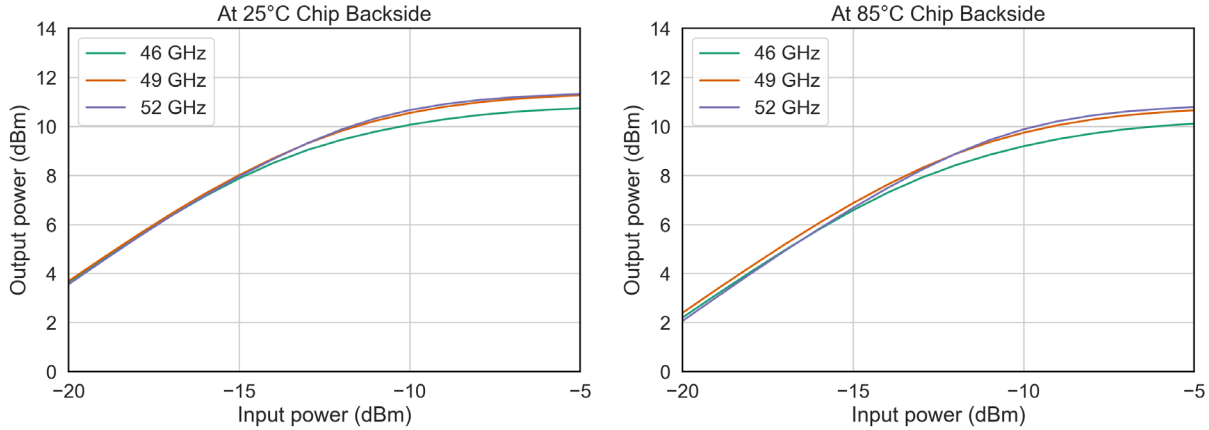
Typical on Board Measurements

Test conditions : $T_{backside}$ = +25°C/85°C, Vd = 3.3V, Id = 55mA
Board losses are de-embedded. Measurements are given in the die access plans.

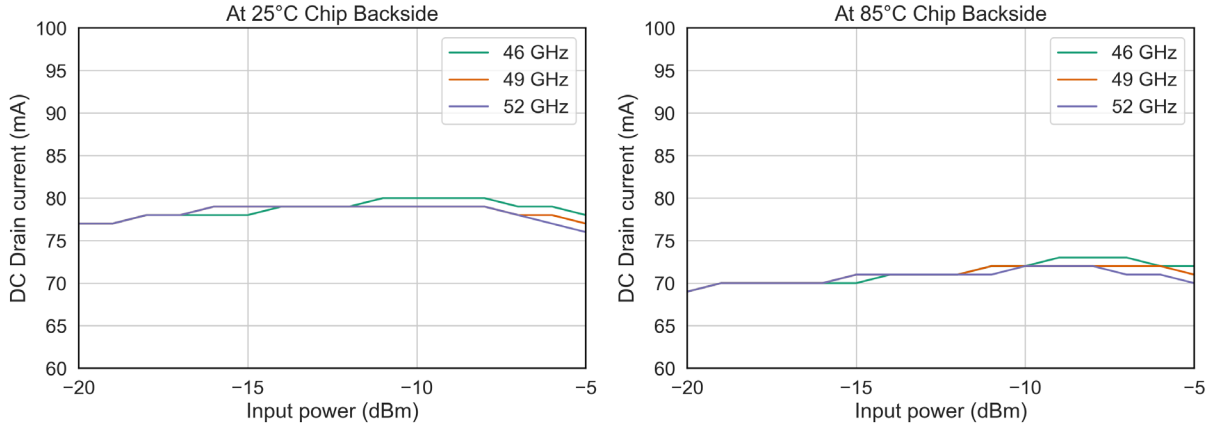
Gain vs. Input Power & Frequency



Output Power vs. Input Power & Frequency



Drain Current vs. Input Power & Frequency



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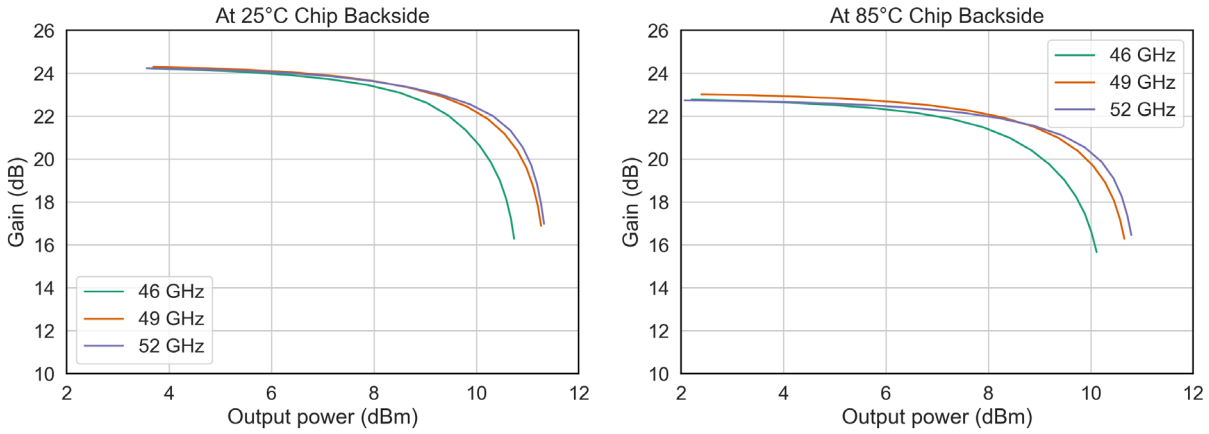
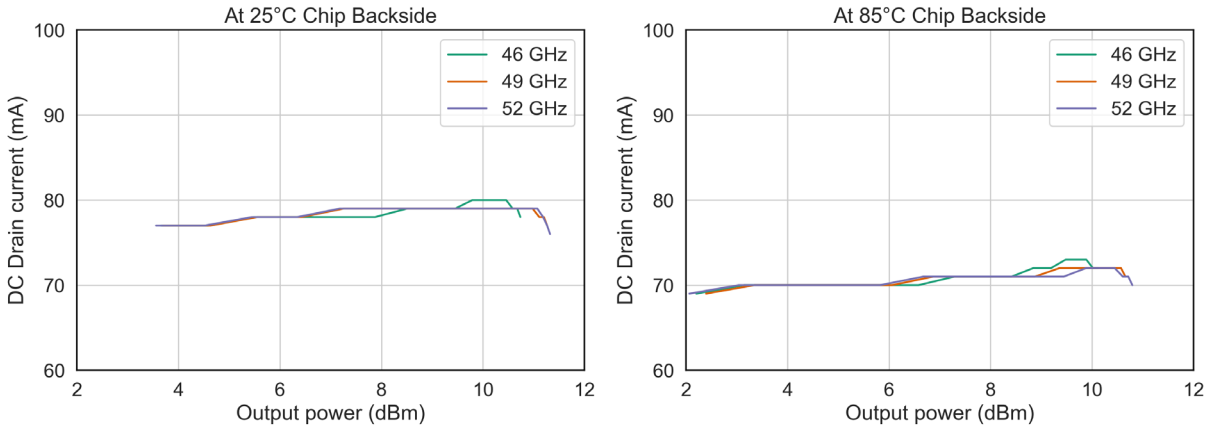
Typical on Board Measurements

Test conditions : $T_{backside}$ = +25°C/85°C, Vd = 3.3V, Id = 55mA
Board losses are de-embedded. Measurements are given in the die access plans.

Gain vs. Output Power & Frequency



Drain Current vs. Output Power & Frequency



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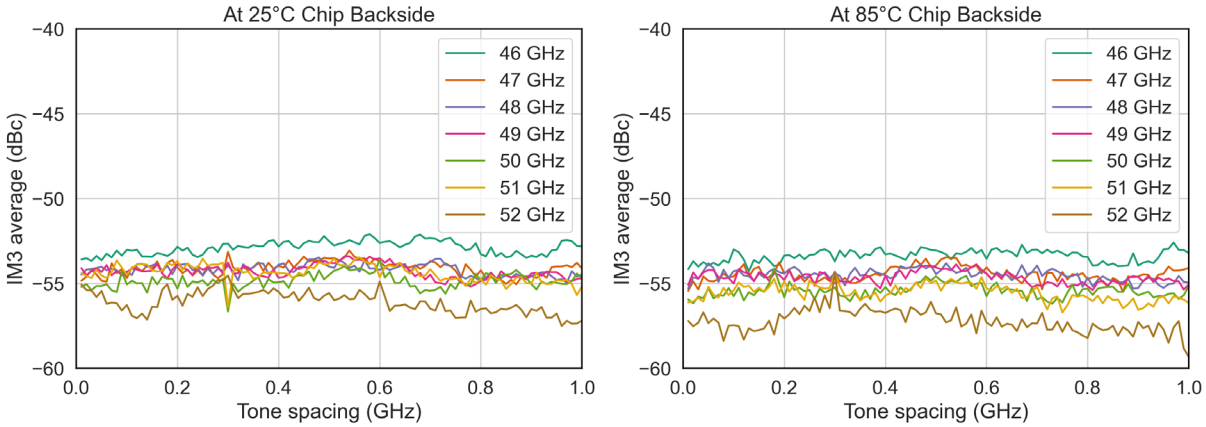
Typical Board Measurements

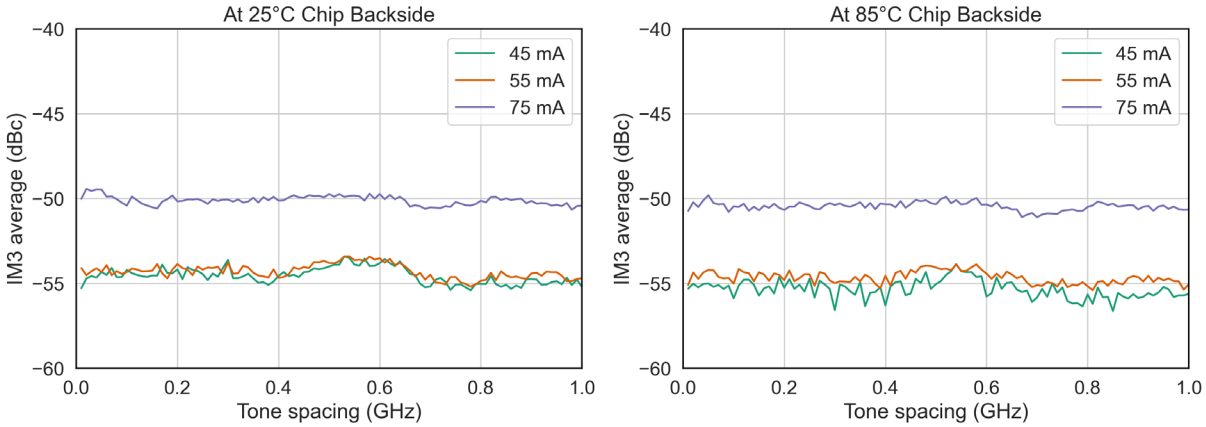
Test conditions : CW dual tones, Vd = 3.3V, Idq = 55mA, Pin/tone = -30dBm, $T_{backside}$ = +25°C/85°C

IMD3 vs. Tone Spacing & Frequency



Test conditions : CW dual tones, Vd = 3.3V, Fc = 49GHz, Pin/tone = -30dBm, $T_{backside}$ = +25°C/85°C

IMD3 vs. Tone Spacing & Drain Current



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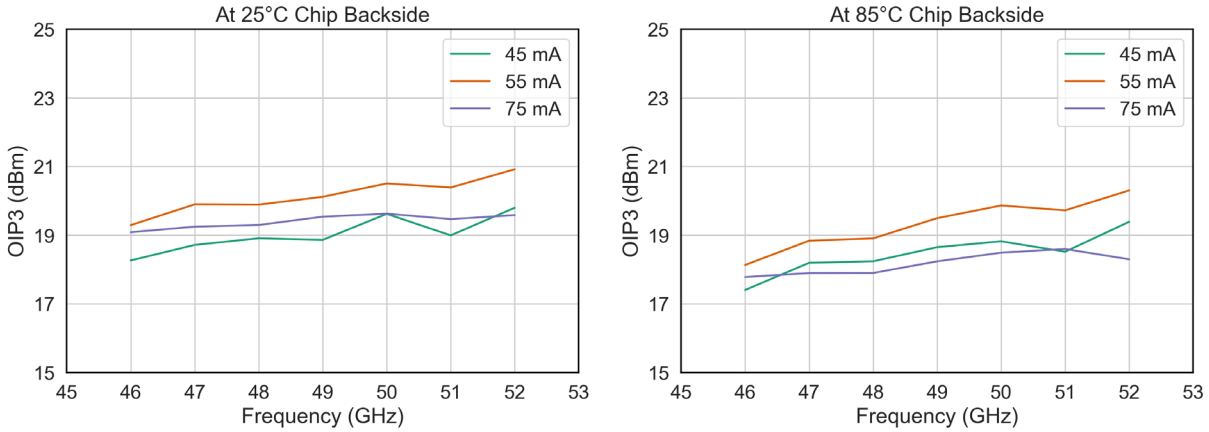
Typical Board Measurements

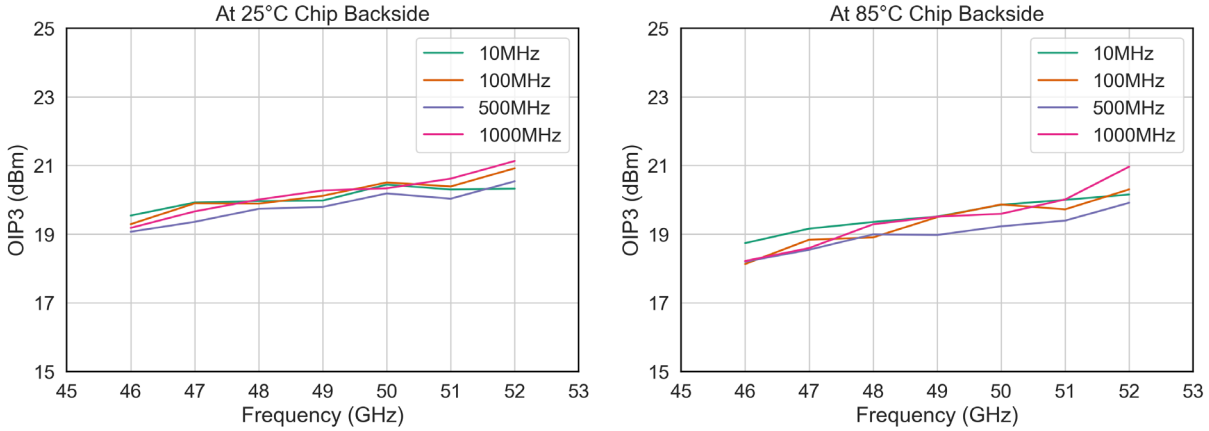
Test conditions : CW dual tones, Vd = 3.3V, Idq = 45/55/75mA, Δf = 10MHz, Pin/tone = -30dBm,

OIP3 vs. Frequency & Quiescent Drain Current



Test conditions : CW dual tones, Vd = 3.3V, Idq = 55mA, Δf = 10/100/500/1000MHz, Pin/tone = -30dBm

OIP3 vs. Frequency & Tone spacing



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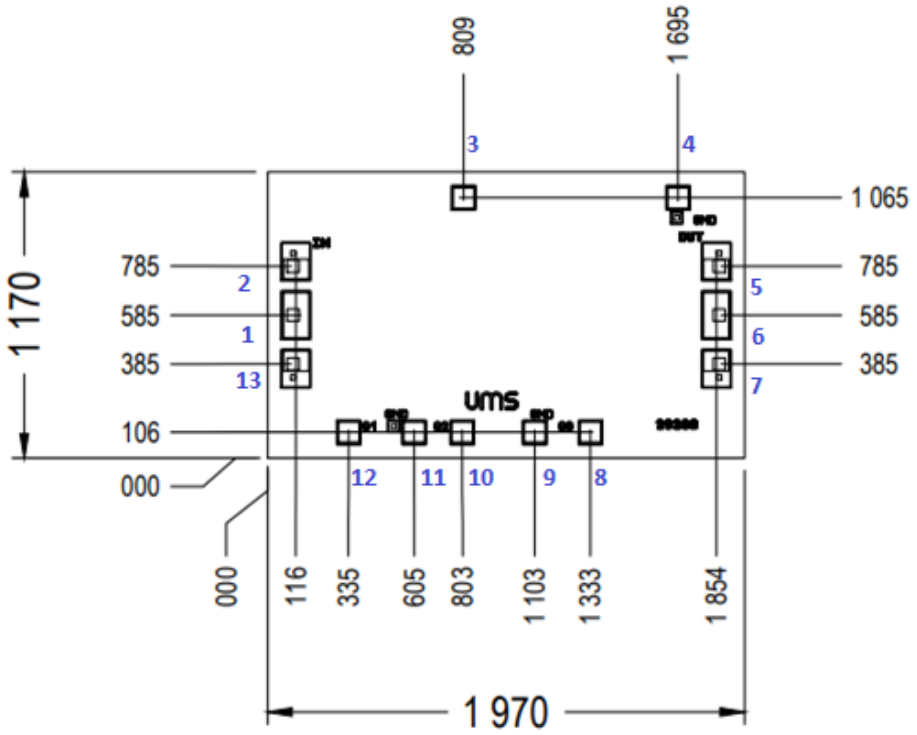
Mechanical data

Chip thickness: 70µm
Chip size: 1970µmx1170µm ±35µm
All dimensions are in micrometers



PAD Number	Name	Description	Pad size (BCB Opening)
1	RF IN	Input RF port	186µm x 105µm
3	D	DC Drain voltage all stages	86µm x 83µm
6	RF OUT	Output RF port	186µm x 105µm
8	G3	DC Gate voltage 3rd stage	86µm x 83µm
10	G2	DC Gate voltage 2nd stage	86µm x 83µm
12	G1	DC Gate voltage 1st stage	86µm x 83µm
4,9,11	GND	Ground DC	86µm x 83µm
2,5,7,13	GND	Ground RF	105 µm x 82 µm

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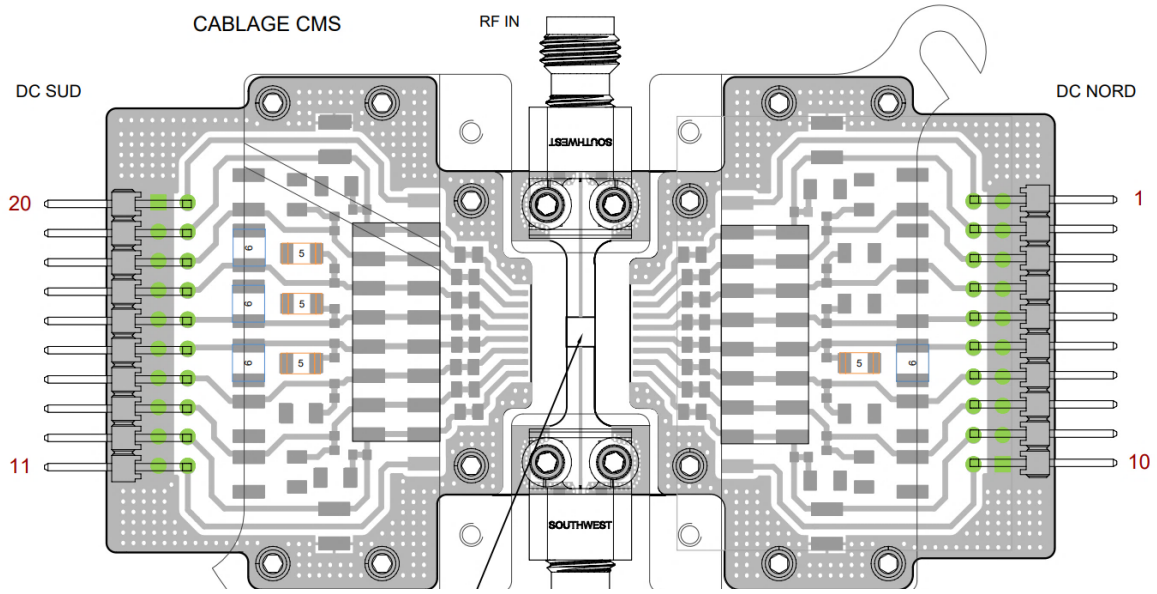
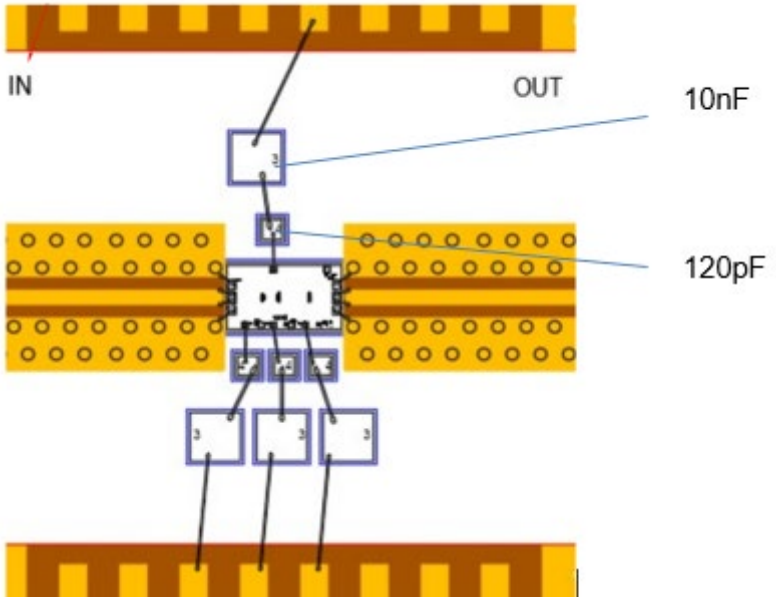
Evaluation board





Total of 4 levels of decoupling capacitors have been used, 2 levels on the tab and 2 levels on the board. The first level is composed of 120pF chip capacitors, the second level is composed of 10nF chip capacitors and the third level is composed of 100nF capacitors and 1µF for the last. The first two levels should be as close as possible to the chip.

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Recommended reflow process assembly

Refer to the application note AN0001 available at http://www.ums-rf.com for die attach.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at http://www.ums-rf.com.

Recommended ESD management

Refer to the application note AN0020 available at http://www.ums-rf.com for ESD sensitivity and handling recommendations for the UMS die products.

Recommended Evaluation board assembly

Refer to the application note AN0030 available at https://www.ums-rf.com for the description of Evaluation Board and recommendations for this UMS die product.

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Ordering request reference

Chip form:	CHA2353-99F/00

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