

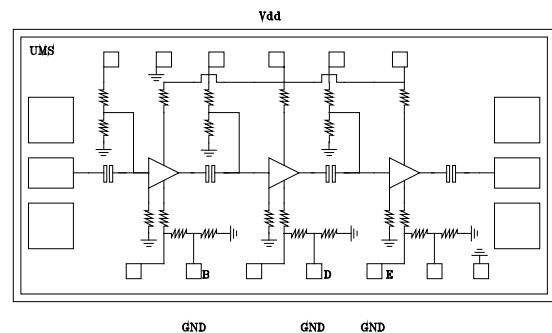
## 17-24GHz Low Noise Amplifier

### GaAs Monolithic Microwave IC

#### Description

The CHA2090-99F is a wide band Low Noise Monolithic Amplifier which integrates three amplification stages that produces 23dB gain associated to 2dB Noise Figure.

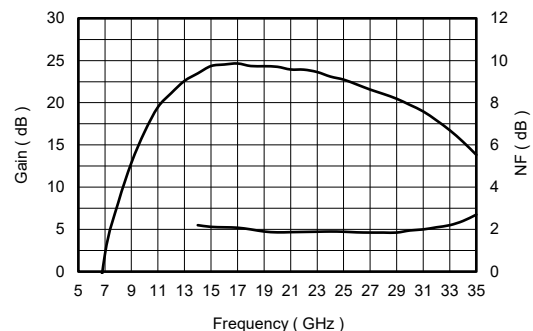
It is designed for a wide range of applications, from military to commercial communication systems. The circuit is manufactured with a pHEMT process.



It is available in chip form.

#### Main Features

- Broadband performance 17-24GHz
- 2.0dB Noise Figure
- 23dB gain,  $\pm 1$ dB gain flatness
- Low DC power consumption, 55mA
- Chip size: 2.17 x 1.27 x 0.1mm



On wafer typical measurement

#### Main Characteristics

$T_{\text{backside}} = +25^{\circ}\text{C}$ ,  $V_d = 4.5\text{V}$ , Pads B,D,E = GND

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	17		24	GHz
Gain	Linear Gain	19	23		dB
NF	Noise Figure		2.0	3.0	dB
VSWRin	Input VSWR		2:1		
VSWRout	Output VSWR		2:1		

## Specifications

$T_{\text{backside}} = +25^{\circ}\text{C}$ ,  $V_d = 4.5\text{V}$ , Pads B, D, E = GND

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	17		24	GHz
Gain	Linear Gain	19	23		dB
NF	Noise Figure		2.0	3.0	dB
P1dB	Output power at 1dB gain compression		10		dBm
VSWRin	Input VSWR <sup>(1)</sup>		2:1		
VSWRout	Output VSWR <sup>(1)</sup>		2:1		
Vd	Drain supply voltage <sup>(2)</sup>		4.5		V

(1) These values are representative of on-wafer measurements that are made without bonding wires at the RF ports. When the chip is attached with typical 0.15nH input and output bonding wires, the indicated parameter values should be improved.

(2) See chip biasing option page 9/10.

These values are representative of onboard measurements as defined on the drawing in paragraph "Evaluation board".

**Absolute Maximum Ratings** <sup>(1)</sup>T<sub>backside</sub> = 25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	5.5	V
Pin	Maximum peak input power	+15	dBm
Tj	Maximum junction temperature	175	°C

<sup>(1)</sup> Operation of this device above any one of these parameters may cause permanent damage.

**Recommended Operating Range**

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	4 to 5	V
Idq	Quiescent current	55	mA
Vg	Gate bias voltage	-3.0 to +0.10	V
Pin	Maximum peak input power	+6	dBm
Tj	Maximum junction temperature	175	°C

**Temperature Range**

$T_{\text{backside}}$	Operating temperature range	-40 to +85	°C
$T_{\text{stg}}$	Storage temperature range	-55 to +150	°C

**“Power ON” sequence**

1. Bias LNA gate voltage at  $V_g$  close to  $V_{\text{pinch-off}}$  (Typically:  $V_g \approx -3.0V$ )
2. Apply  $V_d$  bias voltage (Typically:  $V_d = 4.5V$ )
3. Increase gate voltage  $V_g$  up to quiescent bias drain current  $I_{dq}$
4. Apply RF signal

**“Power OFF” sequence**

1. Turn off RF signal
2. Bias LNA gate voltage at  $V_g$  close to  $V_{\text{pinch-off}}$  (Typically:  $V_g \approx -3.0V$ )
3. Check that quiescent bias drain current  $I_{dq}$  is close to 0mA
4. Turn  $V_d$  bias voltage to 0V
5. Check that quiescent bias drain current  $I_{dq}$  is close to 0mA
6. Turn  $V_g$  bias voltage to 0V

**Device thermal performances**

All the figures given in this section are obtained assuming that the chip device is only cooled down by conduction through the package thermal pad (no convection mode considered).

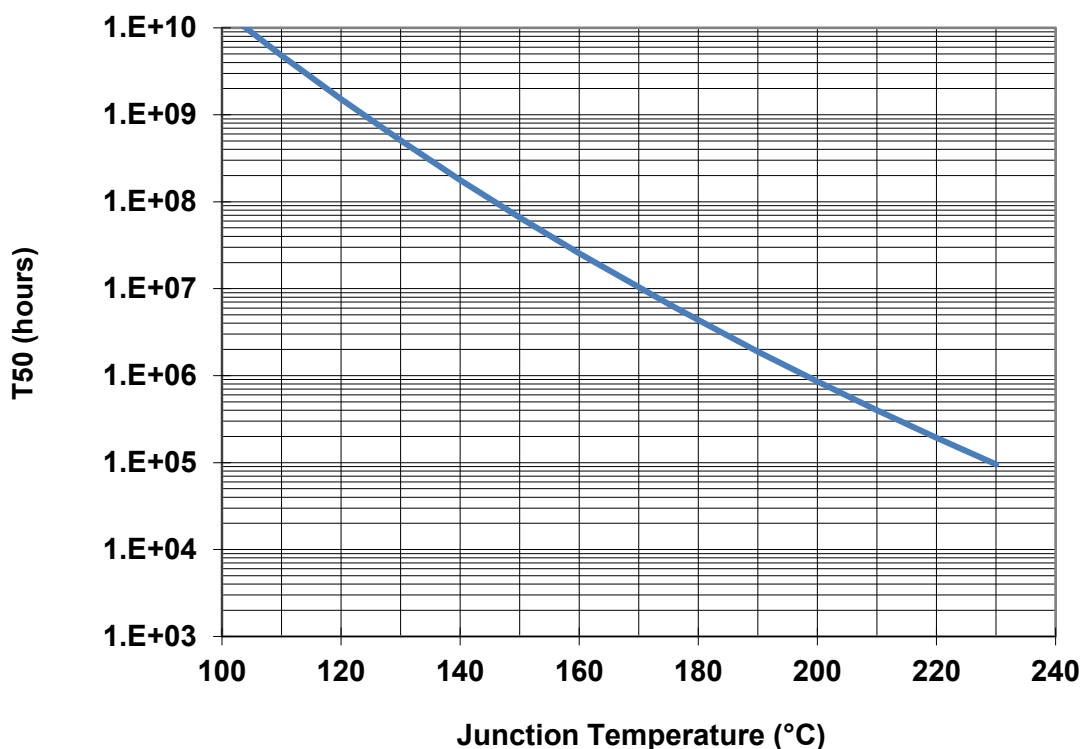
The temperature is monitored at the chip back-side interface ( $T_{backside}$ ).

The system maximum temperature must be adjusted in order to guarantee that  $T_{junction}$  remains below the maximum value specified in the Absolute Maximum Ratings table.

So, the system PCB must be designed to comply with this requirement.

Parameter	Biasing conditions	Tjunction (°C)	RTH (°C/W)	T50 (hours)
RTH <sup>(1)</sup> Thermal Resistance (Junction to Case)	Vd= 4.5V Idq= 55mA Pdiss= 0.2475W	116	130	4E+09

<sup>(1)</sup> Assuming 85°C  $T_{backside}$



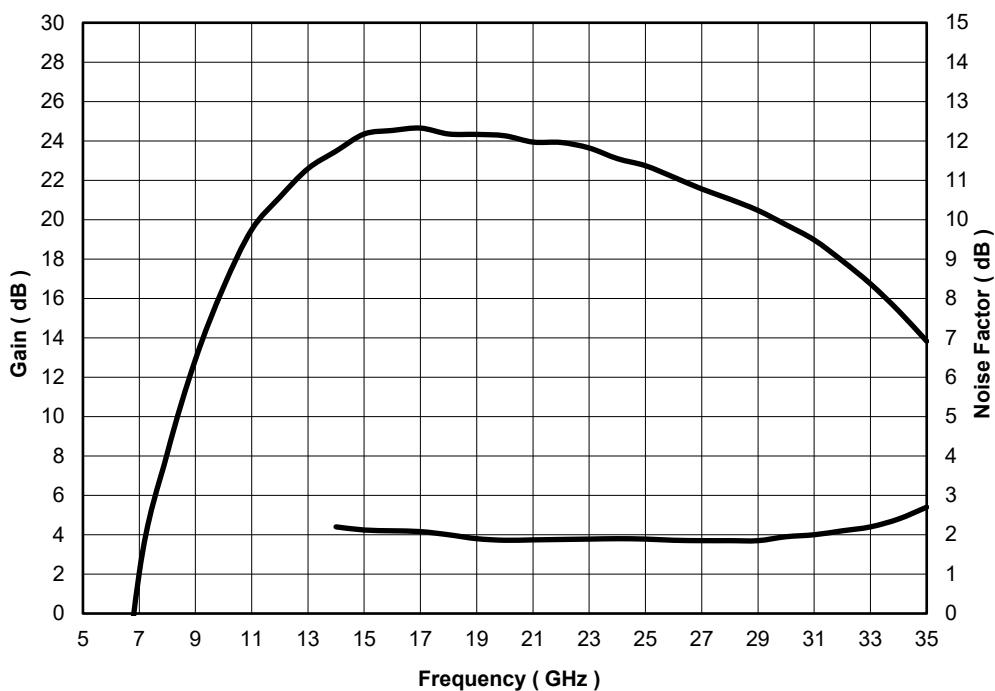
## Typical Scattering Parameters (on Wafer)

T<sub>backside</sub> = +25°C, V<sub>d</sub> = 4.5V, I<sub>d</sub> = 55mA

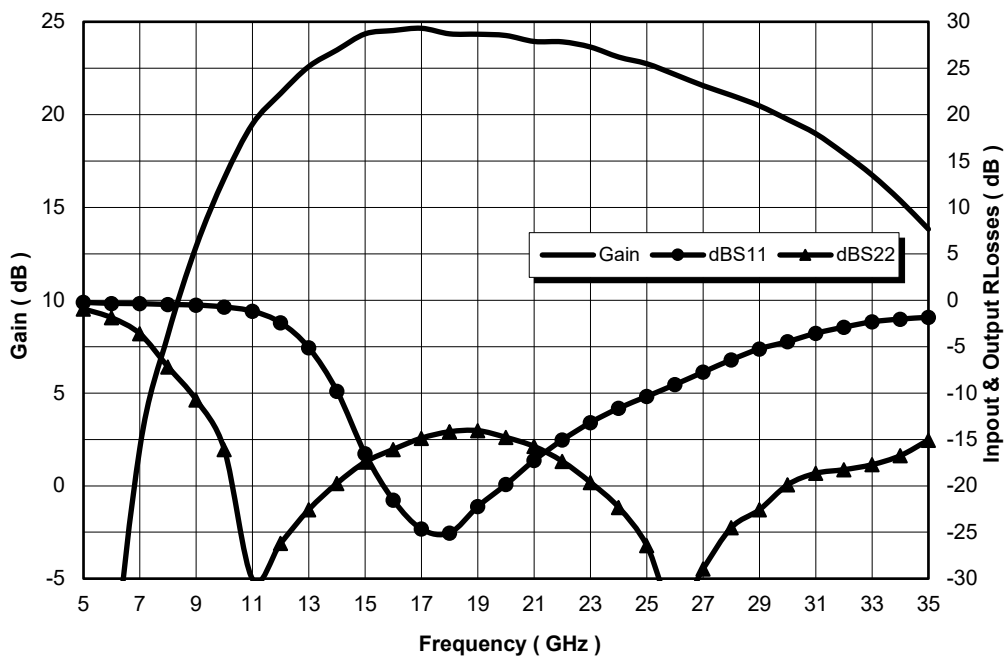
Frequency	S11 <i>mod</i>	PhS11 <i>pha</i>	S12 <i>mod</i>	PhS12 <i>pha</i>	S21 <i>mod</i>	PhS21 <i>pha</i>	S22 <i>mod</i>	PhS22 <i>pha</i>
GHz	dB	deg	dB	deg	dB	deg	dB	deg
1.000	-0.53	-20.8	-89.62	-92.0	-41.76	-148.5	-0.72	-23.8
2.000	-0.06	-39.0	-97.43	26.6	-48.17	170.5	-0.30	-50.3
3.000	-0.10	-58.5	-87.21	-23.0	-52.46	74.5	-0.33	-75.6
4.000	-0.16	-77.4	-84.87	-135.7	-61.22	154.8	-0.49	-101.9
5.000	-0.23	-96.5	-83.35	120.1	-35.86	-69.1	-0.89	-129.8
6.000	-0.34	-115.2	-66.23	84.2	-12.12	-123.6	-1.77	-159.0
7.000	-0.35	-134.1	-72.40	-58.1	1.34	145.9	-3.35	168.8
8.000	-0.45	-154.1	-73.93	-13.6	7.48	75.4	-6.63	141.1
9.000	-0.52	-175.4	-72.23	-7.1	11.96	18.3	-9.34	119.1
10.000	-0.75	160.3	-66.01	-34.2	15.54	-28.2	-13.97	85.5
11.000	-1.21	132.1	-60.26	-60.3	18.30	-72.2	-22.57	53.2
12.000	-2.33	97.8	-56.60	-94.9	19.92	-116.5	-39.69	-60.4
13.000	-4.60	57.2	-53.53	-135.9	21.36	-163.1	-30.19	-133.1
14.000	-8.86	8.5	-52.43	-173.4	22.49	149.3	-25.30	-127.8
15.000	-16.48	-40.4	-52.50	157.8	23.60	100.6	-21.56	-134.5
16.000	-24.70	-70.2	-52.26	135.4	23.89	62.2	-19.34	-144.1
<b>17.000</b>	<b>-27.75</b>	<b>-80.6</b>	<b>-52.62</b>	<b>108.9</b>	<b>24.01</b>	<b>28.4</b>	<b>-17.60</b>	<b>-158.0</b>
<b>18.000</b>	<b>-23.51</b>	<b>-87.4</b>	<b>-51.36</b>	<b>100.6</b>	<b>23.66</b>	<b>-1.9</b>	<b>-16.51</b>	<b>-172.3</b>
<b>19.000</b>	<b>-21.41</b>	<b>-95.7</b>	<b>-51.27</b>	<b>60.6</b>	<b>23.52</b>	<b>-30.5</b>	<b>-16.34</b>	<b>163.7</b>
<b>20.000</b>	<b>-18.63</b>	<b>-107.0</b>	<b>-54.07</b>	<b>52.8</b>	<b>23.46</b>	<b>-57.8</b>	<b>-17.75</b>	<b>149.6</b>
<b>21.000</b>	<b>-16.77</b>	<b>-115.6</b>	<b>-55.06</b>	<b>30.3</b>	<b>23.11</b>	<b>-84.4</b>	<b>-19.33</b>	<b>131.6</b>
<b>22.000</b>	<b>-14.95</b>	<b>-123.2</b>	<b>-57.35</b>	<b>23.7</b>	<b>23.14</b>	<b>-111.0</b>	<b>-22.26</b>	<b>113.9</b>
<b>23.000</b>	<b>-13.73</b>	<b>-132.0</b>	<b>-59.54</b>	<b>8.0</b>	<b>22.82</b>	<b>-137.3</b>	<b>-25.44</b>	<b>89.1</b>
<b>24.000</b>	<b>-12.59</b>	<b>-138.8</b>	<b>-60.85</b>	<b>32.3</b>	<b>22.36</b>	<b>-162.8</b>	<b>-29.95</b>	<b>43.8</b>
25.000	-11.60	-144.7	-62.07	49.5	22.01	171.8	-28.26	-24.5
26.000	-10.61	-149.8	-54.29	40.2	21.46	147.9	-22.90	-58.9
27.000	-9.34	-154.5	-55.03	23.9	20.91	125.0	-19.22	-84.3
28.000	-7.89	-160.6	-52.05	-11.6	20.49	102.3	-17.12	-102.6
29.000	-6.63	-171.3	-60.41	-22.1	20.06	78.5	-16.20	-114.2
30.000	-5.86	179.9	-56.56	23.2	19.50	55.4	-14.73	-123.1
31.000	-4.83	172.0	-52.73	-13.7	19.03	31.5	-13.72	-137.5
32.000	-3.95	161.7	-54.11	-40.7	18.31	6.9	-13.60	-147.0
33.000	-3.18	151.2	-54.59	-51.2	17.51	-17.5	-13.61	-155.8
34.000	-2.61	140.2	-55.15	-37.9	16.54	-42.3	-14.22	-161.4
35.000	-2.15	129.3	-51.68	-92.2	15.35	-66.8	-14.94	-161.8
36.000	-1.77	117.9	-57.64	-111.2	13.94	-91.0	-15.31	-154.5
37.000	-1.65	106.7	-60.87	-68.5	12.41	-114.4	-13.87	-143.9
38.000	-1.64	95.9	-53.10	-33.4	10.67	-137.5	-11.60	-140.4
39.000	-1.65	85.9	-47.45	-99.7	8.76	-159.6	-9.18	-143.5
40.000	-1.76	75.2	-46.80	-137.0	6.70	178.9	-7.06	-151.0

Typical on Wafer Measurements

T<sub>backside</sub> = +25°C, V<sub>d</sub> = 4.5V, I<sub>d</sub> = 55mA



Gain & Noise Figure vs. Frequency

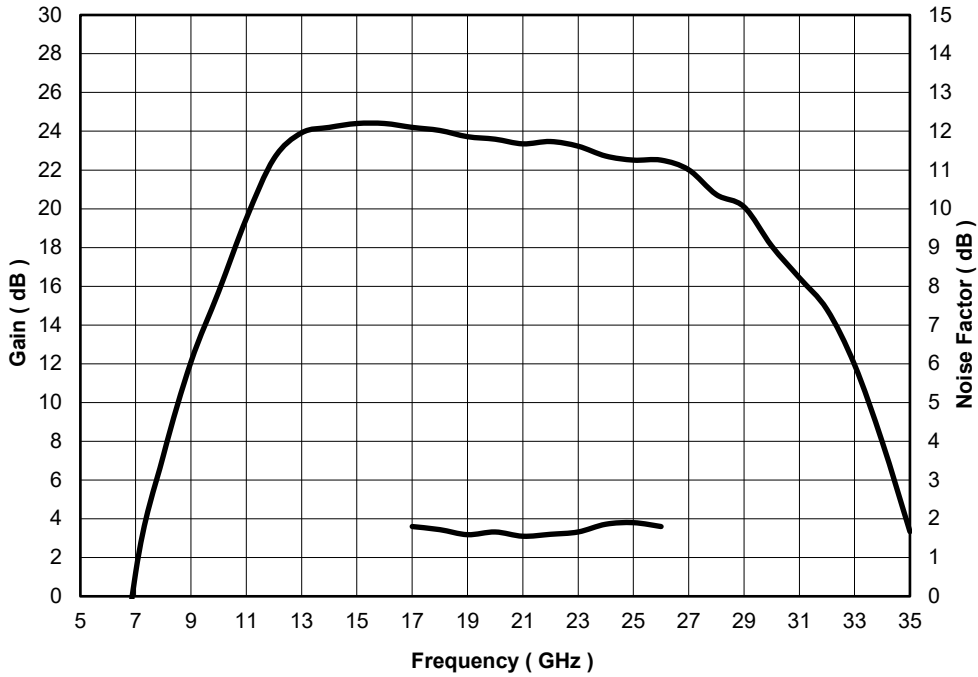


Gain & Input and Output Loss vs. Frequency

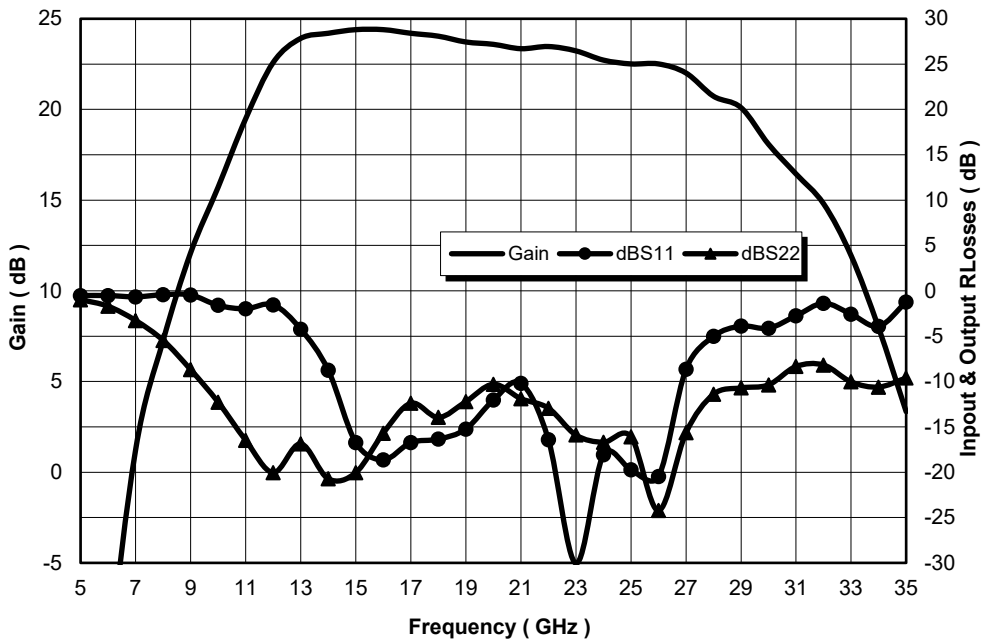


Typical on Evaluation Board Measurements

T<sub>backside</sub> = +25°C, V<sub>d</sub> = 4.5V, I<sub>d</sub> = 55mA



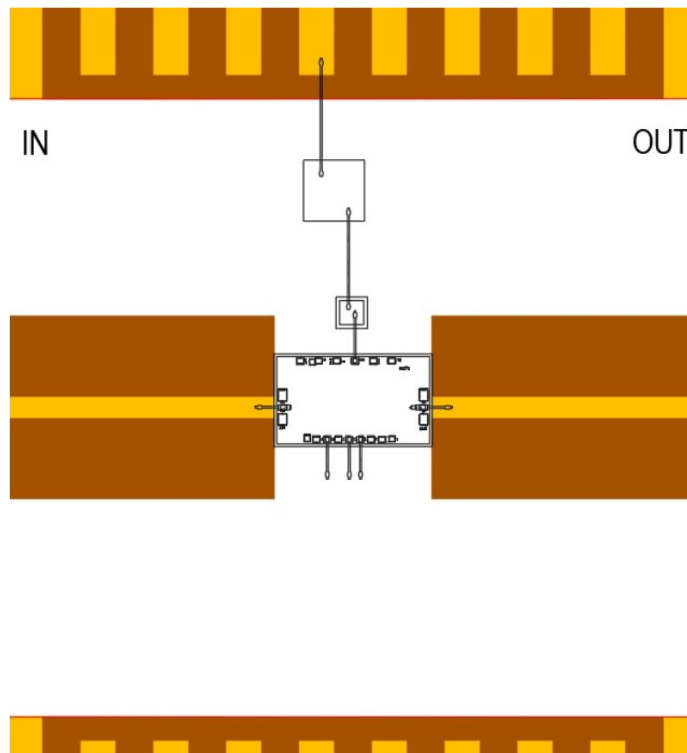
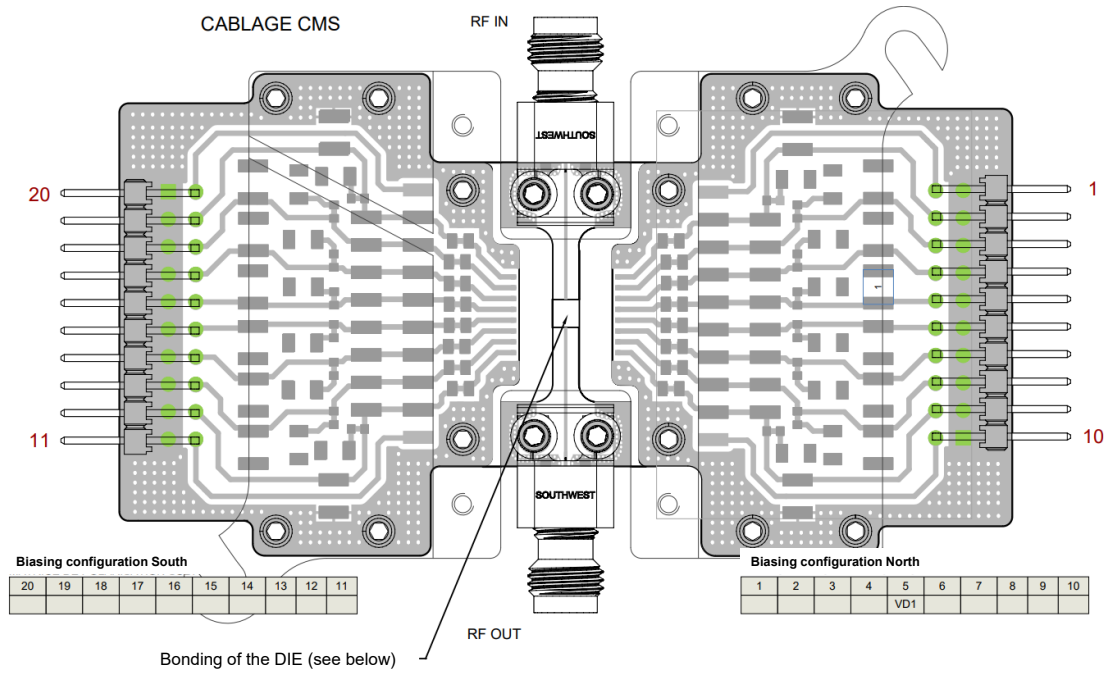
Gain & Noise Figure vs. Frequency



Gain & Input and Output Loss vs. Frequency

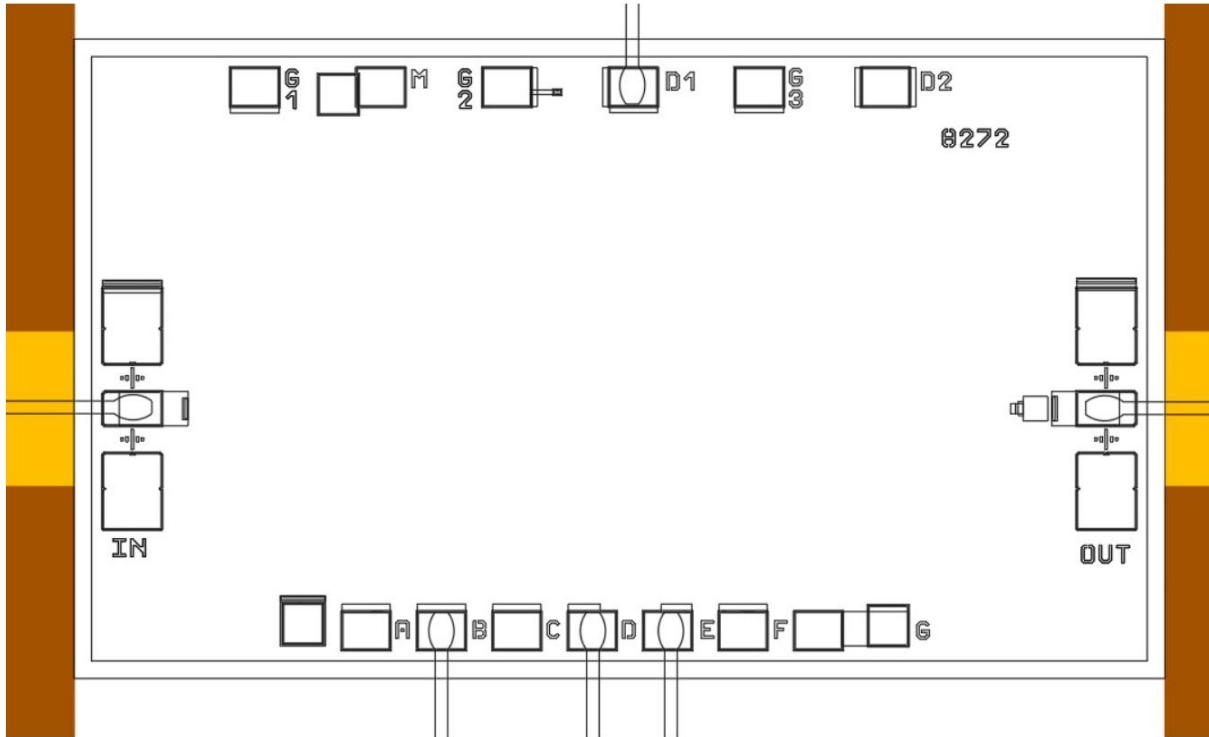


Evaluation board



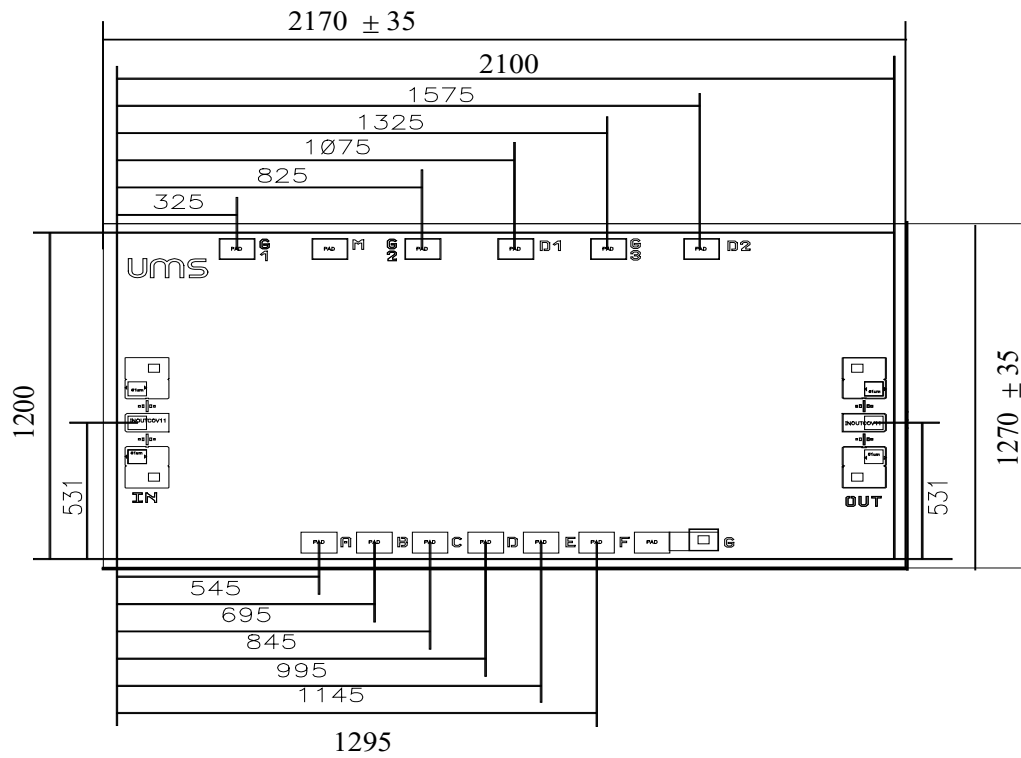
See next page for recommended assembly plan

## Recommended Assembly Plan (zoom in)



Three levels of decoupling capacitors are recommended. The first and second levels are composed of 120pF and 10nF chip capacitors, the third level is composed of 1µF SMD capacitors. The first level should be as close as possible to the die. PADS B,D and E are grounded.

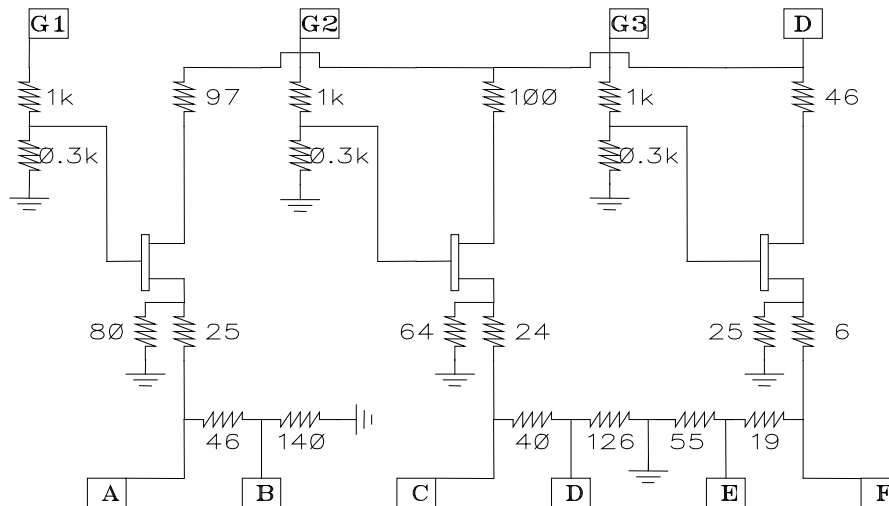
**Mechanical Data**



**Bonding pad positions.**  
 (Chip thickness:  $100\mu\text{m}$ . Pad size:  $100 \times 80\mu\text{m}^2$ )  
 (All dimensions are in micrometers)

## Chip Biasing Options

This chip is self-biased, and flexibility is provided by the access to number of pads. The internal DC electrical schematic is given in order to use these pads in a safe way.



The two requirements are:

- N°1: Not exceed  $V_{ds} = 3.5V$  (internal Drain to Source voltage)
- N°2: Not biased in such a way that  $V_{gs}$  becomes positive (internal Gate to Source voltage)

Low Noise and low consumption biasing condition:

- $V_d = 4.5V$  and B, D, E grounded
- All the other pads non connected (NC)
- $I_d = 55mA$  and  $P_{out-1dB} = 10dBm$

**Note**

## Recommended reflow process assembly

Refer to the application note AN0001 available at <https://www.ums-rf.com> for die attach.

## Recommended ESD management

Refer to the application note AN0020 available at <https://www.ums-rf.com> for ESD sensitivity and handling recommendations.

## Recommended Evaluation board assembly

Refer to the application note AN0030 available at <https://www.ums-rf.com> Evaluation board.

## Ordering Information

Die form	CHA2090-99F/00
Evaluation board	EVB-CHA2090-99F

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