United Monolithic Semiconductors

CHA2069-QDG

18-31GHz Low Noise Amplifier

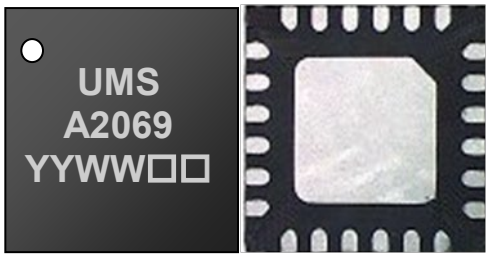
GaAs Monolithic Microwave IC in SMD leadless package

Description

The CHA2069-QDG is a three-stage self-biased wide band monolithic low noise amplifier. Typical applications range from telecommunication (point to point, point to multi-point, VSAT) to ISM and military markets.

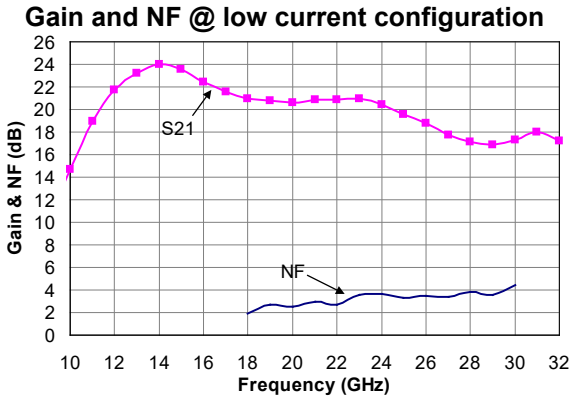
The circuit is manufactured with a standard pHEMT process, via holes through the substrate, air bridges and electron beam gate lithography.

It is supplied in low cost SMD RoHS compliant QFN plastic package.



Main Features

- Frequency Range: 18-31GHz
- Noise Figure: 3dB
- Linear Gain: 20dB
- Bias: Vd = 4.5V and Idq = 65mA
- 3rd order intercept point (low current configuration): 18dBm
- 24L-QFN Plastic Package 4x4 mm^2
- MSL1



Main Characteristics

Tcase = +25°C, Vd = +4.5V Pads: B, D, E = GND (Low consumption configuration)

Symbol	Parameter	Min	Typ	Max	Unit
NF	Noise Figure		3	4.5	dB
Gain	Linear Gain	17	20		dB
IP3	3rd order intercept point (Pout/tone=-5dBm) 18-26GHz	18	20		dBm

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Electrical Characteristics (low current configuration)

Tcase = +25°C, Vd = +4.5V, pads: B, D, E = GND

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Operating frequency range	18		31	GHz
G	Gain	16.5	19.5		dB
ΔG	Gain flatness		±2	±2.5	dB
NF	Noise Figure		3	4.5	dB
IS11I	Input return loss		-5	-2	dB
IS22I	Output return loss		-7	-2.5	dB
IP3	3rd order intercept point (Pout/tone=-5dBm) 18-26GHz	16.5	18.5		dBm
P1dB	Output power at 1dB gain compression	9	10.5		dBm
Id	Drain bias current		65		mA

These values are representative of onboard measurements as defined on the drawing in paragraph "Evaluation board".

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Absolute Maximum Ratings (1)

Tcase= +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	5	V
Pin	Maximum input power overdrive	+10	dBm
Top	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +150	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.

“Power ON” sequence

1. Ground the device
2. Set the gate voltage close to Vpinch-off (-1.5V)
3. Apply the drain voltage Vd (typically +4.5V)
4. Increase Vg up to quiescent bias drain current Id
5. Apply RF signal

“Power OFF” sequence

1. Turn off RF signal
2. Decrease the gate voltage to -1.5V
3. Decrease the drain voltage to 0V
4. Turn off Vd supply
5. Turn off Vg supply

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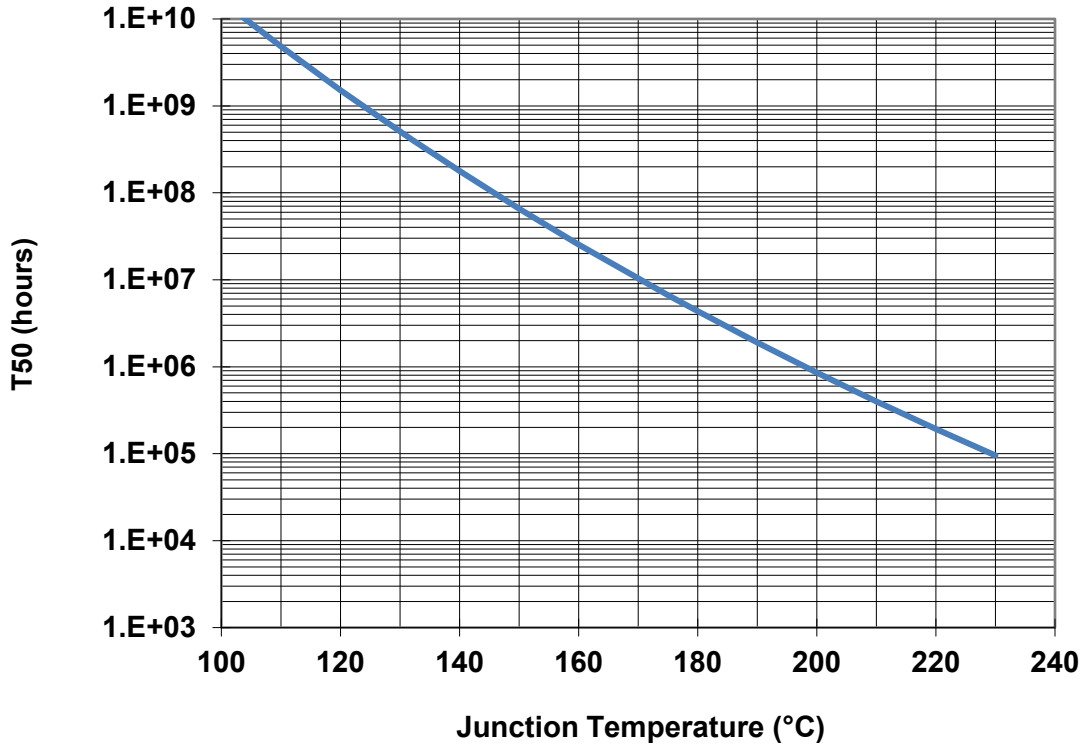
Device Thermal Performances

All the figures given in this section are obtained assuming that the QFN device is only cooled down by conduction through the package thermal pad (no convection mode considered). The temperature is monitored at the package back-side interface (Tcase). The system maximum temperature must be adjusted in order to guarantee that Tjunction remains below the maximum value specified in the Recommended Operating Range table. The system PCB must be designed to comply with this requirement.

Parameter	Conditions	Tjunction (°C)	Rth (°C/W)	T50 (hours)
Rth(1) Thermal Resistance (Junction to Case)	Vd = 4.5V Idq = 65mA Pdiss = 0.293W	132	161	4.1E+08

(1) Assuming 85°C Tcase



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Typical Package Sij parameters for low current configuration

Tcase = +25°C, Vd = +4.5V, pads: B, D, E = GND

Freq (GHz)	S11 (dB)	S11 (°)	S12 (dB)	S12 (°)	S21 (dB)	S21 (°)	S22 (dB)	S22 (°)
2	-0.1	-58.7	-95.2	-85.6	-57.5	-2.4	-0.6	-148.4
3	-0.1	-89.3	-68.8	63.3	-77.6	-24.4	-0.9	157.1
4	-0.1	-123.5	-63.2	93.4	-52.9	62.8	-0.9	112.4
5	-0.2	-160.8	-62.9	47.1	-37.4	145.3	-1.3	72.0
6	-0.4	156.1	-58.1	11.4	-18.1	93.6	-1.7	39.9
7	-0.6	107.6	-67.5	-59.7	-4.4	28.0	-2.0	8.4
8	-1.2	58.9	-68.1	93.7	4.4	-52.1	-3.0	-20.2
9	-1.8	13.5	-61.6	-9.2	9.6	-122.4	-3.9	-38.6
10	-2.8	-26.1	-60.0	-42.6	14.7	176.1	-4.4	-69.5
11	-4.0	-58.0	-55.1	171.8	19.0	109.4	-8.3	-92.5
12	-5.7	-89.1	-53.4	87.2	21.7	41.3	-13.4	-92.8
13	-8.8	-122.0	-49.6	14.1	23.3	-24.1	-17.0	-67.1
14	-15.8	-173.9	-50.5	-42.8	24.0	-86.8	-12.6	-36.0
15	-17.4	24.9	-48.2	-120.3	23.5	-146.2	-8.3	-46.7
16	-10.9	-20.6	-48.3	171.6	22.4	162.0	-6.3	-65.3
17	-8.5	-47.1	-49.6	133.4	21.5	116.9	-5.9	-85.2
18	-7.0	-65.5	-47.3	121.9	20.9	75.8	-5.9	-99.8
19	-6.2	-82.8	-44.9	92.5	20.8	34.2	-6.1	-116.0
20	-5.8	-98.4	-42.5	57.3	20.7	-6.5	-7.2	-130.1
21	-4.9	-110.8	-43.2	20.1	20.9	-48.3	-7.9	-137.3
22	-4.7	-125.9	-45.3	14.9	20.9	-90.8	-9.2	-142.4
23	-4.3	-138.7	-43.3	-0.5	20.9	-135.3	-8.7	-139.3
24	-3.9	-152.2	-43.7	-14.8	20.4	178.7	-7.6	-141.9
25	-3.8	-163.2	-44.2	-36.7	19.6	135.8	-6.3	-148.5
26	-3.3	-173.7	-45.4	-48.5	18.8	92.8	-4.4	-156.9
27	-3.0	175.5	-46.5	-43.8	17.8	52.7	-3.7	-169.0
28	-2.5	166.4	-43.7	-45.2	17.1	13.2	-3.0	-179.9
29	-2.5	155.4	-43.2	-59.5	16.8	-26.3	-2.7	171.2
30	-2.8	146.3	-42.0	-81.7	17.3	-69.6	-2.7	161.4
31	-3.9	144.4	-46.4	-112.7	18.0	-123.9	-2.6	156.1
32	-2.8	154.3	-47.9	-148.6	17.2	168.4	-2.5	150.5

The Sij measurement calibration planes are defined in the paragraph “Definition of the Sij reference planes”.

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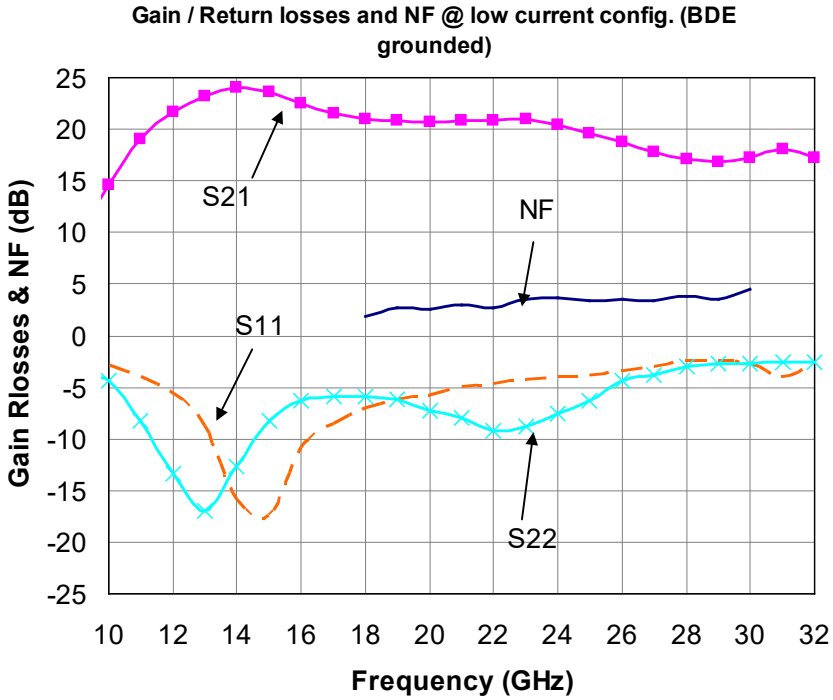
Typical on wafer Measurements

Tcase = +25°C, Vd = +4.5V

Measurements are given in the package access plans, using the proposed pattern and board given in the paragraph “Evaluation board”.



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Typical on wafer Measurements

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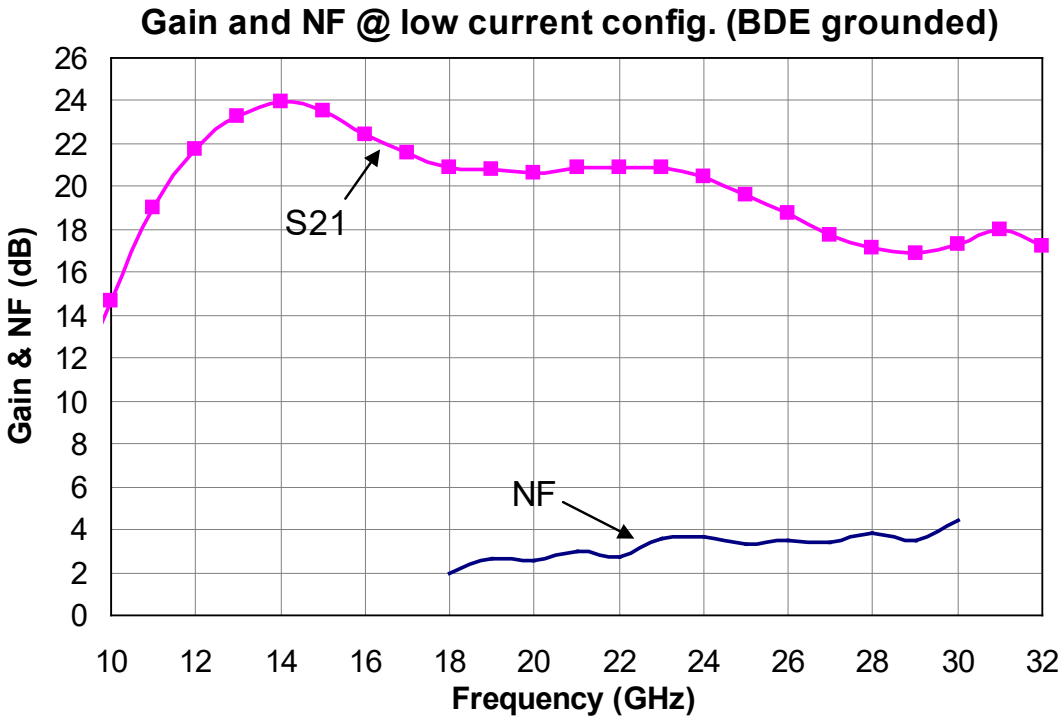

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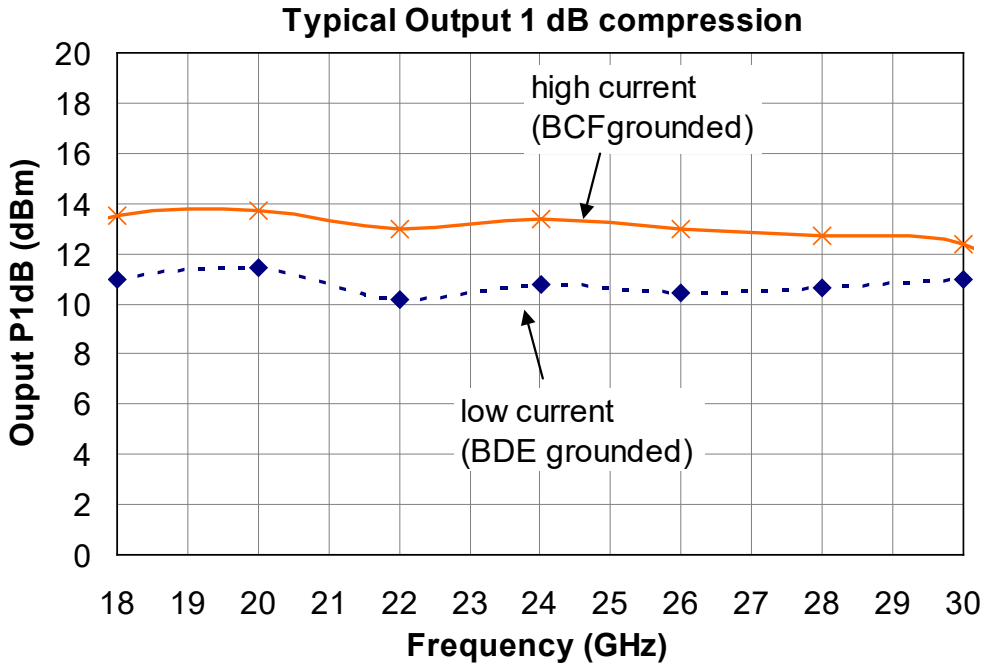
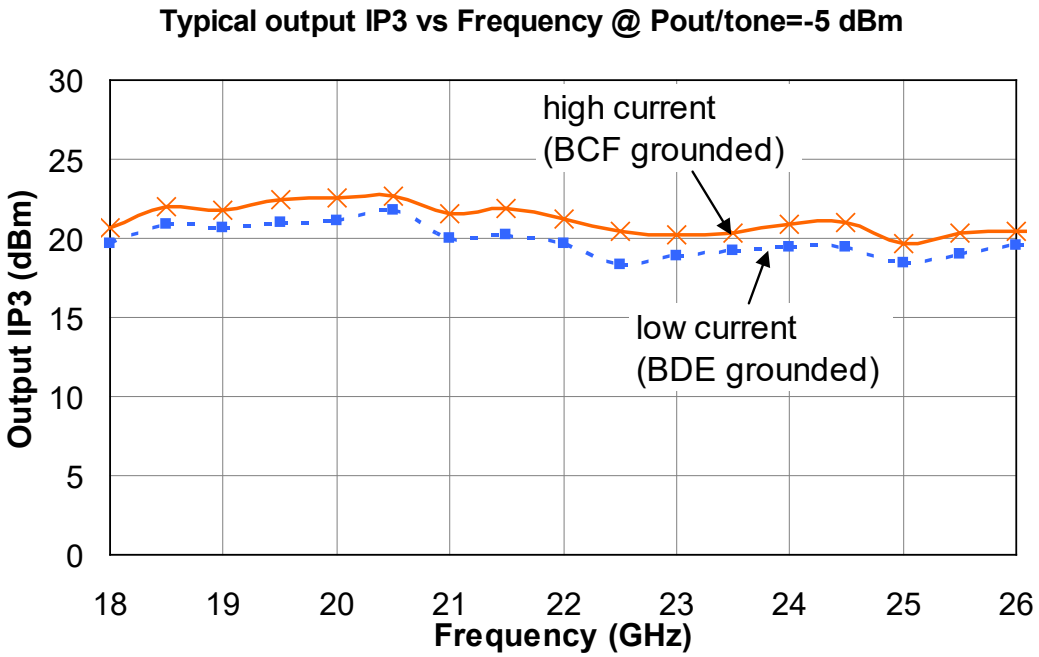
Typical Board Measurements

Tcase = +25°C, Vd = +4.5V
Measurements are given in the connectors' access plans, using the proposed land pattern and board given in the paragraph "Evaluation board".
For these measurements, losses due to board are not de-embedded.





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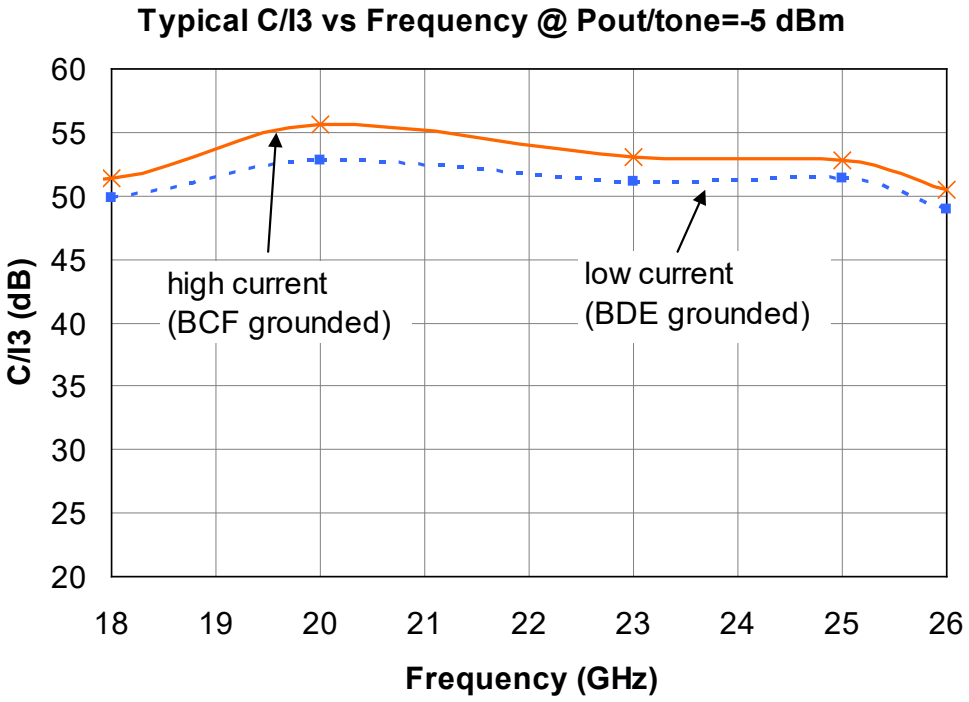
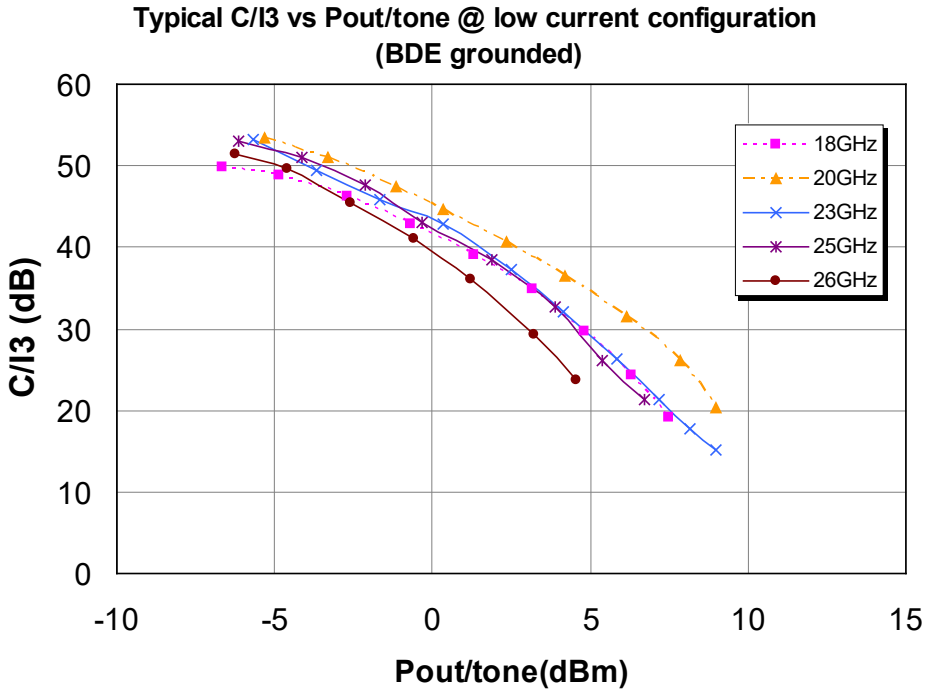
Typical Board Measurements

Tcase = +25°C, Vd = +4.5V





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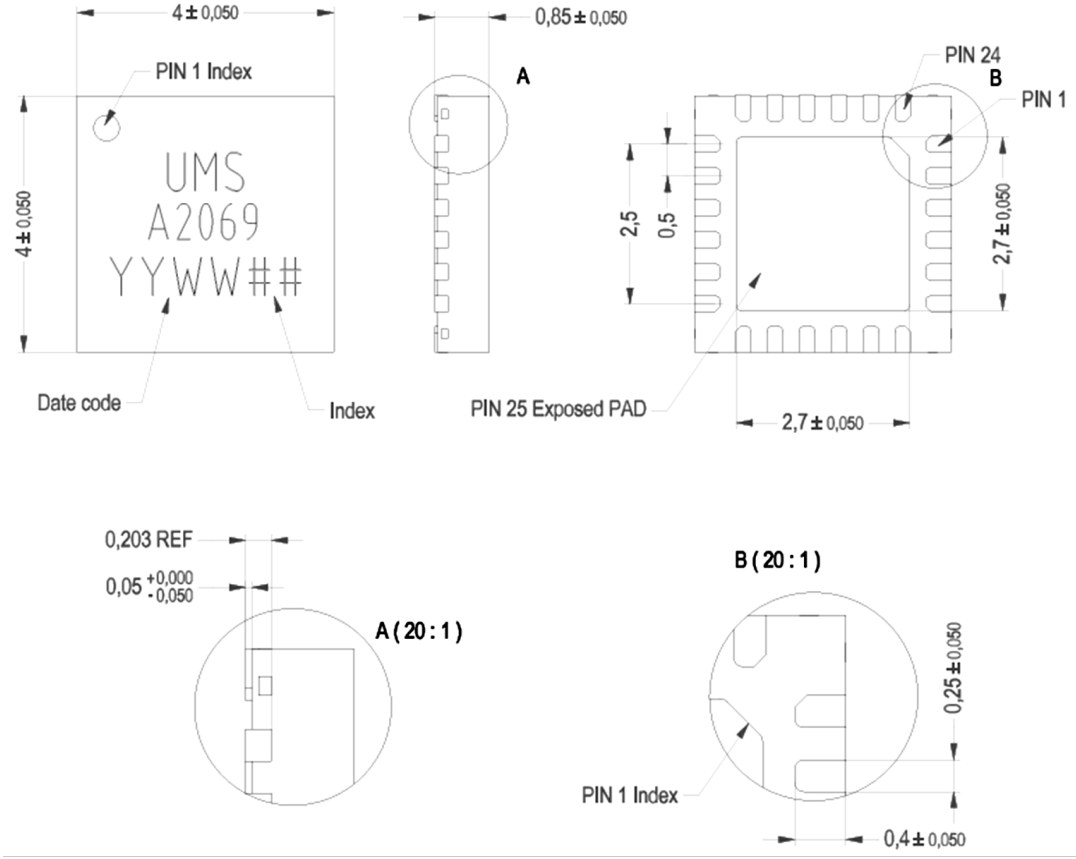
Package outline (1)



Matt tin, Lead Free	(Green)	1- NC (3)	13- NC (3)
Units	mm	2- NC (3)	14- GND(2)
From the standard	JEDEC MO-220 (VGGD)	3- GND(2)	15- RF OUT
		4- RF IN	16- GND(2)
25-	GND(2)	5- GND(2)	17- NC (3)
		6- NC (3)	18- NC (3)
		7- B	19- Vd
		8- C	20- Vd
		9- D	21- Vg3
		10- NC (3)	22- Vg2
		11- E	23- Vg1
		12- F	24- NC (3)

(1) Refer to the application note AN0017 (https://www.ums-rf.com) for general consideration and recommendations for molded plastic QFN/DFN packages.

(2) It is strongly recommended to ground all pins identified as GND through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

(3) NC: Not Connected.

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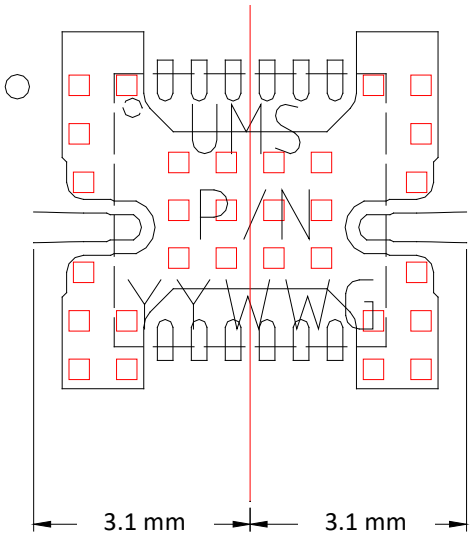
Definition of the Sij reference planes

The reference planes used for Sij measurements given above are symmetrical from the symmetrical axis of the package (see drawing beside). The input and output reference planes are located at 3.1mm offset (input wise and output wise respectively) from this axis. Then, the given Sij parameters incorporate the land pattern of the evaluation board recommended in paragraph "Evaluation board".



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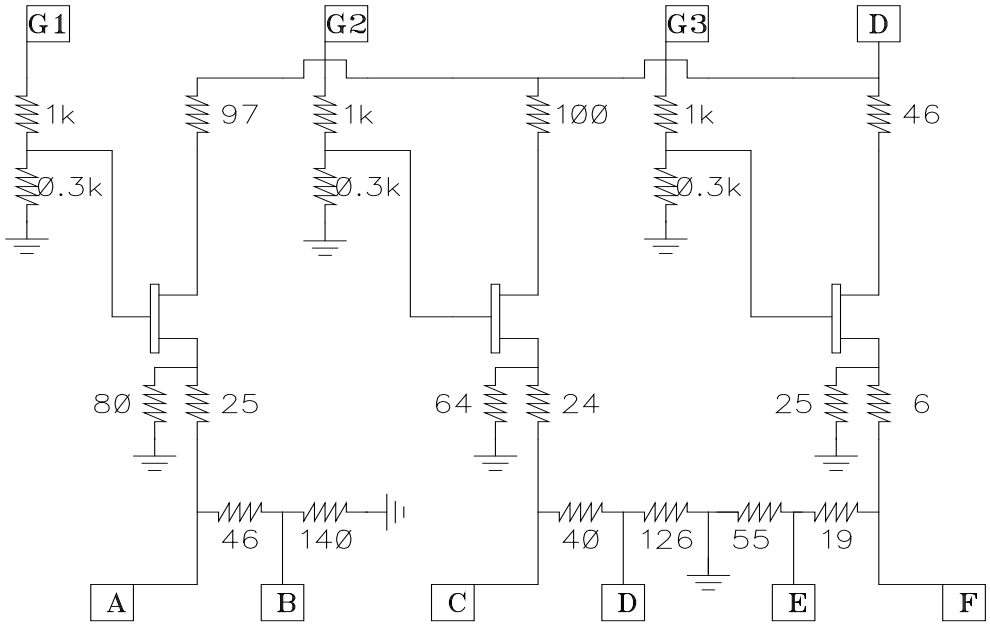
Chip Biasing Options

This circuit is self-biased, and flexibility is provided by the access to number of pads. The internal DC electrical schematic is given in order to use these pads in a safe way.



The two requirements are:

- N°1: Not exceed Vds = 3.5V(internal Drain to Source voltage)
- N°2: Not biased in such a way that Vgs becomes positive (internal Gate to Source voltage)

Low Noise and low consumption biasing condition:

- Vd = 4.5V and B, D, E grounded
- All the other pads Non Connected (NC)
- Id = 65mA & Pout-1dB = 10dBm

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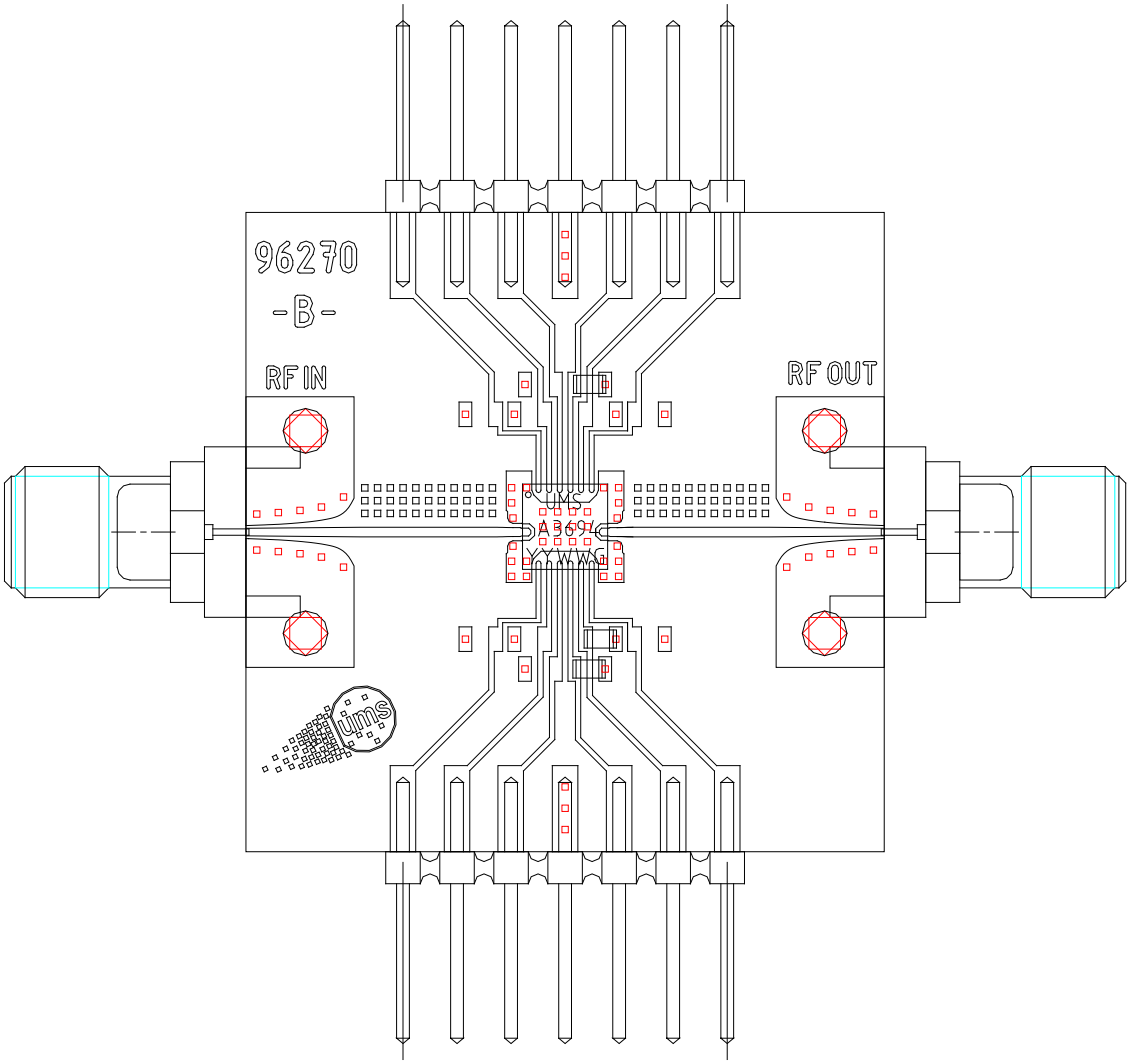
Evaluation Board

- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a micro-strip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 10nF ±10% are recommended for all DC accesses.
- See application note AN0017 for details.



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Recommended Package Footprint

Refer to the application note AN0017 available at https://www.ums-rf.com for package foot print recommendations.

SMD Mounting Procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017 at https://www.ums-rf.com.

Recommended Environmental Management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at https://www.ums-rf.com.

Recommended ESD Management

Refer to the application note AN0020 available at https://www.ums-rf.com for ESD sensitivity and handling recommendations for the UMS package products.

Description of Evaluation Board

Refer to the application note AN0031 available at https://www.ums-rf.com for the description of Evaluation Board for Packaged Die and recommendations for this UMS package product.

Ordering Information

QFN 4x4 package:	CHA2069-QDG/XY	
	Stick: XY = 20	Tape & reel: XY = 21
Evaluation Board:	EDG-CHA2069-QDG	

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