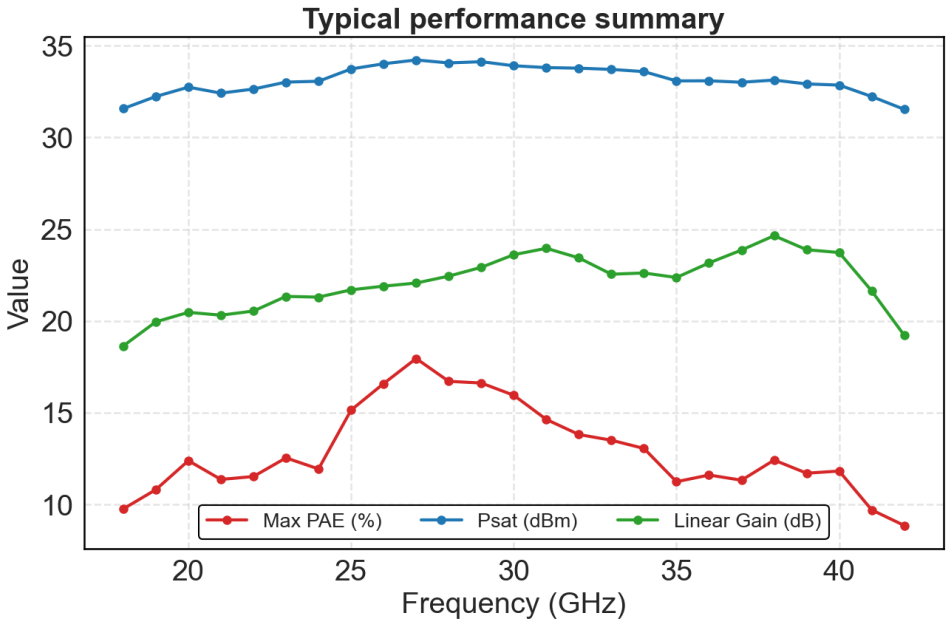
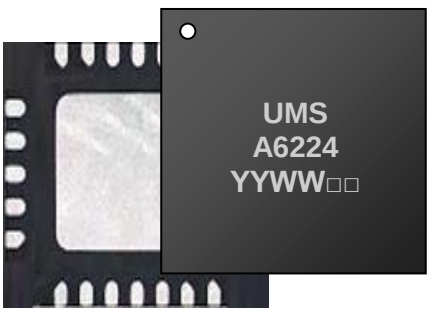
Advanced Information: AI2520

20-40GHz 2W GaN Power Amplifier

GaN Monolithic Microwave IC



CHA6224-QCB is a three-stage wideband power amplifier operating between 20 and 40GHz. The amplifier provides nominal 2W saturated output power and minimum 20dB linear gain. With its compact footprint and excellent RF performance, this amplifier delivers optimized mmWave power solutions to meet the stringent requirements of next-generation Satcom, 5G infrastructure, Test instrumentation and wideband electronic warfare systems. The circuit is manufactured on a robust HEMT GaN-on-SiC process and is available in 5x5 QFN package. Input and Output are 50Ω matched.



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Electrical Characteristics

Tcase = +25°C, Vd = +15V, CW mode (Tcase: Package backside temperature)

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	20		40	GHz
Gain	Linear Gain		21		dB
Pout	Output Power @Pin = 23dBm		33		dBm
PAE	Power Added Efficiency @Pin = 17dBm		11		%
Pdiss	Dissipated power @Pin = 17dBm		14		W
S11	Input Return Loss		-12		dB
S22	Output Return Loss		-10		dB
Idq	Quiescent Drain bias current		560		mA
Vd	Drain voltage			15	V

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Absolute Maximum Ratings (1)

Tcase = +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	19	V
Vg	Gate bias voltage	-7 to -1.5	V
Pin	Maximum peak input power overdrive	27	dBm

(1) Operation of this device above anyone of these parameters may cause permanent damage.

Recommended Operating Range (2), (3)

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	≤15	V
Vg	Gate bias voltage	-5 to -2.3	V
Pin	Maximum peak input power overdrive (2)	+23	dBm
Tj	Maximum Junction temperature	200	°C
Tcase	Operating Temperature Range	-40 to 85	°C
Tstg	Storage Temperature Range	-55 to 150	°C

(2) Electrical performances are defined for specified test conditions

(3) Electrical performances are not guaranteed over all recommended operating conditions

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Typical Bias Conditions

Tcase = +25°C

Symbol	Pad Nº	Parameter	Values	Unit
Vg	9, 11, 13	Gate voltage tuned for Idq~560mA	-2.4	V
Vd	22, 25, 27	Drain Voltage	15	V

“Power ON” sequence

1. Bias HPA gate voltage at Vg close to Vpinch-off (Vg~-5V)
2. Set Vd bias voltage to 0V: Id=0mA
3. Apply Vd bias voltage, Vd = 15V: Id=0mA
4. Increase Vg up to quiescent bias drain current Idq=560mA
5. Apply RF input Power

“Power OFF” sequence

1. Turn off RF input power
2. Bias HPA Gate voltage at Vg~-5V: Id=0mA
3. Decrease Vd bias voltage down to 0V
4. Turn Vg bias voltage to 0V

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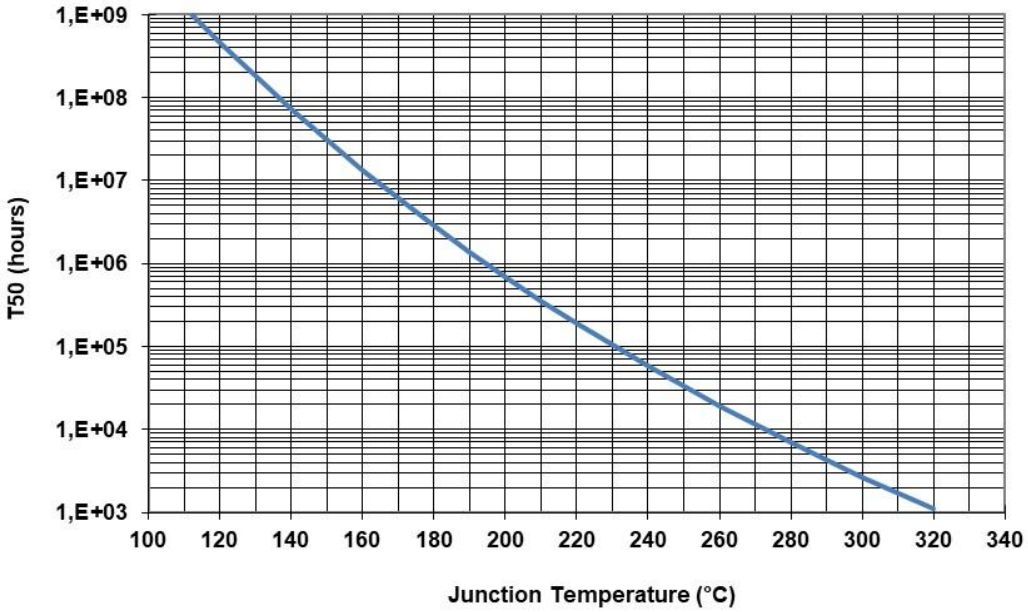
Device Thermal Performance

The device thermal performances below are based on UMS rules to evaluate the junction temperature. All the figures given in this section are obtained assuming that the device is only cooled down by conduction through the thermal pad (no convection mode considered).
The temperature is monitored at the chip back-side interface (Tb).
This same procedure is the basis for junction temperature evaluation of the samples used to derive the Median lifetime and activation energy for the particular technology on which the CHA6224-QCB is manufactured.
The temperature T_{case} is defined as the package backside temperature. The thermal resistance (Rth), given in the following table, is for the full circuit in CW mode.
The system maximum temperature must be adjusted in order to guarantee that $T_{junction}$ remains below the maximum value specified in the Recommended Operating Range table. The system PCB must be designed to comply with this requirement.

Parameter	Conditions	Tjunction (°C)	Rth (°C/W)	T50 (hours)
Rth(1) Thermal Resistance	Vd = 15V Idq = 560mA Pin = 23dBm Dissipated power = 17W	177	5.3	$6.8x10^5$

(1) QFN backside thermal resistance evaluated at Tcase=85°C



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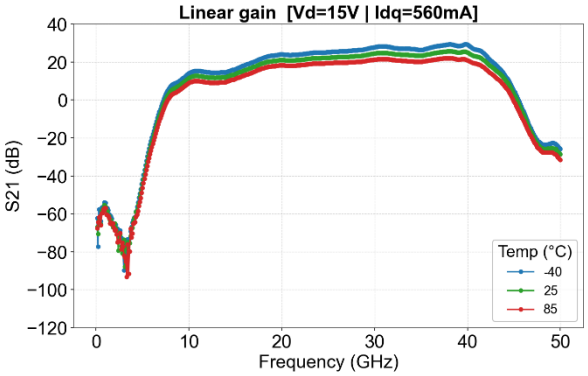
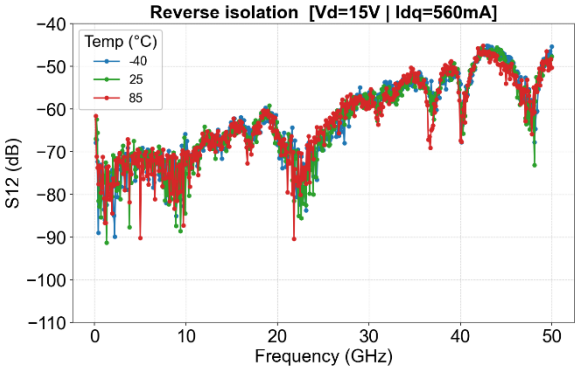
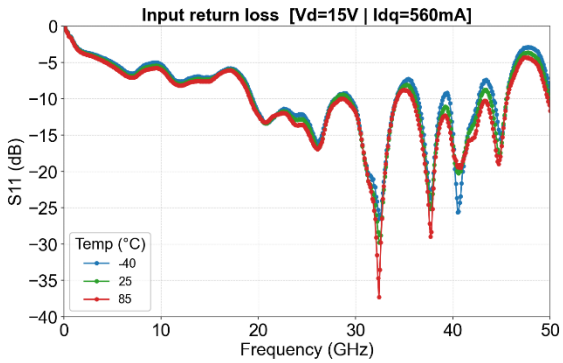
Typical Board Measurements – Small Signal Performance

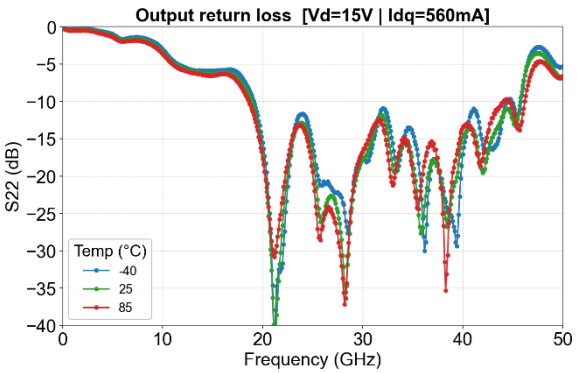
Measurement reference is at the connector plane for S11 and S22, and de-embedded at the package reference planes.

Wide-band S-Parameters versus Frequency and Temperature
Test conditions: Vd = 15V, Idq = 560mA, Tcase = -40°C/25°C/85°C









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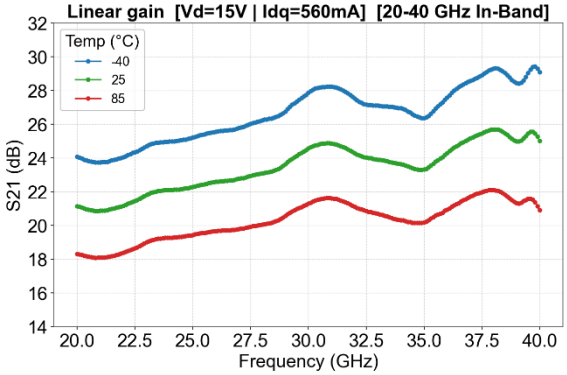
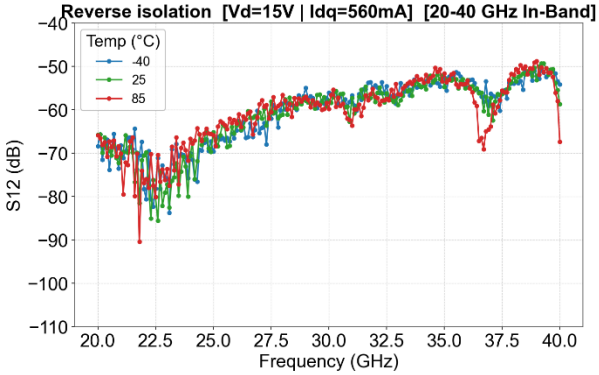
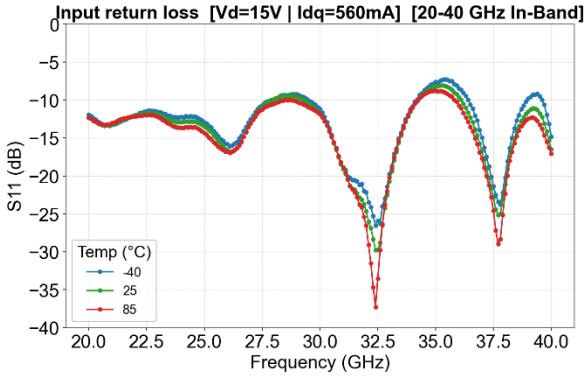
Typical Board Measurements – Small Signal Performance

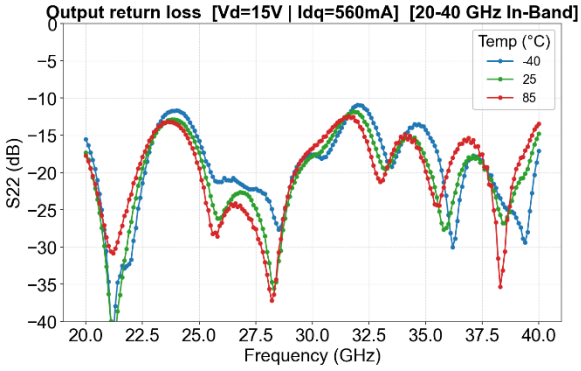
Measurement reference is at the connector plane for S11 and S22, and de-embedded at the package reference planes.

Narrow-band S-Parameters versus Frequency and Temperature
Test conditions: Vd = 15V, Idq = 560mA, Tc = -40°C/25°C/85°C









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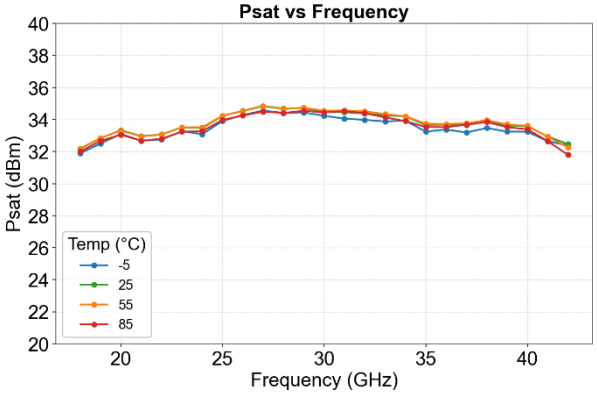
Typical Board Measurements – Large Signal Performance

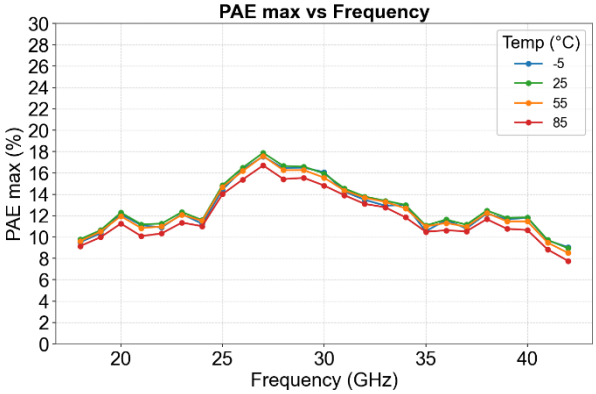
Test conditions: Vd = 15V, Idq = 560mA, Tcase = -5°C/25°C/55°C/85°C

Measurement reference plane is de-embedded at the package reference planes.

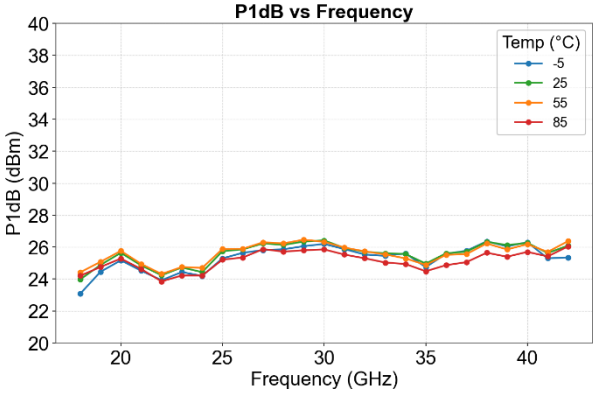
Pout vs Frequency at Pin = 23 dBm



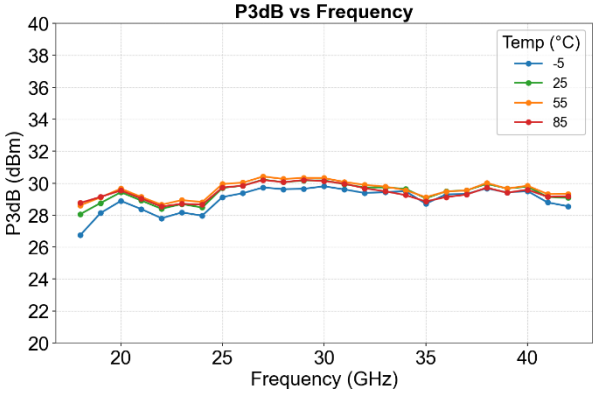
PAE vs Frequency at Pin = 17 dBm for all temperature values



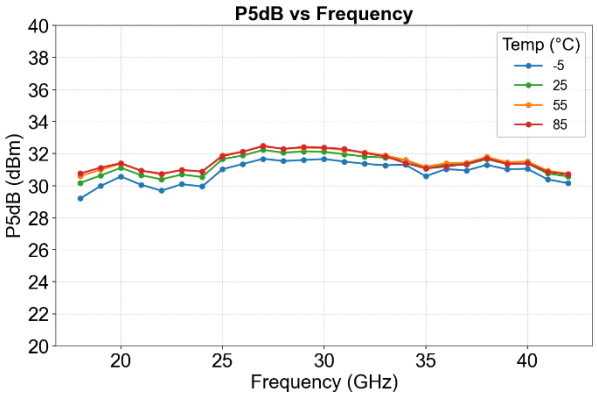
1-dB Compression Output Power



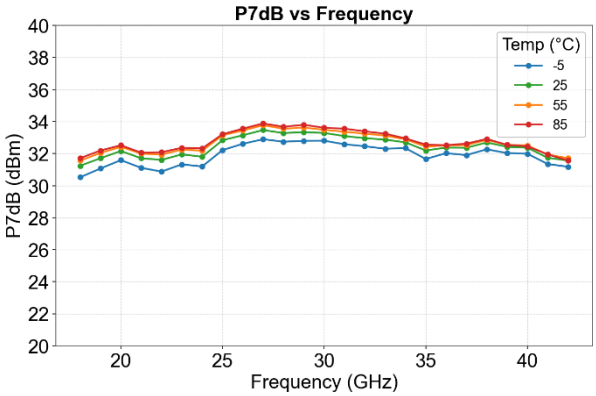
3-dB Compression Output Power



5-dB Compression Output Power



7-dB Compression Output Power



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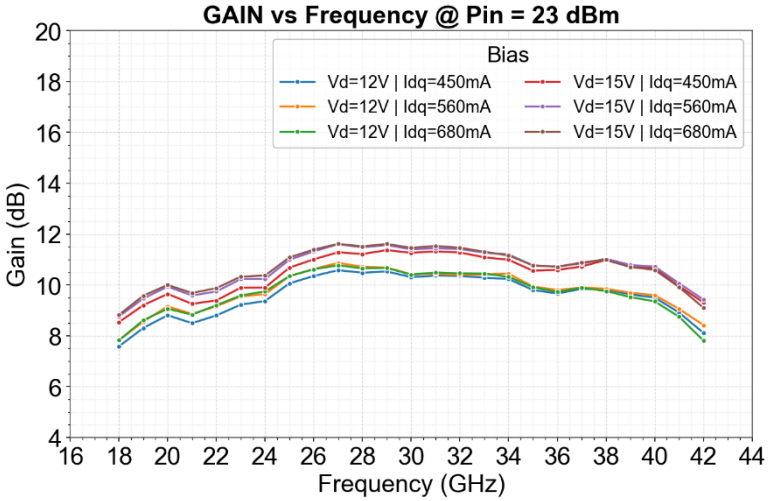
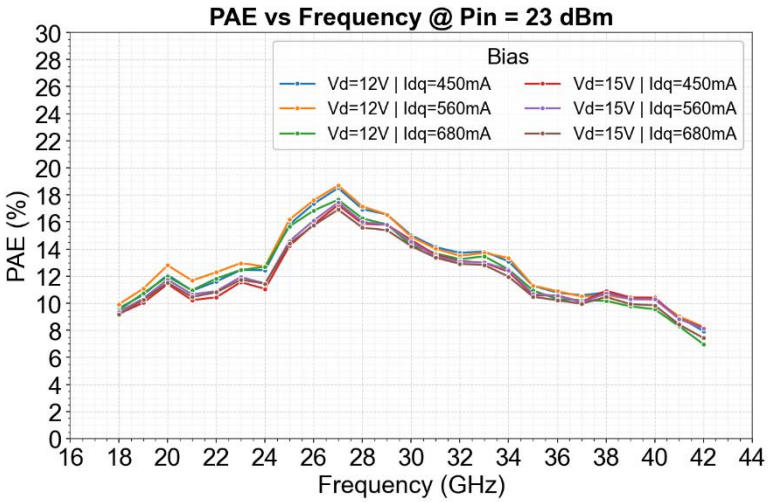
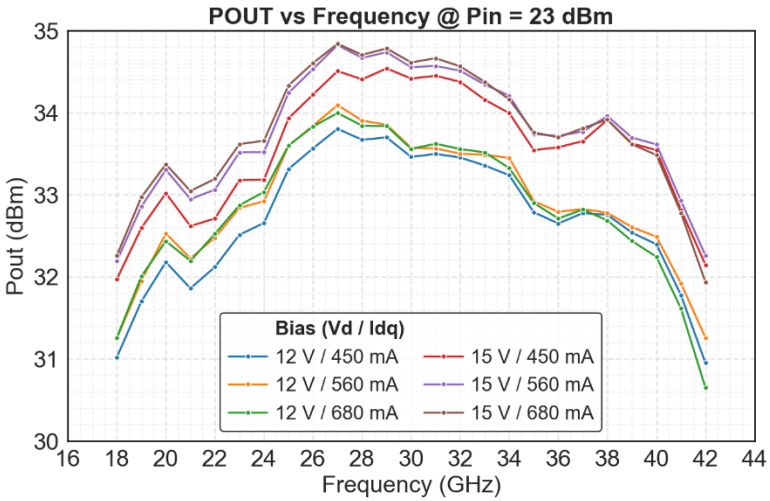
Typical Board Measurements – Large Signal Performance

Test conditions: Tcase = 25°C, Pin = 23 dBm with different bias sets
Vd = [12; 15V] and Idq = [450; 560; 680mA]

Measurement reference plane is de-embedded at the package reference planes.







Advanced Information

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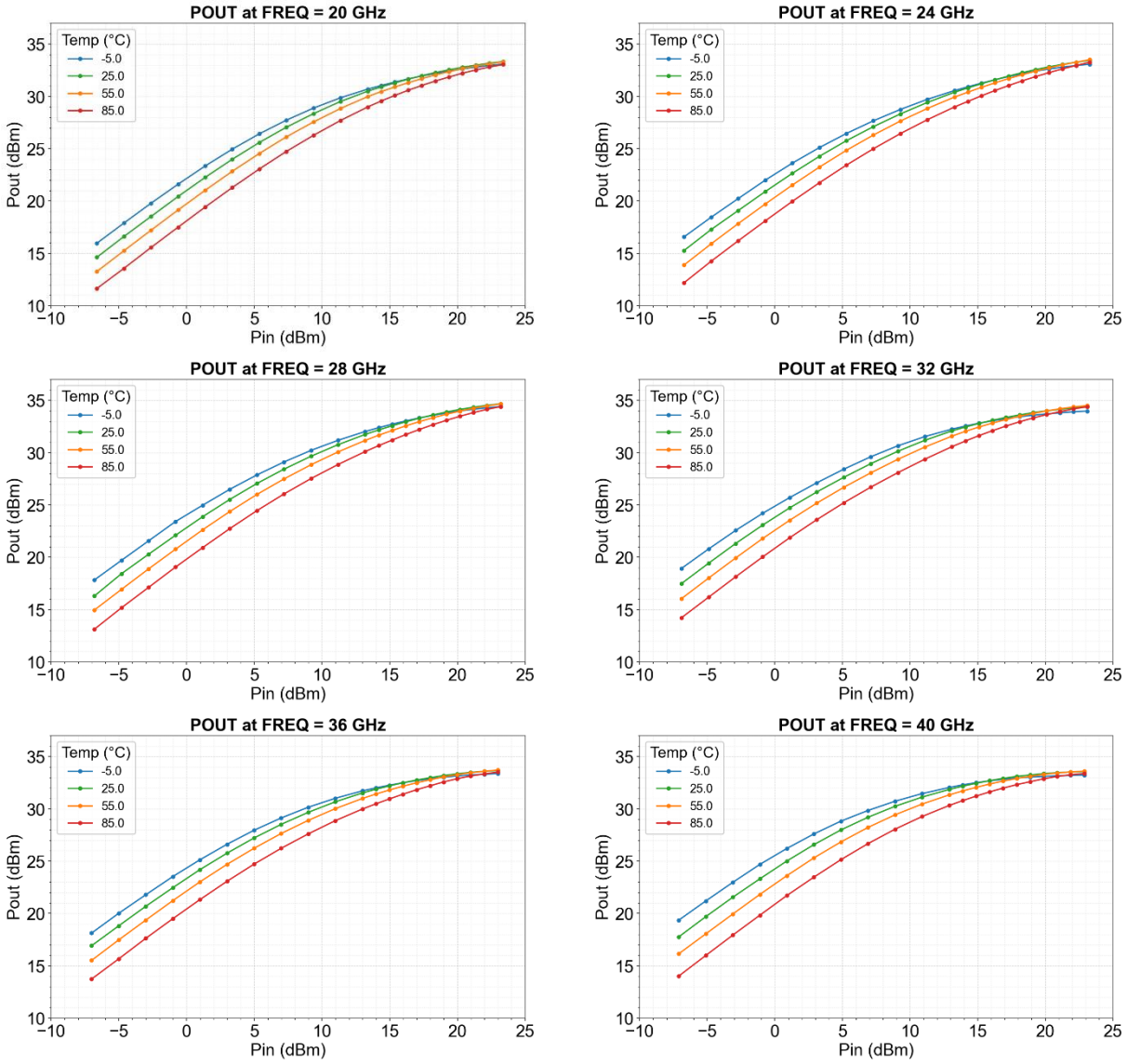
Typical Board Measurements – Large Signal Performance

Test conditions: Vd = 15V, Idq = 560mA, Tcase = -5°C/25°C/55°C/85°C

Measurement reference plane is de-embedded at the package reference planes.

Output power versus Input power per Frequency



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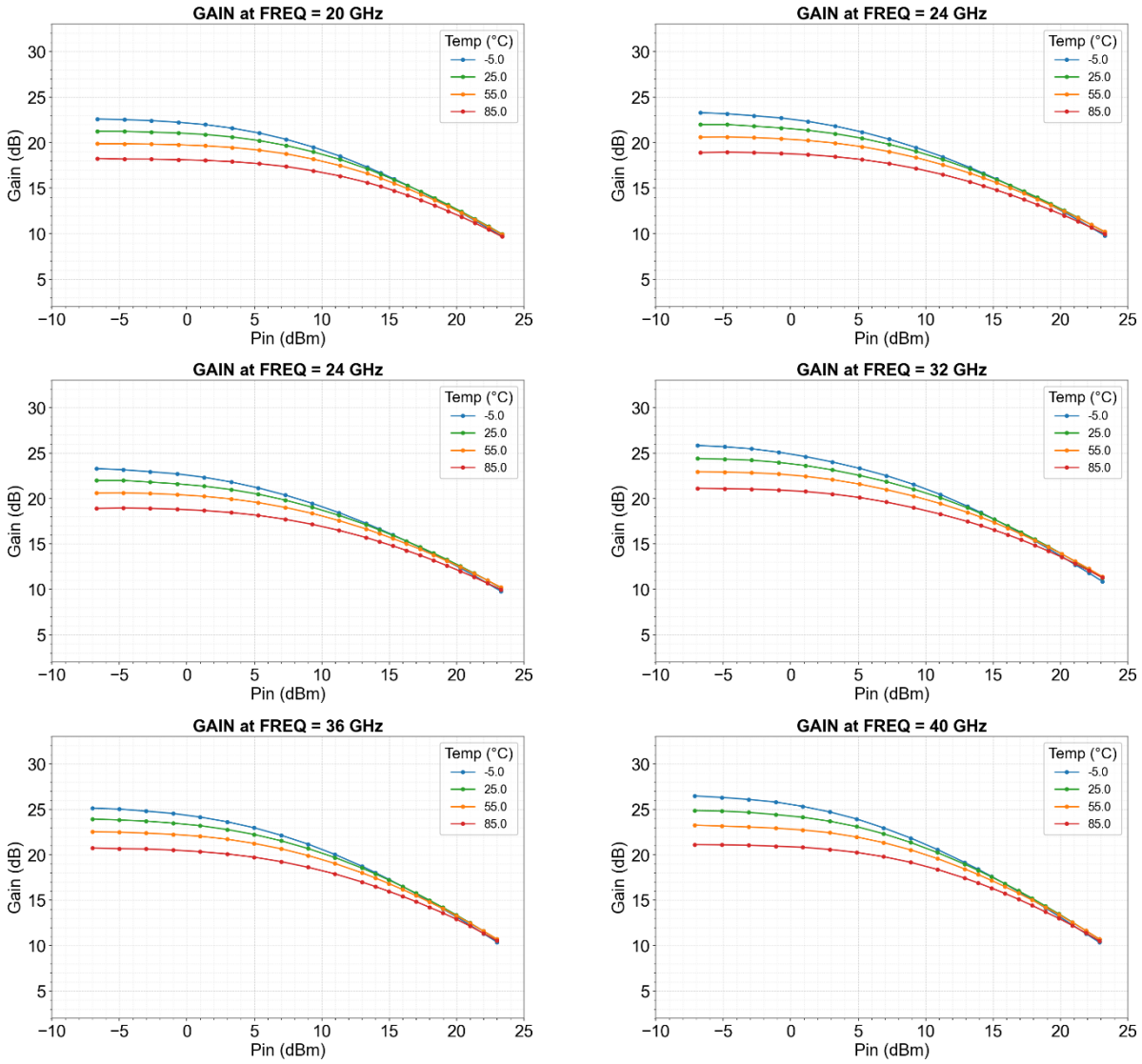
Typical Board Measurements – Large Signal Performance

Test conditions: Vd = 15V, Idq = 560mA, Tcase = -5°C/25°C/55°C/85°C

Measurement reference plane is de-embedded at the package reference planes.

Gain versus input power per Frequency



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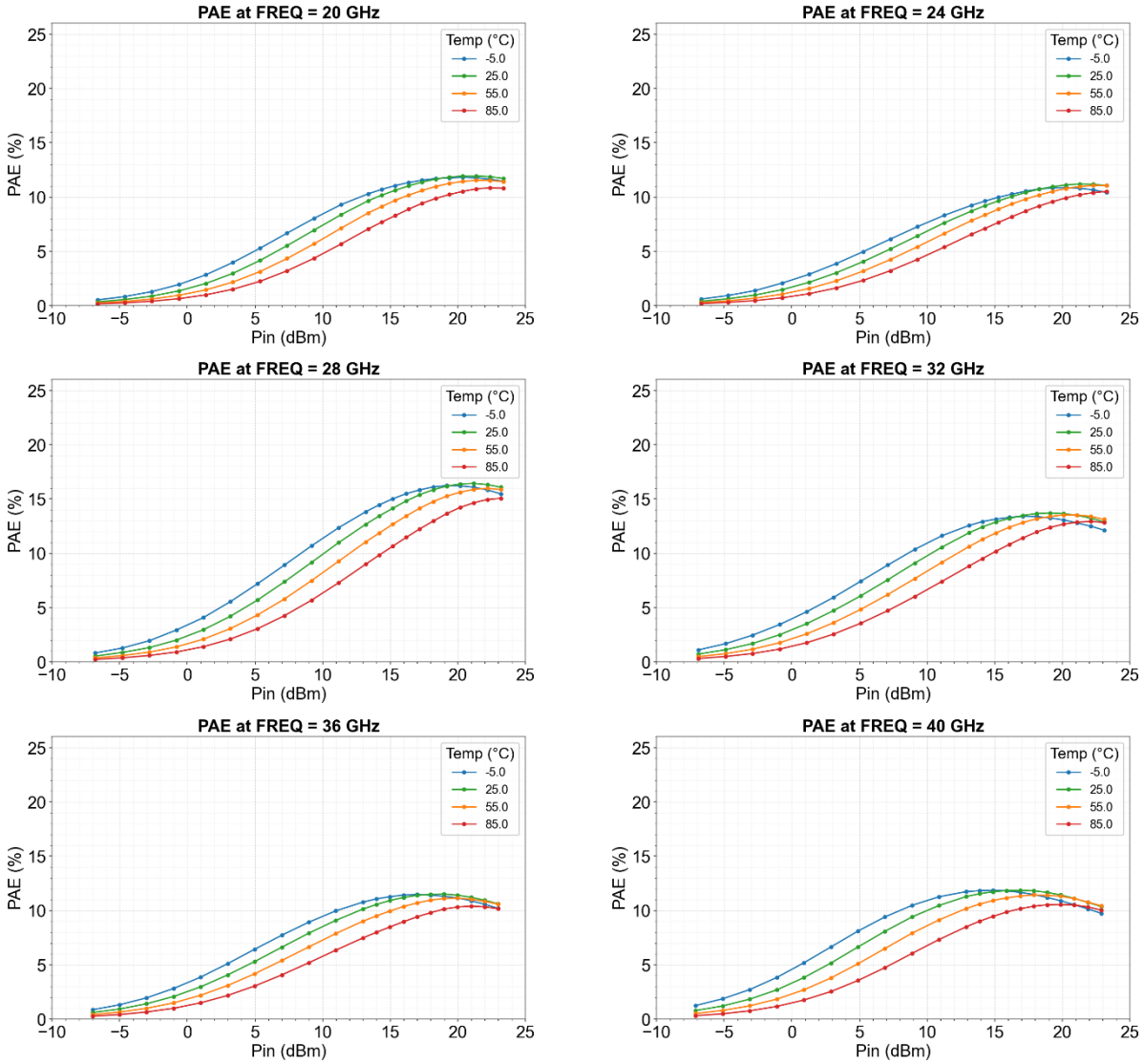
Typical Board Measurements – Large Signal Performance

Test conditions: Vd = 15V, Idq = 560mA, Tcase = -5°C/25°C/55°C/85°C

Measurement reference plane is de-embedded at the package reference planes.

PAE versus input power per Frequency



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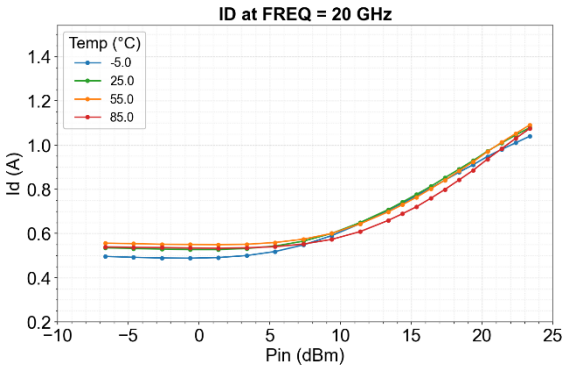
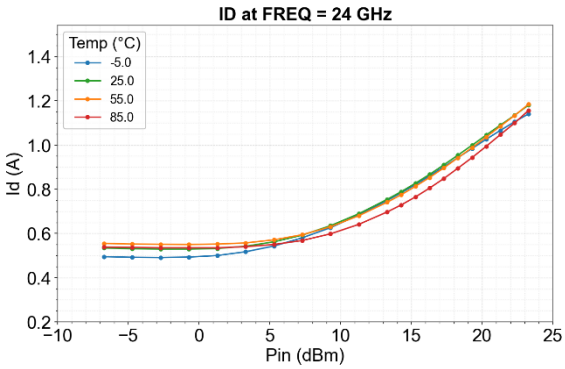
Typical Board Measurements – Large Signal Performance

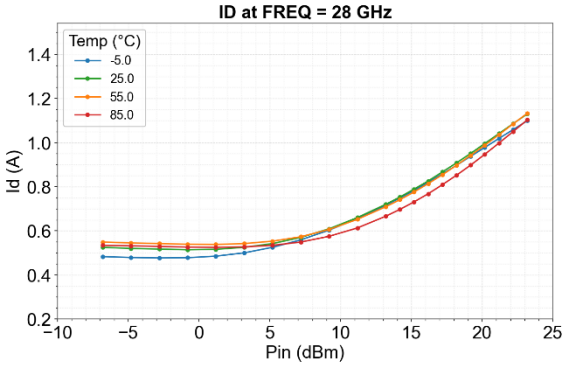
Test conditions: Vd = 15V, Idq = 560mA, Tcase = -5°C/25°C/55°C/85°C

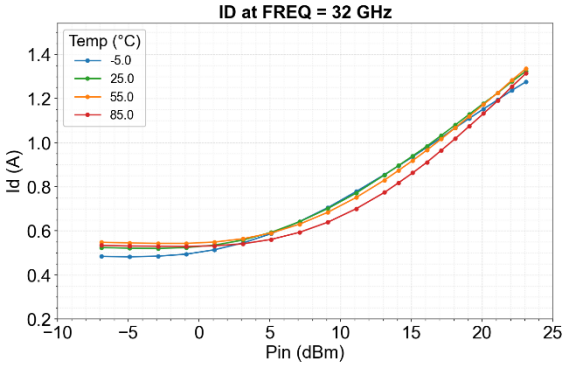
Measurement reference plane is de-embedded at the package reference planes.

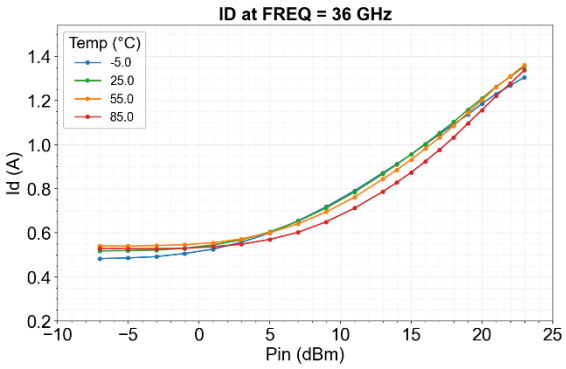
Drain current versus input power per Frequency

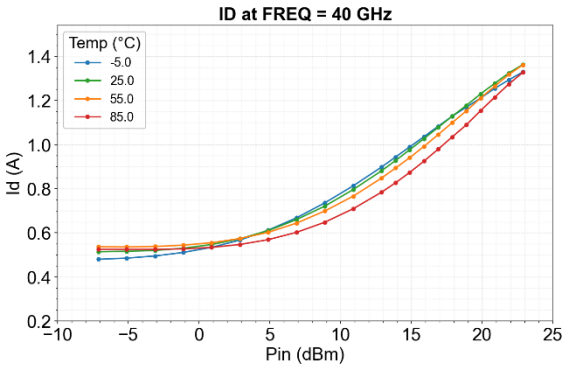












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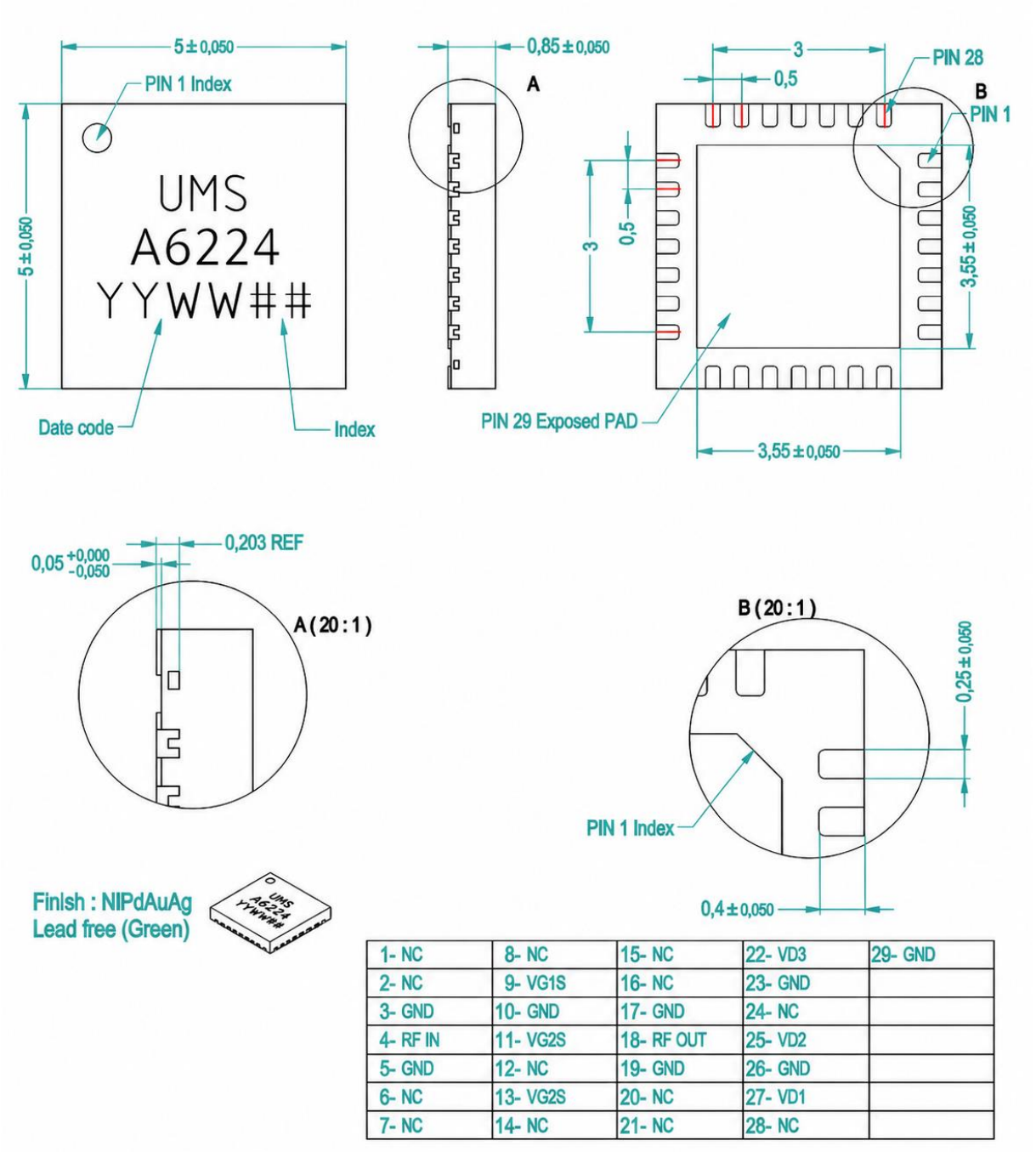
Package outline (1)



1- NC	8- NC	15- NC	22- VD3	29- GND
2- NC	9- VG1S	16- NC	23- GND	
3- GND	10- GND	17- GND	24- NC	
4- RF IN	11- VG2S	18- RF OUT	25- VD2	
5- GND	12- NC	19- GND	26- GND	
6- NC	13- VG2S	20- NC	27- VD1	
7- NC	14- NC	21- NC	28- NC	

(1) Refer to the application note AN0017 (https://www.ums-rf.com) for general consideration and recommendations for Molded Plastic QFN/DFN packages.

(2) It is strongly recommended to ground all pins marked “GND” through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

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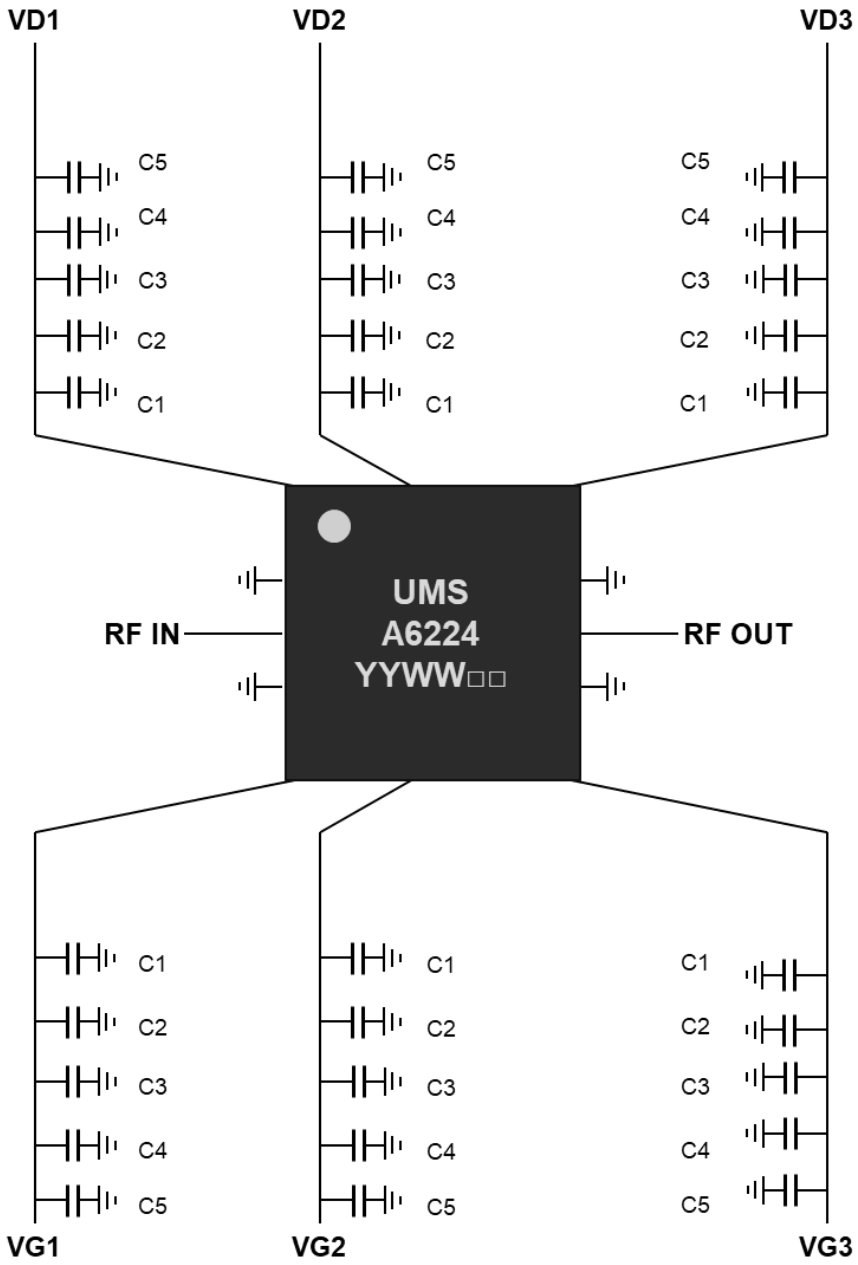
Recommended Assembly Plan



Note : Drain (VD's) biased from the north side.and Gate (VG's) biased from the south side

Bill of Materials

Component	Value	Description
C1	100pF	CAP, 100pF, ±10%, 50V, 0402
C2	1nF	CAP, 1nF, ±10%, 50V, 0402
C3	10nF	CAP, 10nF, ±10%, 50V, 0402
C4	100nF	CAP, 100nF, ±10%, 50V, 0402
C5	1µF	CAP, 1µF, ±10%, 50V, 0805

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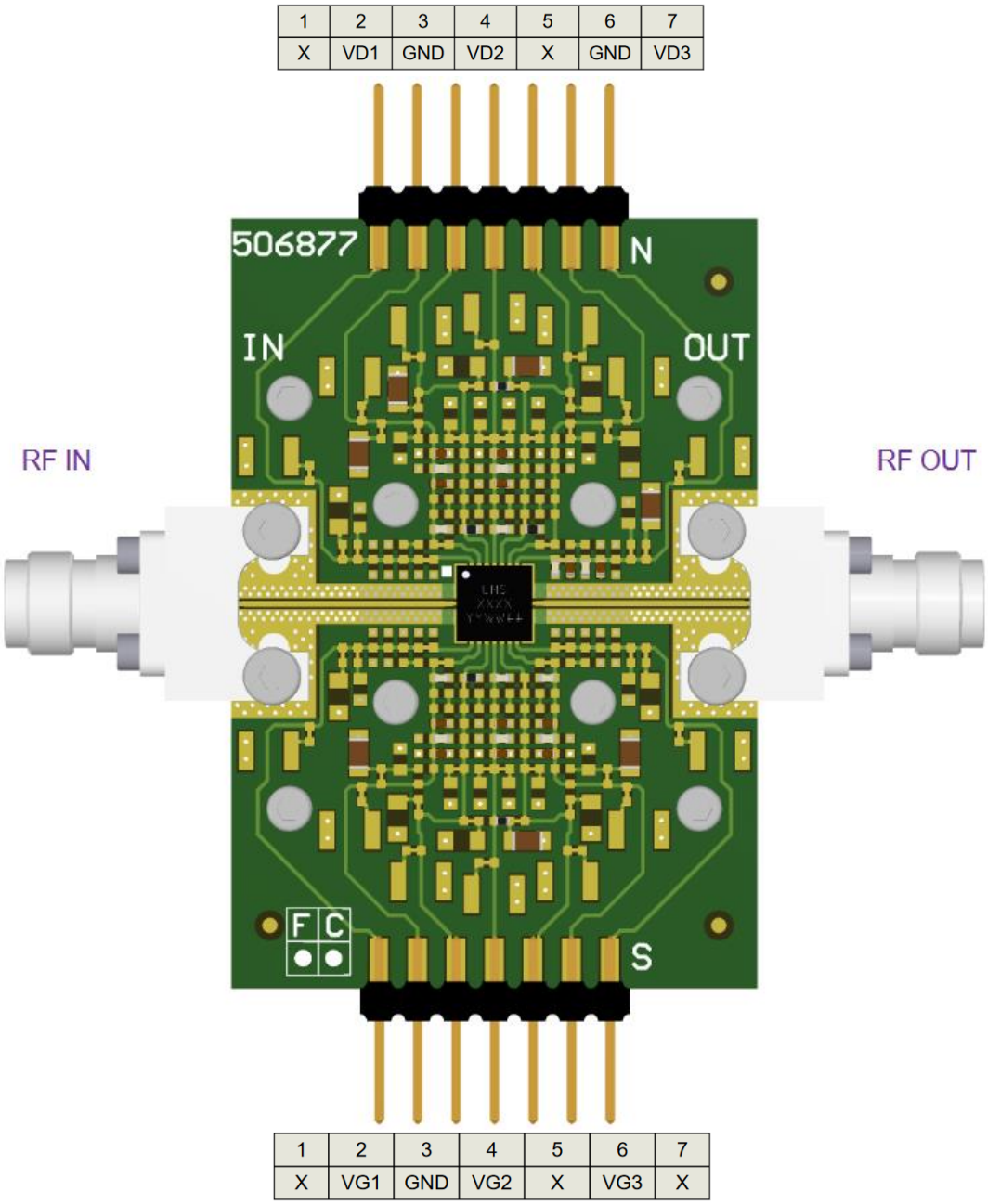
Evaluation Board (EVB)

- Compatible with the proposed footprint.
- Based on 10mils RT6035HTC or equivalent.
- Recommended for the implementation of this product on a module board.
- See application note AN0031 for details.



Note: All board measurements are performed using **shielded cables**, even for DC bias, to ensure safe operation.

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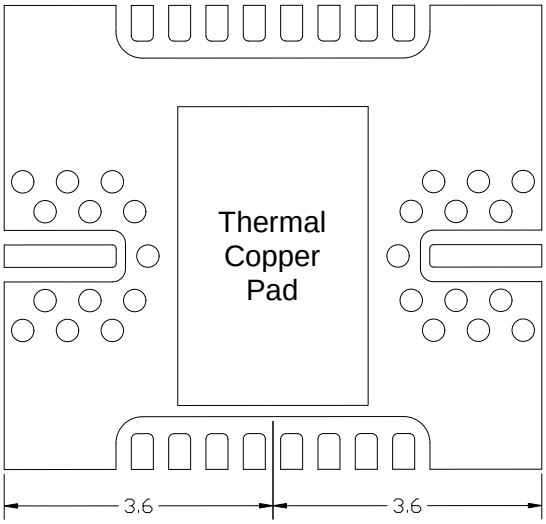
Measurement Reference Planes

The measurements reference planes are symmetrical from the symmetrical axis of the package as defined on the drawing beside. The input and output reference planes are located at 3.6mm offset (input wise and output wise respectively) from this axis.



ESD Sensitivity

Parameter	Classification	Standard
Human Body Model (HBM)	1A	ANSI/ESDA/JEDEC JS-001

Package Information

Parameter	Value
Package body material	RoHS-compliant
	Low stress Injection Molded Plastic
Lead finish	100% Ni-Pd-Au-Ag
MSL Rating	MSL3

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Notes

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SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017 available at http://www.ums-rf.com.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at http://www.ums-rf.com.

Recommended ESD management

Refer to the application note AN0020 available at http://www.ums-rf.com for ESD sensitivity and handling recommendations for the UMS package products.

Description of Evaluation Board

Refer to the application note AN0031 available at https://www.ums-rf.com for the description of Evaluation Board for Packaged Die and recommendations for this UMS package product.

Maturity Level

Maturity Level	Product status	Documentation	Reliability	Usage in a system
Lab Sample (LS)	Decision to develop the product is not confirmed	Technical Information	No commitment	Lab demonstrator
Engineering Sample (ES)	**Design may change**	**Advanced Information**	**The design is within the recommended temperature, current and voltage ranges as regards the technology used.**	**Engineering demonstrator**
Product Representative Unit (PRU)	Design is frozen	Data-sheet	Tests results are available on the foreseen product or on an similar one	Production

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Sampling request reference

Package:	ES-CHA6224-QCB
Evaluation board:	EVB-CHA6224-QCB

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