

# Seamless Heterointegration of Components: Advancements in Fanout Technology and Thermal Solutions in System in Package

Robert Gernhardt  
Fraunhofer Institute for Reliability and  
Microintegration IZM  
Berlin, Germany  
robert.gernhardt@izm.fraunhofer.de

Marius Adler  
Fraunhofer Institute for Reliability and  
Microintegration IZM  
Berlin, Germany  
marius.adler@izm.fraunhofer.de

Tanja Braun  
Fraunhofer Institute for Reliability and  
Microintegration IZM  
Berlin, Germany  
tanja.braun@izm.fraunhofer.de

Markus Wöhrmann  
Fraunhofer Institute for Reliability and  
Microintegration IZM  
Berlin, Germany  
markus.woehrmann@izm.fraunhofer.de

Benoit Lambert  
United Monolithic Semiconductors  
S.A.S.  
Villebon-sur-Yvette, France  
Benoit.Lambert@ums-rf.com

Jesse Riedl  
United Monolithic Semiconductors  
S.A.S.  
Villebon-sur-Yvette, France  
Jesse.Riedl@ums-rf.com

Ulrike Ganesh  
Technische Universität Berlin  
Berlin, Germany  
ulrike.ganesh@tu-berlin.de

Martin Schneider-Ramelow  
Technische Universität Berlin  
Berlin, Germany  
martin.schneider-ramelow@tu-berlin.de

**Abstract**—The advent of fan-out technology has revolutionized the integration of various chip front-end technologies within a single package, offering significant advantages in performance and efficiency. By enabling a more compact design and improved signal integrity, fan-out technology facilitates the seamless interconnection of diverse semiconductor components, particularly within System-in-Package (SiP) architectures. This paper explores the benefits of fan-out technology, with a particular focus on approaches for enhanced thermal management, reduced form factor, and increased functionality through the integration of antenna structures. Furthermore, its pivotal role in the heterogeneous integration and the associated reliability aspects within SiP solutions is discussed, thereby paving the way for advanced applications in the rapidly evolving landscape of electronics.

**Keywords**— FOWLP, Heterointegration; System-in-Package; III-V semiconductor, RF applications

## I. INTRODUCTION

Fan-out technology, whether wafer- [1] or panel-based [2], has become a common and largely mature technology with a wide range of variants. While many of these variants focus on the packaging of a single die, one of the major advantages of this technology is its inherent ability to integrate different dies from various front-end technologies (and vendors) into a single package in the form of a SiP. The electrical connection between the embedded dies is facilitated by Redistribution Layers (RDLs), which offer optimal signal integration with the shortest interconnection lengths and improved signal integrity compared to former integration technologies such as wire bonding. The advantages of this approach are particularly relevant and beneficial in high-frequency applications and in the integration of III/V semiconductors. A significant challenge confronting this domain is - in addition to the handling structural characteristics of III/V semiconductors, such as the use of mainly gold for metallization, that they are much thinner and, by that, more fragile compared to silicon

chips, and the presence of air bridges - the development of effective and robust thermal management solutions that can be applied consistently across different device types. The present document therefore concentrates on the technical approaches for the thermal management of embedded III/V semiconductors and on the validation of Fan-Out Wafer-Level Packaging (FOWLP) technology for RF applications.

## II. METHODOLOGY AND TECHNOLOGY

In order to validate the technology and to assess its reliability in a systematic and application-oriented manner, United Monolithic Semiconductors (UMS) designed various test vehicles, including simple test structures such as daisy-chain build-ups as well as real application demonstrators. These demonstrators include, among others, a Ka-band transceiver with a GaN and a GaAs die in one FOWLP, an E-band low-noise amplifier (LNA), a V-band high-power amplifier (HPA), and a transceiver for airborne radar with a GaN and a SiGe die integrated within a single FOWLP. Furthermore, UMS provided the chips intended for embedding, with a part of these chips being specially manufactured by UMS for this purpose to ensure compatibility with the embedding process and to allow specific process experiments. The FOWLPs are realized with the chip-first RDL-last approach. In this process, the chips are first assembled onto a carrier with thermal release tape (TRT), compression molded in epoxy molding compound (EMC), and subsequently released from the thermal release tape to create a reconstructed wafer on which the dies are connected by RDL. After the finalization of the RDL, the wafers are grinded to the final package thickness and optionally provided with a backside metallization. Subsequent to this, the balls are placed, and the wafers are separated into individual SiPs through wafer dicing. The process flow can be seen in Figure 1. The heat dissipation, especially for RF ICs in FOWLP, is critical because the die is embedded in epoxy molding compound, which has a comparatively low thermal

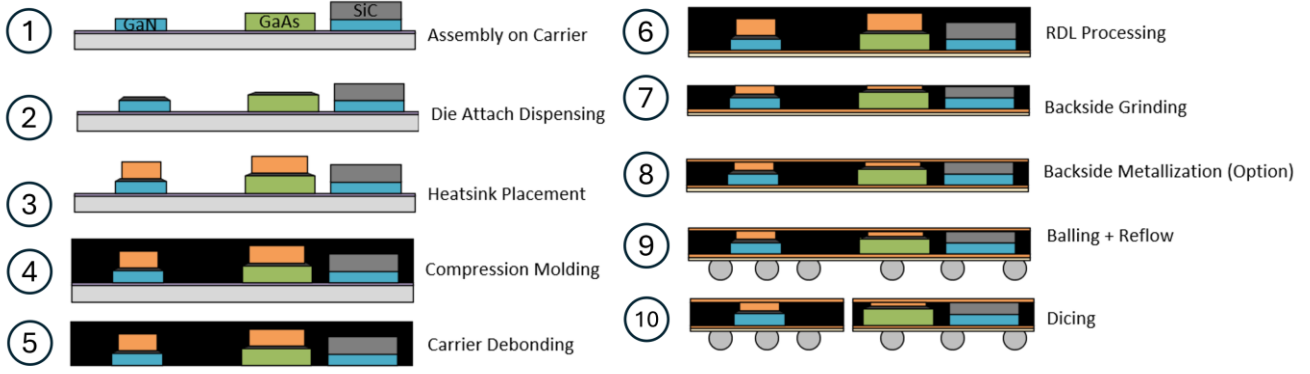


Figure 1: process flow of the fanout packages with integrated heat transfer element

conductivity. In certain configurations, the FOWLP can be grinded to a thickness at which the embedded chip backside is revealed, thus allowing direct access for heat dissipation. However, this is sometimes either not desired or not feasible due to overall thickness limitations and/or various embedded die thicknesses in more complex SiP configurations. The novel approach to improving heat transfer to the back of the package involves integrating heat transfer elements individually onto the back of the embedded dies before compression molding (unlike other methods [3],[4]). The design and implementation of these elements is described in detail in the next section. In order to expose the heat transfer element and to enable access to it for thermal coupling, the wafers are grinded from the backside after RDL completion. Subsequently, the backside of a part of the test vehicles is additionally covered with a backside metallization stack of 5  $\mu\text{m}$  Cu, 5  $\mu\text{m}$  Ni, and 0.2  $\mu\text{m}$  Au to realize a larger and more uniform interface for the thermal contact to the cooling system. An analysis was conducted to assess the impact of these measures on reliability.

The build-up of all created test vehicles has been analyzed by Fraunhofer IZM and UMS using optical inspection, cross-sectioning, X-ray inspection, and scanning acoustic microscopy (C-SAM). The subsequent reliability tests were conducted by UMS. Depending on the test vehicle configuration, these tests included high-temperature storage live (HSTL; 1000 h; 150  $^{\circ}\text{C}$ ), temperature humidity bias (THB; 1000 h; 85  $^{\circ}\text{C}$ ; 85 % rel. humidity), radio-frequency life test (RFTL; 2000 h), moisture sensitivity level MSL3 (168 h; 30  $^{\circ}\text{C}$ ; 60 % rel. humidity), thermal cycling (TC), and thermal cycling on board (TCoB; >1000 cycles; -55/125  $^{\circ}\text{C}$ ). This comprehensive methodology ensured that both initial manufacturing quality and long-term reliability under representative stress conditions were evaluated.

### III. HEAT TRANSFER ELEMENT INTEGRATION AND FACE-UP APPROACHES FOR HEAT DISSIPATION

Before the actual molding process of the chips starts, two kinds of heat transfer elements are mounted on the backside of the chips, depending on chosen approach. In the first approach, a block of metal is glued onto the chip backside after the assembly of the chips on the thermal release tape and before the actual molding process. In the second approach, the chips to be embedded are already provided with the heat transfer element, which is done in advance in a wafer-bonding process directly after the finalization of the initial device wafer from which the chips originate. The heat transfer elements

were revealed by grinding of the wafer backside after the finalization of the RDL on the wafer front side. In a third approach, the integration of the embedded die was flipped to a face-up configuration, and solder balls were placed directly on the chip backside (with an under-bump metallization, UBM, in between) to enable a better and more direct path for heat dissipation through the bumps in contrast to the other approaches in which the balls are located over the RDL and do not have direct contact with the embedded die.

#### A. Assembled Heat Transfer Element

In the assembled heat transfer element approach, the chips to be embedded are first assembled on the thermal release tape. Subsequently, a die-attach adhesive is dispensed onto the chip backside, and the heat transfer element, in the form of a block of copper-molybdenum (CuMo), is glued on top of the chip. The curing process of the die-attach adhesive is performed in a two-stage manner. The initial part of the curing already starts after dispensing. The final curing step occurs during the subsequent molding process. Copper-molybdenum (CuMo) was chosen as heat transfer element material because it is available as sheet material in the thicknesses needed for the compression molding with sufficient quality, and because its coefficient of thermal expansion (CTE) is a good compromise between the CTEs of the EMC and the embedded dies. A design of experiment (DoE) was performed to determine the best size for the heat transfer element and the optimal amount of adhesive (Figure 2). The goal was to achieve robust and reliable full coverage of either the backside of the embedded chip or the surface of the heat transfer element while avoiding process-induced side effects. Using heat transfer elements that are larger than or equivalent in size

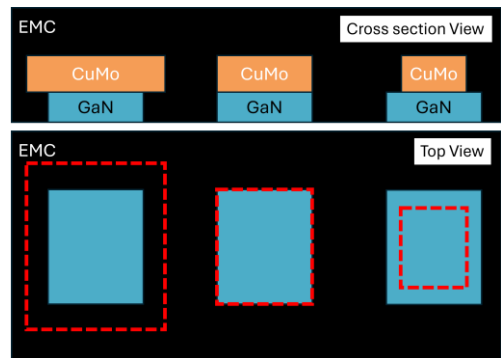


Figure 2: schematic cross section (top) and front side view (bottom) of the DoE

to the embedded die proved counterproductive. This configuration resulted in the adhesive migrating to the front side of the wafer and in an interaction with the TRT tape, which led to TRT residues after de-bonding. Furthermore, subsequent RDL processing was adversely affected at these locations, resulting in wetting issues during coating of the first polyimide (PI) layer. This migrating effect is a result of the surface tension of the adhesive, which wets also the side walls of the chips and forms a meniscus between the heat transfer element and the chip. Is the amount of the die-attach adhesive large enough, it can reach the TRT tape. Even without the migration effect of the adhesive, the EMC surface in the area of an overlapping heat transfer element showed high roughness due to protruding filler particles of the EMC (see Figure 3), which again interfered with uniform thin-film coating. It was determined that a 100  $\mu\text{m}$  recess towards the chip edge is sufficient to prevent adhesive migration and to avoid the aforementioned issues, while still maintaining

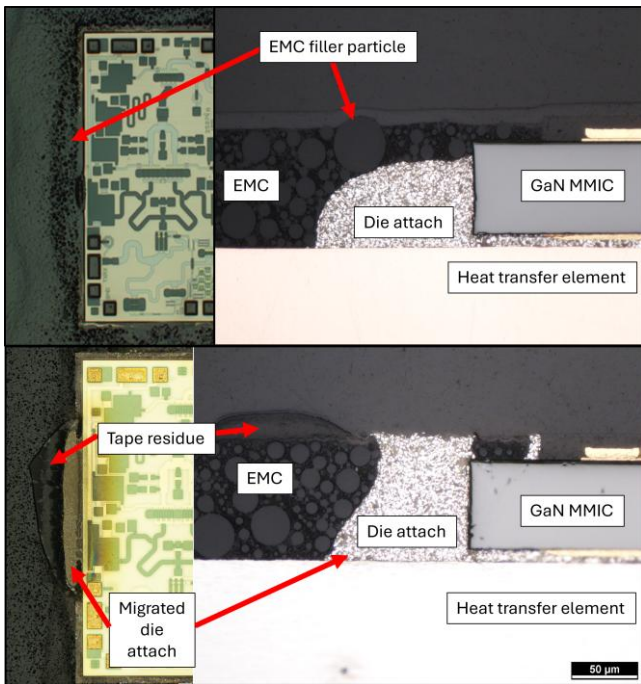


Figure 3: protruding filler particle (top); migrated die-attach (bottom)

efficient thermal coupling between the die and the heat transfer element.

### B. Wafer Bonded Heat Transfer Element

The assembled heat transfer element approach has several advantages, such as lower process costs and broad compatibility with different types of chips, which do not need to be specially prepared before the embedding process. In parallel, the approach is not without its drawbacks. The process is serial in nature, occurring subsequent to the assembly stage of the embedding procedure. This characteristic presents a cost disadvantage for high-throughput manufacturing. In addition, a significant number of III/V semiconductors have gold metallization on the backside, which can compromise the adhesion of polymers such as the die-attach adhesive utilized in this study. The specific die-attach used has – due to the presence of metal filler particles – a thermal conductivity that is suitable for a limited temperature range. To achieve a better thermal conductivity, to simplify the embedding process, and reduce

the difference in CTE between the chip and the heat transfer element, the wafer-bonded heat transfer element was developed. The schematic process flow is shown in Figure 4. For the realization of this element, access to the front-end device wafer is needed before the singulation. A wafer with

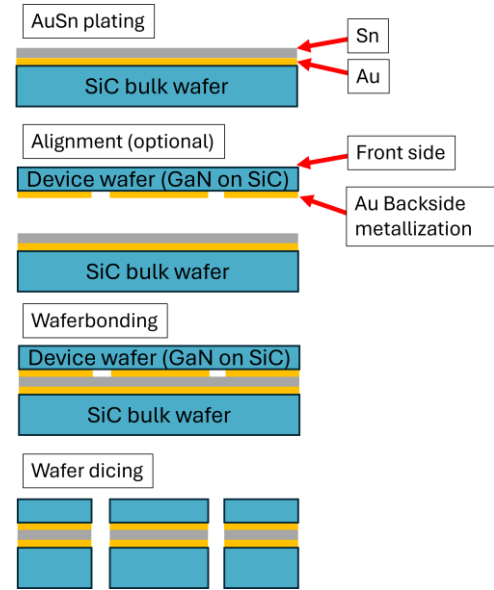


Figure 4: process flow wafer-bonded heat transfer element

the same bulk material and CTE as the device wafer – silicon carbide (SiC) in this study – was bonded to the device wafer using a solder metal layer. The solder alloy of choice was AuSn due to its compatibility with the gold metallization on the backside of the device wafers and due to the thermal-mechanical characteristics of the alloy. AuSn was plated on the heat transfer element wafer with a specific proportion of Au and Sn to achieve – together with the amount of Au on the device wafer – a specific eutectic phase that is formed under the temperature and pressure conditions of the wafer-bonding process. The plating was done both non-structured and structured. In the structured version, the dicing streets were kept free from any metal. This was implemented because it could not be guaranteed that dicing through the alloy would be successful and possible without contamination of the device wafer front side or the chip itself. The backside of the device wafer is anyway structured to keep the dicing streets

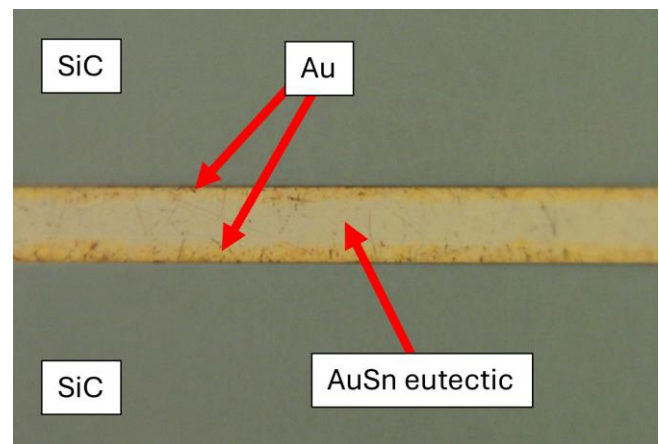


Figure 5: cross section of the bond interface

free of metal (standard foundry process). The bonding of the structured wafer was more complex because precise alignment is needed to match the metal-free streets. Both versions, however, worked well without any voids in the bond interface and were able to be diced without issues. The bond interface was checked locally by cross-sections (Figure 5) and over the entire wafer via X-ray inspection. Based on these results, the non-structured version is preferred, as the lithography step for masking the plating is not needed and the bonding is simplified, given that no alignment is required. A cross-section of one demonstrator (transceiver Ka band) can be seen in the bottom part of Figure 6. In this package, the GaAs die is equipped with an assembled heat transfer element and – within the same package – the GaN die with a wafer-bonded heat transfer element. The slight protrusion of the

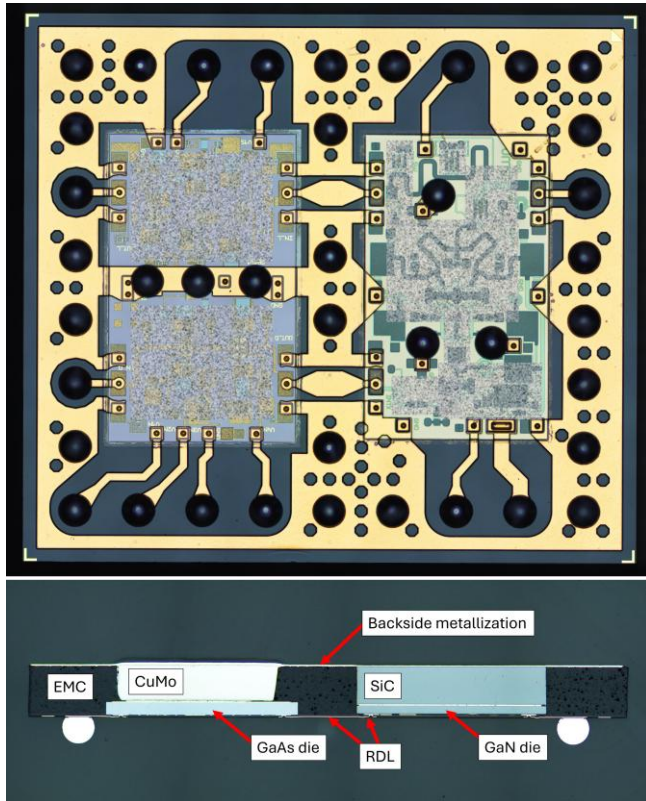


Figure 6: front side (top) and cross section (bottom) view of the FOWLP with assembled and wafer-bonded heat transfer element

CuMo heat transfer element is a result of the cross-section preparation and was not present on the final packages.

### C. Face-Up Integration Approach

For one demonstrator with an embedded GaAs die, another integration approach was possible. The signals of the GaAs die were routed to the backside of the die by so-called hot vias. These are vias through the GaAs substrate routing signals from the front to the backside. This enables the embedding of the die face-up, with the chip front side facing into the EMC and connecting the die via RDL from the backside. Additionally, thermal and electrical bumps could be placed directly on the chip backside with barely any polyimide (which has low thermal conductivity) of the RDL in between, thereby achieving a better thermal contact and shorter thermal path. The benefit of the RDL with polyimide to act as a stress buffer is not present in this configuration, which needs to be considered in the mechanical design. However, routing the

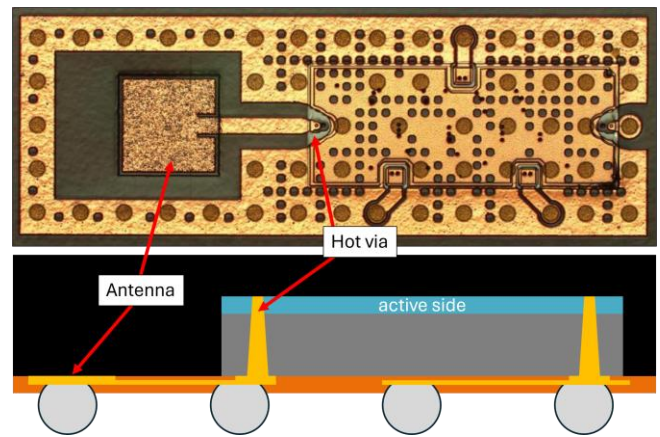


Figure 7: image of the RDL (top) and schematic cross section (bottom) of the AiP

signal to the backside of the die, respectively to the backside of the package, allows the integration of a patch antenna in the RDL layer, and this was realized offside the area of the embedded die (Figure 7). Depending on their design, antennas mainly radiate in one direction. However, some power is always emitted in the opposite direction, as shown the upper left image of Figure 10. Placing the patch antenna offside the die area, the surrounding shielding in the RDL, and the vertical distance to the active side of the embedded die with the EMC in between enable a good electromagnetic isolation between the antenna and the active side of the embedded die. This improves the electromagnetic compatibility (EMC) of the package and avoids electromagnetic interference (EMI) with other devices. All of this was realized with only one RDL layer and without additional shielding layers or other measures like through mold vias [5].

## IV. RESULTS

All test vehicles were manufactured successfully according to the described processes. The investigations (optical inspection, X-ray inspection, electrical tests, and CSAM) and the reliability tests that had been initially planned were subsequently completed as scheduled. All RF and

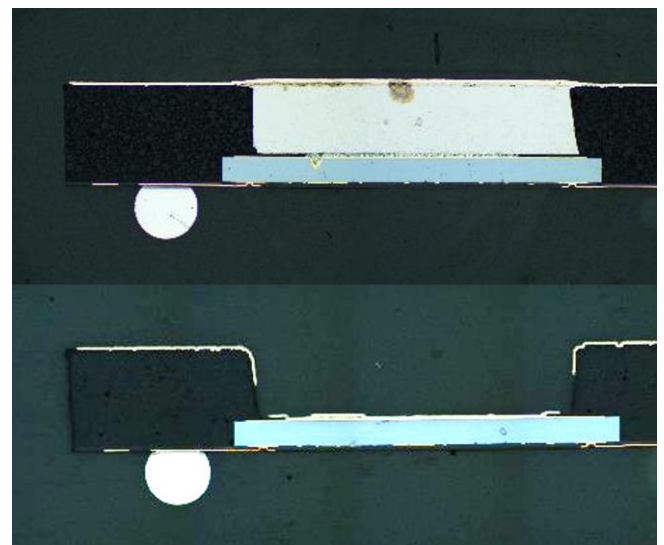


Figure 8: cross sections of a FOWLP with proper (top) and detached (bottom) heat transfer element

reliability test vehicles passed the criteria of the conducted reliability tests (board level: HTSL, THB, RFLT, and TCoB; chip level: MSL3 and TC). Within the scope of the planned reliability test campaign, no significant differences between the two variants of the heat transfer element (assembled vs. wafer-bonded) could be determined with respect to long-term reliability indicators. Only some of the test vehicles with assembled heat transfer elements showed an initial structural failure. Specifically, the die-attach adhesive and the EMC exhibited signs of delamination from the Au-metallized backside of the embedded chips in some cases. The extent of delamination remained essentially constant during the course of the reliability tests, provided that the delamination was already present at the commencement of the tests. In the course of the reliability test, and specifically during the thermal cycling tests, no initiation of delamination was observed. This phenomenon is attributed to the generally poor adhesion of polymers to gold, which is a known materials interface challenge. Consequently, even during the grinding process of the manufacturing procedure, some heat transfer elements detached in certain instances (see Figure 8), reinforcing the conclusion that Au/polymer adhesion is a key factor. The presence of a backside metallization showed a strong influence on thermo-mechanical reliability under thermal cycling. The samples with a backside metallization had a significantly higher failure rate compared to the samples without metallization, as can be seen in Figure 9. The large,

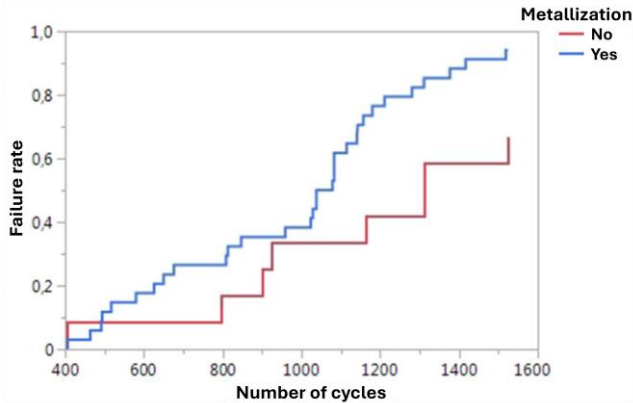


Figure 9: failure rate of the TCoB test samples

closed area represented by the rear metallization appears to produce significant stresses in the package due to the high CTE of the metals. In combination with the mechanically much stiffer GaN (more exactly GaN-on-SiC) technology compared to GaAs, this resulted in a delamination of the EMC from the flanks of the GaN dies and further crack propagation into the RDL. This, in turn, caused the failure. In terms of performance, all application demonstrators (Ka-band transceiver, E-band LNA, V-band HPA, transceiver for airborne radar) achieved their previously designed and simulated electrical performance metrics. Figure 10 shows the measured results for the E-band LNA with the antenna in the package. The upper left shows the simulation of the electrical field, while the other panels show the measured values for noise figure, linear gain and output power at 1 dB gain compression over the frequency spectrum. This proves that the demonstrator is operating within the desired frequency bandwidth.

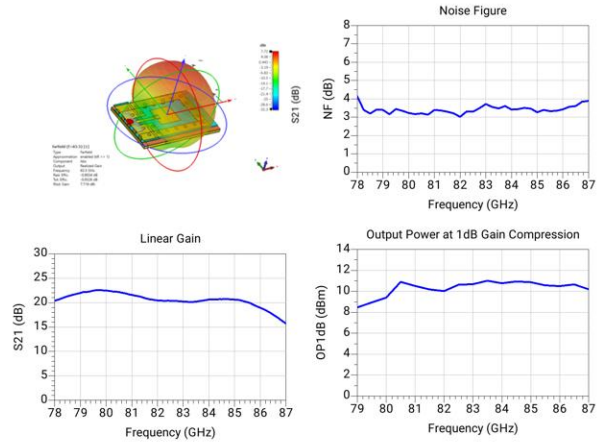


Figure 10: measurement results of the AiP package

## V. CONCLUSION

The feasibility of integrating diverse chip technologies, such as GaAs, GaN/GaN-on-SiC, and SiGe, simultaneously into one fan-out package using the developed heat transfer elements, while maintaining good reliability, has been demonstrated. This not only validates the use of fan-out (FO) packaging for high-frequency applications, but also demonstrates the advantages of FO technology in this field in terms of integration density, thermal paths, and functional co-integration. For example, the transceiver for airborne radar demonstrator with a GaN and a SiGe die in one FOWLP achieved a reduction of the footprint by approximately 50% compared to other solutions. The E-band LNA demonstrator showcased a straightforward antenna integration solution with just one RDL layer, as opposed to comparable solutions that require multiple RDL layers for adequate shielding and to prevent electromagnetic interference (EMI) and ensure electromagnetic compatibility (EMC). The face-up approach enabled a better heat management by the possibility of placing bumps directly onto the backside of the embedded chip, thereby reducing thermal resistance. The two developed solutions for integrating a heat transfer element demonstrated good performance, each having unique advantages and disadvantages. The assembled heat transfer element is a highly versatile solution, since the embedded dies do not require preliminary preparation and the solution is compatible with a broad spectrum of materials and device types. However, there appears to be scope for enhancement, as adhesion - particularly to Au-metallized backsides - is currently a matter of concern. The wafer-bonded heat transfer element demonstrates effective adhesion properties and is anticipated to achieve optimal reliability due to its material continuity and improved CTE matching. One of the main disadvantages is the necessity of accessing the front-end wafers prior to singulation. In future research, in addition to the further exploration and optimization of the technologies presented here, the focus will be on the increase of RDL layers for more complex routing and shielding concepts, the integration of SMD components to expand system functionality, and the integration of through-mold vias (TMV) to enable vertical interconnects and improved thermal paths within the fan-out package.

## ACKNOWLEDGMENT

The authors acknowledge the partner members of the project SMART3 (supported by French 2022 Nanoelectronic Plan (DGE / AID)).

APECS is co-founded by the European Commission and national ministries of the eight member states within the framework of the EU Chips Act.

## REFERENCES

- [1] J. H. Lau et al., "Fan-Out Wafer-Level Packaging for Heterogeneous Integration," in *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 8, no. 9, pp. 1544-1560, Sept. 2018, doi: 10.1109/TCPMT.2018.2848649.
- [2] T. Braun et al., "Panel Level Packaging - A View Along the Process Chain," 2018 IEEE 68th Electronic Components and Technology Conference (ECTC), San Diego, CA, USA, 2018, pp. 70-78, doi: 10.1109/ECTC.2018.00019.
- [3] A. Tomas et al., "Reliability of Fan-Out Wafer Level Packaging For III-V RF Power MMICs," 2021 IEEE 71st Electronic Components and Technology Conference (ECTC), San Diego, CA, USA, 2021, pp. 1779-1785, doi: 10.1109/ECTC32696.2021.00281.
- [4] S. S. Siew Boon et al., "Multi-RF Chip Module Through FOWLP," 2024 IEEE 26th Electronics Packaging Technology Conference (EPTC), Singapore, 2024, pp. 172-177, doi: 10.1109/EPTC62800.2024.10909941.
- [5] B. Yu et al., "A Wideband mmWave Antenna in Fan-Out Wafer Level Packaging With Tall Vertical Interconnects for 5G Wireless Communication," in *IEEE Transactions on Antennas and Propagation*, vol. 69, no. 10, pp. 6906-6911, Oct. 2021, doi: 10.1109/TAP.2021.3087859.