0.1µm-UMS GaN-on-SiC Technology: Qualification & Perspectives

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***Abstract* — UMS has developed a new generation of GaN-on SiC technology identified as GH10-10. Promising performance, good device robustness and reduced memory effect were achieved with a combination of process and device optimization. Large signal measurements were performed at 18 GHz, 30GHz, 45 GHz and 60 GHz. The results at 45 GHz have shown more than 46% of PAE, 11dB linear gain and 2.5 W.mm^{-1} output power. At 60 GHz, a maximum PAE of 31-33% is obtained. The nonlinear electrical model accuracy is proven with the HPA designed at Q-Band and showing promising results.**

***Keywords* — GaN, HEMT, transistor, power amplifiers.**

I. Introduction

The Gallium-Nitride (GaN) HEMTs technology enables high power and high efficiency operation in a wide range of applications compared to a decade ago [1], communication systems [2], and radars [3]. Further enhancements of the technology first commercialized by UMS in 2012 are pursued to address higher frequency application up to V-band as well as deliver improved linearity, and power efficiency up to V-bands and below.

An optimization of 100 nm-GaN HEMT device process to be described subsequently has achieved F_{Max} around 200 GHz, an I_{DSS} of 1.5 A.mm^{-1}, a maximum transconductance Gm of 0.55 S.mm^{-1} and the threshold voltage of -2.6 V allowing a high voltage swing margin for operation at 15V or higher.

This paper describes several of the key challenges faced in bringing this technology to fruition. After the description of the MMIC technology and key elements of its optimization, the main achievement are discussed: the Schottky robustness, the memory effect and the main performance obtained will be deeply discussed on the device and also at the MMIC level.

II. MMIC Technology

A GaN epitaxial layers is grown on the Ga-face by MOCVD after an initial nucleation layer on an initial 100 mm diameter 4H SiC substrate. A buffer layer is engineered to intentionally incorporate deep acceptors Fe. Due to lattice misfit, dislocations also act as electronic traps that affect the resistivity [4], [5], and [6].

The GaN technology described leverages existing production technologies from 0.5 µm [7] to 0.15 µm [8] nodes featuring a passivated T-gate structure, two routing levels of thick metal, metal-insulator-metal capacitors and high value resistors. In this node, further lateral scaling of the gate length to 100 nm has been achieved. For improved gain level, the SiC substrate is thinned to 50 µm and backside metalized connected to the front-side through via-holes. The contact resistance of the ohmic contacts has been minimized to less than 0.1 Ω.mm. These regions are commonly recessed to minimize the series resistance to the channel region or also heavily doped with a Si implantation subsequently activated with a thermal process similar to [9]. Comparable low resistance values have been reported using alternative approach with epitaxial regrown layer [10] and implemented also on commercial, high performances GaN platforms [11], [12].

III. Optimized Gate for Schottky Robustness

The gate electrode is laterally scaled to 100 nm with e-beam lithography. The combination of the reduced gate length and a thinner barrier increases the electric field with a maximum occurring immediately adjacent to the gate on the drain side. The shape of the gate has been engineered to moderate the field strength.

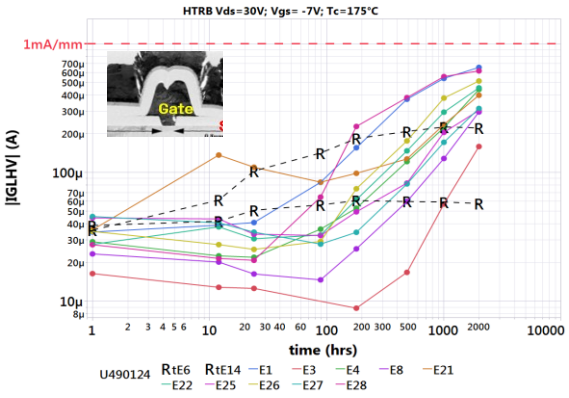

Fig. 1. Gate Leakage after measured 1000 h under V_{DS} bias of 30 V and with Vgs of -7 V, temperature of 175°C.

As an indicator of the device reliability as in [13], the measured gate leakage is approximately 100 µA.mm^{-1} at a DC bias at V_{DS}=20 V, V_{GS}=-7 V at 25°C. In addition, the break down voltage of 90 V is achieved under Vgs bias of -7 V.

To assess the gate robustness, the High Temperature Reverse Bias (HTRB) is carried out at 175°C under high voltage (Vds=30 V) as shown in Fig.1. The obtained leakage after 1000 h, is less than 200 µA.mm^{-}. These results confirm the robustness of the device and the capability of operating at high voltage.

IV. Memory Effect Investigation

Bulk and surface trapping phenomena can highly affect the performance of GaN FETs [14], [15], and the switching properties. The effect of the traps can be observed on the transient drain current characteristics as shown in [16].

The impact of the memory effects on the device behavior is very much dependent on the operative conditions (e.g: bias, load-line, gain compression level); at the same time, the acceptable impact is very much dependent on the applications. This makes hard establishing a figure of merit or a global specification for these effects and the evaluation of the compatibility of technology with the application remains a task for the system houses.

Nevertheless, it is important for a foundry to monitor the memory effect on a GaN technology, during the development to ensure a good coverage of the application needs and during the production to ensure an homogeneous behavior across the wafer and wafer to wafer. UMS has, thus, developed a memory measurement method based on the transient drain current including DC trapping excitation of the device to highlight the recovery time of the devices and predict the impact on the HPA and switching applications,.

From the previous UMS GaN technologies experience, UMS has fixed a target for the time constant of the main traps activation to reach current recovery of 90% of the targeted current. Of course the results are linked to the measurement conditions applied during this sequence.

The memory sequence of the GaN technology at UMS is defined for each technology by taking into account the technology maximum ratings to stay in the safe operating area, without device degradation but with the highest trapping excitation on the gate to get the worst case. The Vds is set to 1 V for all the technologies whereas the trapping gate voltage depends on the technology. For example, Vgs is set at: -40 V for GH25-10, -30 V for GH15-10 and Vgs of -20 V for GH10-10.

This memory test sequence is based on three main steps in addition to the burn-in phase: **Reset**, **Excitation** and **Relaxation** step during with the drain current is monitored. The chronogram of the memory sequence is given in the fig. 2.

This measurement is carried out on the 8x75-µm device at ambient temperature. Before the start of the sequence the device is biased at Vd =1 V, Vg=0 V during 5 S, called burning phase. This allows to make all the virgin devices in the same electrical state.

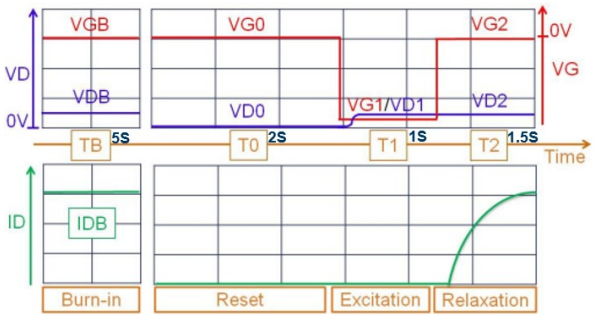

Fig. 2. Chronogram of the memory test sequence.

Then, the sequence starts first with the reset phase under the bias of [Vds, Vgs] of [0 V, 0 V] as a reference point. Secondly, the trapping within the excitation step is performed with [Vgs= -20 V, Vds = 1 V] during 1 S along with the deep channel depletion under the gate and the drain region is reached. After that the device is driven to the on state at the relaxation (step2) with [Vgs =0V] and Vds kept at 1V to allow the electron excursion in the channel. The Fig.3 shows the illustration of the bias swings on Ids (Vds) curve and the behavior of the transient current regarding the ideal case in red.

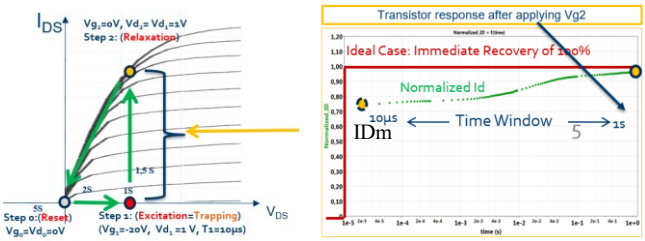

Fig. 3. Illustration of the test sequence measurement steps and the monitoring of the drain current.

Then, the trapping profile will impact the initial memory current (IDM) level and the main time constant needed to reach 90% of the targeted current.

The Fig.4 shows the measured transient drain current versus the time in logarithm scale. The memory current (IDm) reached at the beginning of the relaxation step is around 80% of the targeted current witch is a good level. After that, the transient current increases with the time to reach the level of 90% of current recovery with less than 10 mS as time constant of the main traps. This main constant is extracted from the first and the second derivative of the fitted current at the Ids slope. This time constant is commonly correlated to the main traps in the buffer and the bulk.

The results obtained on GH10 with less than 10 mS main time constant shows a good behavior as well as the GH15-10 and GH25-10 UMS-GaN technologies with a main constant of 15 ms and 20 mS, respectively .

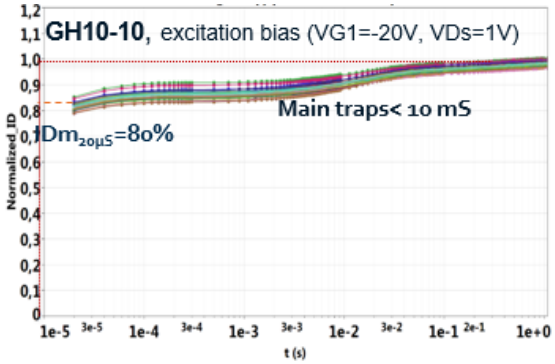

Fig. 4. The transient drain current measured during the relaxation phase at Vgs=0V and Vds=1V

Then this result should allow faster signal recovery at high compression as already demonstrated on GH15-10 and GH25-10.

V. Load-Pull Performance

The large signal measurements are performed at frequencies: 18 GHz, 30 GHz, 45 GHz and 60 GHz. The measurements are de-embedded at the intrinsic device reference plane. All measurements discussed in this paper are performed at ambient temperature without harmonic tuning.

At 18GHz the peak PAE is approaching the 60% of PAE at Opt PAE with the maximum density of 3.25W.mm^{-1}at opt Pout. This good value are well saved @30GHz with 55% of Peak PAE and 3 W.mm^{-1}of power density.

In the following, the main results obtained at 45 GHz are presented to give an overview of the capability of this technology in Q band. After that the overall performances versus the frequency will be discussed.

A. Measured results at 45GHz

Power sweep measurements are performed at 45GHz at Vds= 15 V and Idq= 150 mA.mm^{-1} on the 6x50-µm FET. The impedance load is matched for the maximum PAE.

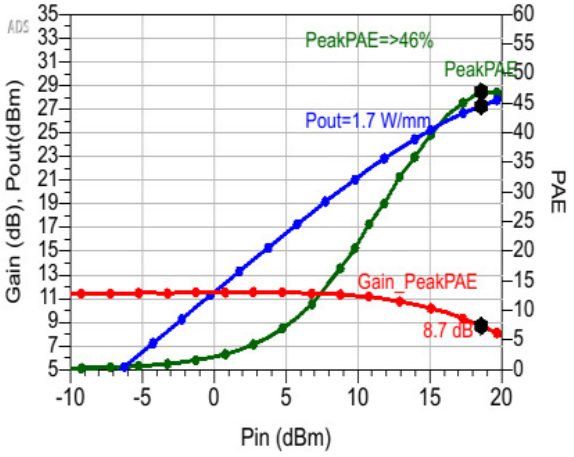

Fig. 5. Load-Pull measurement performed at 45GHz for a transistor geometry of 6x50µm at bias conditions V_{DS}=15V and I_{dq}=150mA.mm^{-1}, Z_L= Optimum PAE.

As shown in the Fig.5, the results obtained on the 6x50µm transistor are state of the art with a maximum PAE above 46%, Pout and Gain obtained at Peak-PAE of 1.7W.mm-^{1} and 8.7dB respectively. The linear power gain is larger than 11.5 dB.

B. Load-Pull results vs frequency up to 60GHz

In addition to the measurement capabilities at 45GHz and due to the unavailability of load-Pull measurement capability @60 GHz in the RF community to our knowledge, UMS has implemented a new load-Pull test bench @60GHz to assess the RF performances of GH10-10 up to V Band.

Measurements were performed on the 6x50 µm on the individual source via transistor biased at V_{DS}= 15 V and I_{dq}= 150 mA.mm^{-1}. First, the impedance load is matched for maximum PAE to get the maximum available PAE and then matched for max Power to extract the maximum power achievable.

The Fig.6 shows the Peak PAE, the power density and the linear gain achievable at each frequency.

@60GHz, a maximum PAE of 31-33% is obtained with maximum output power density of 2.8W/mm^{-1} when the load is centered at the maximum Pout. The linear gain around 8dB.

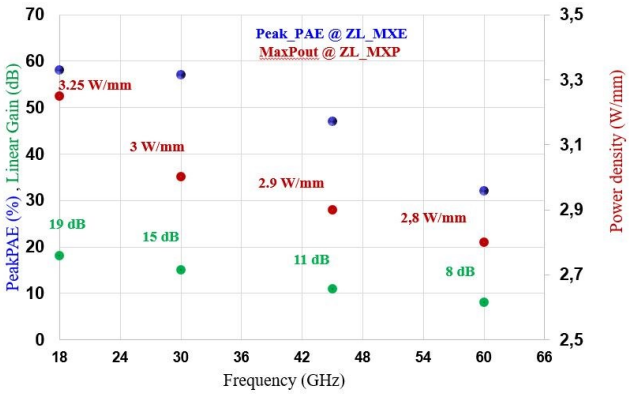

Fig. 6. Load-Pull measurement performed at 18 GHz, 30 GHz, 45 GHz and 60 GHz for a transistor geometry of 6x50µm, at bias conditions of VDS=15V and Idq=150mA.mm-1, ZL= Optimum PAE for Peak PAE and ZL= Optimum Pout for the maximum power density.

VI. GH10 MMIC capability at Q band

To assess the design activities with the GH10-10 technology a Process Design kit (PDK) is developed, including: the thermal electrical models, the linear Noise models and the RF FET switch models.

The back simulation of high power amplifier designed at UMS at Q-band for SatCom application shows the good agreement between the measurement and the simulation, fig.7.

This good agreement obtained between the measurement and the simulation illustrates the good reproducibility of the process the accuracy of the model and the design capability at high frequency.

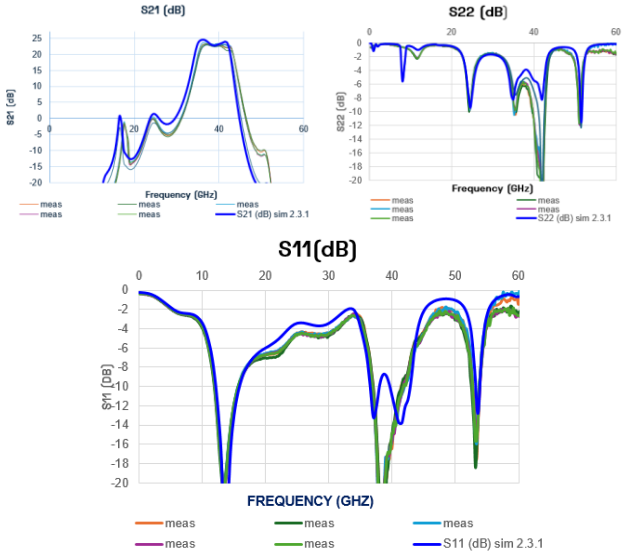

Fig. 7. Comparison of the small signal measurements of the Q-band HPA and the model of the GH10-10 PDK under bias conditions V_{DS}=15V and I_{dq}=100mA.mm^{-1}

VII. Conclusion

UMS has extended its GaN technology portfolio to include a 100nm node. The combination of both vertical and lateral scaling and the optimization of both the epitaxy and the process has achieved, a good gate robustness, short recovery time (<10mS) and a competitive performance measured up to 60GHz. At 45GHz, a peak PAE of 47%, a maximum Pout of 2.9W.mm^{-1} and a linear gain of 11.5dB were demonstrated. At 60GHz, excellent results are obtained with more than 31% of Peak-PAE, 2.8W.mm^{-1} maximum output power, and 8 dB of linear gain. To the author's knowledge, these are the first experimental large signal results published at 60 GHz on an industrial GaN technology. In addition, the high good PAE level obtained at 18 GHz and at 30 GHz demonstrate that GH10 is a good technology candidate also for lower frequency applications by simplifying thermal management thanks to an improved PAE.

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References

[1] A. Lidow, J. Strydom, R. Strittmatter and C. Zhou, "GaN: A Reliable Future in Power Conversion: Dramatic performance improvements at a lower cost," in *IEEE Power Electronics Magazine*, vol. 2, no. 1, pp. 20-26, March 2015.

[2] S. Ganguly et al., "DC and RF Reliability Assessment of 5G-MMW capable GaN HEMT Process (Invited)," 2022 IEEE International Reliability Physics Symposium (IRPS), Dallas, TX, USA, 2022, pp. 11B.5-1-11B.5-6improvements at a lower cost," IEEE Power Electronics Magazine,

[3] G. Formicone, J. Burger, R. Keshishian and J. Walker, "A 1.5kW 90V S-band GaN Transistor for Air Traffic Control Radars," 2022 17th European Microwave Integrated Circuits Conference (EuMIC), Milan, Italy, 2022, pp. 76-79.

[4] F. A. Marino, N. Faralli, T. Palacios, D. K. Ferry, S. M. Goodnick and M. Saraniti, "Effects of Threading Dislocations on AlGaN/GaN High-Electron Mobility Transistors," in IEEE Transactions on Electron Devices, vol. 57, no. 1, pp. 353-360, Jan. 2010

[5] P. Roy, S. Jawanpuria, Vismita, S. Prasad and A. Islam, "Characterization of AlGaN and GaN Based HEMT with AlN Interfacial Spacer," 2015 Fifth International Conference on Communication Systems and Network Technologies, Gwalior, India, 2015, pp. 786-788.

[6] T. Zhang *et al.*, "Current-Collapse Suppression of High-Performance Lateral AlGaN/GaN Schottky Barrier Diodes by a Thick GaN Cap Layer," in *IEEE Electron Device Letters*, vol. 42, no. 4, pp. 477-480, April 2021.

[7] D. Floriot et al., "New qualified industrial AlGaN/GaN HEMT process: Power performances & reliability figures of merit," 2012 7th European Microwave Integrated Circuit Conference, Amsterdam, Netherlands, 2012, pp. 317-320.

[8] V. Di Giacomo-Brunel et al., "Industrial 0.15-µm AlGaN/GaN on SiC Technology for Applications up to Ka Band," 2018 13th European Microwave Integrated Circuits Conference (EuMIC), Madrid, Spain, 2018, pp. 1-4.

[9] P. Fedeli et al., "Ni-Al-Ti ohmic contacts on Al implanted 4H-SiC," 2016 European Conference on Silicon Carbide & Related Materials (ECSCRM), Halkidiki, Greece, 2016, pp. 1-1

[10] Y. Zhou et al., "A Novel Regrown Ohmic Contact Technique to Improve the Performance of GaN HEMT," 2022 IEEE MTT-S International Microwave Workshop Series on Advanced Materials and Processes for RF and THz Applications (IMWS-AMP), Guangzhou, China, 2022, pp. 1-3.

[11] Y. Cao et al., "Qorvo's Emerging GaN Technologies for mmWave Applications," 2020 IEEE/MTT-S International Microwave Symposium (IMS), Los Angeles, CA, USA, 2020, pp. 570-572.

[12] R. Leblanc, P. Frijlink and M. Rocchi, "Sub-100nm GaN/Si MMIC processes for 6G telecommunications," *2022 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS)*, Phoenix, AZ, USA, 2022, pp. 160-165.

[13] J. -S. Moon *et al.*, "Power Scaling of Graded-Channel GaN HEMTs With Mini-Field-Plate T-gate and 156 GHz fT," in *IEEE Electron Device Letters*, vol. 42, no. 6, pp. 796-799, June 2021.

[14] R. Ye et al, An Overview on Analyses and Suppression Methods of Trapping Effects in AlGaN/GaN HEMTs, in IEEE Access, vol. 10, pp. 21759-21773, 2022.

[15] G. Meneghesso, M. Meneghini, E. Zanoni, P. Vanmeerbeek and P. Moens, "Trapping induced parasitic effects in GaN-HEMT for power switching applications," 2015 International Conference on IC Design & Technology (ICICDT), Leuven, Belgium, 2015, pp. 1-4, doi: 10.1109/ICICDT.2015.7165899.