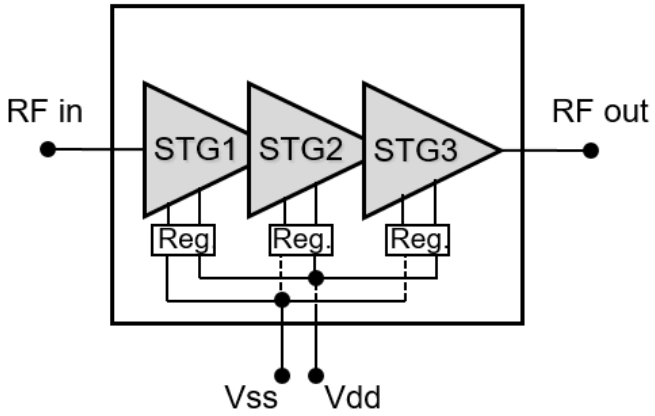
Advanced Information: AI2409

30 – 44GHz Low Noise Amplifier

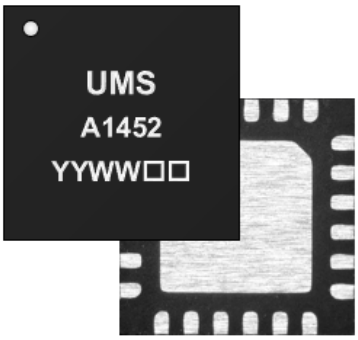
GaAs Monolithic Microwave IC



The CHA1452-QDG is a three-stage GaAs Low Noise Amplifier operating in the 30 – 44GHz frequency band including current regulation circuit on each stage. This LNA typically presents low Noise Figure of 1.75dB associated to a small signal Gain of 20dB.
It can provide up to 4dBm output power at 1dB gain compression and needs DC power supply of Vdd=3V and Vss=-3V corresponding to a current of 47mA. The current variation is lower than 2mA when the temperature varies from -40°C to 85°C thanks to the integrated regulation on each stage of the LNA. It is available in 4x4 plastic package.

Designed for space applications, it is also ideal for a wide range of microwave systems.

This new product is developed using GaAs pHEMT process and is provided on low cost SMD RoHS compliant QFN plastic package.



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Electrical Characteristics

Tcase= +25°C,

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	30		44	GHz
Gain	Small signal Gain		20		dB
NF	Noise Figure		1.8		dB
S11	Input Return loss		10		dB
S22	Output return loss		10		dB
OP1dB	Output Power at 1dB gain compression		4		dBm
OIP3	Output Third order Intercept Point		14		dBm
Vdd	Quiescent Drain voltage		3		V
Vss	Quiescent Gate voltage		-3		V
Id	Quiescent Current		47		mA
PDC	DC Power Consumption		141		mW

These values are representative of on board measurements as defined on the drawing in paragraph "Evaluation board".

Absolute Maximum Ratings (1)

Tcase= +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	4	V
Vg	Gate bias voltage	-4	V
Pin	Maximum peak input power overdrive	0	dBm
Id	Quiescent Drain current	70	mA

(1) Operation of this device above anyone of these parameters may cause permanent damage.

Recommended Operating Range (2), (3)

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	2.5 – 3.5	V
Vg	Gate bias voltage	-2.5 – -3.5	V
Pin	Maximum peak input power overdrive (2)	-5	dBm
$T_{junction}$	Junction temperature	175	°C
T_{case}	Operating temperature range	-40 to 85	°C
T_{stg}	Storage temperature range	-55 to 150	°C

(2) Electrical performances are defined for specified test conditions
(3) Electrical performances are not guaranteed over all recommended operating conditions

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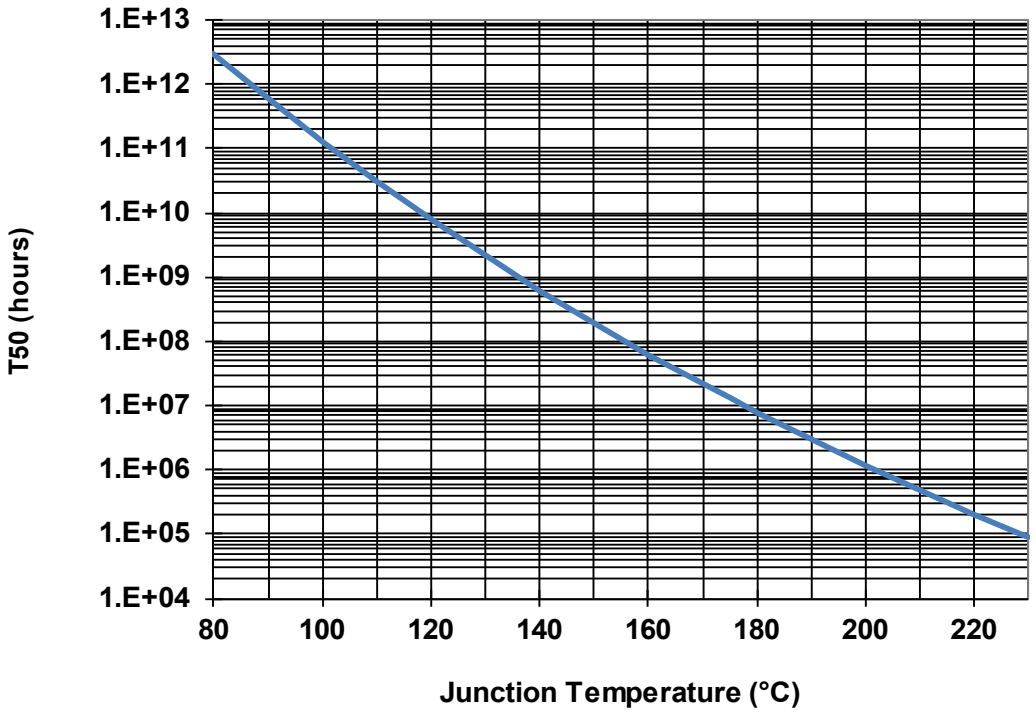
Device thermal performance

All the figures given in this section are obtained assuming that the die is only cooled down by conduction through the package case.
The temperature is monitored at the QFN backside interface (T_{case}).
For nominal operation, the system's maximum temperature must be adjusted to ensure that the junction temperature ($T_{junction}$) remains below the maximum value specified in the Recommended Operating Ratings table.
The system PCB must be designed to comply with this requirement.

Parameter	Biasing conditions	$T_{junction}$ (°C)	R_{TH} (°C/W)	T_{50} [2] (hours)
R_{TH} [1] Thermal Resistance (Junction to Case)	Vdd= 3V Vss=-3V Pdiss= 145mW	121	248	7E+09
	Vdd= 2.5V Vss= -2.5V Pdiss= 92.5mW	108	249	4E+10

[1] Assuming 85°C T_{case}

[2] The time at which 50% of the products are expected to have failed or reached the end of their useful life.



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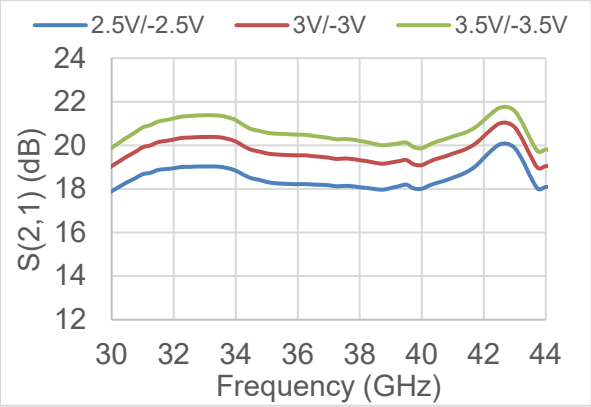
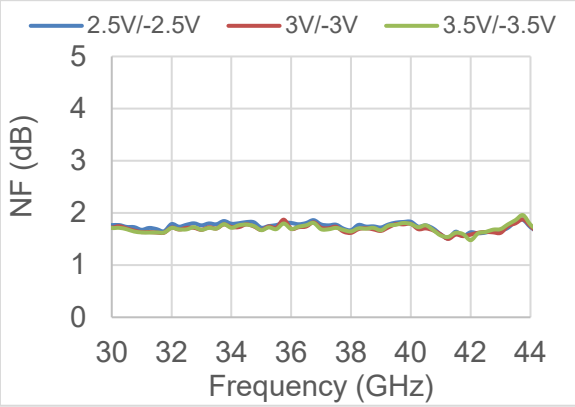
Typical Board Measurements

Board losses are de-embedded. Measurements are given in the package reference planes.
Test conditions : CW, T_{case} = 25°C, Vdd /Vss= 2.5V/-2.5V ; -3V/3V ; -3.5V/3.5V

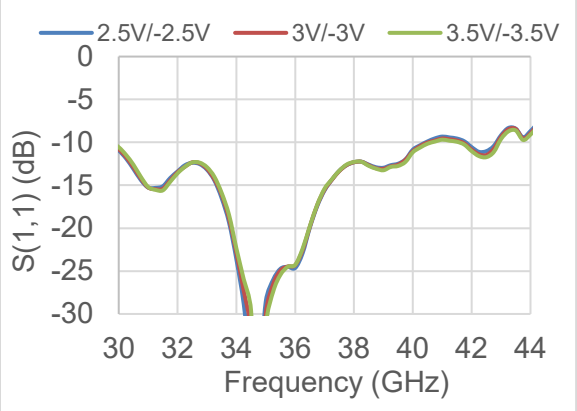
Linear Gain vs. frequency and Bias



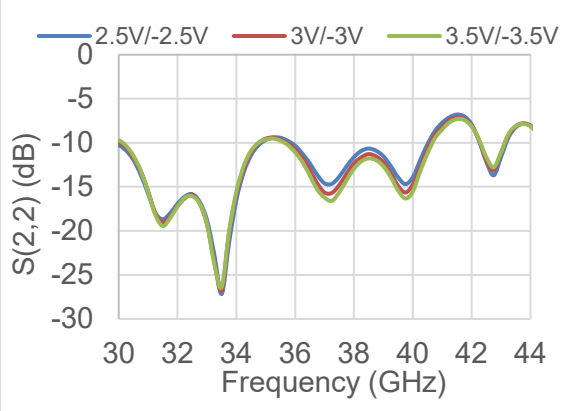
Noise Factor vs. frequency and Bias



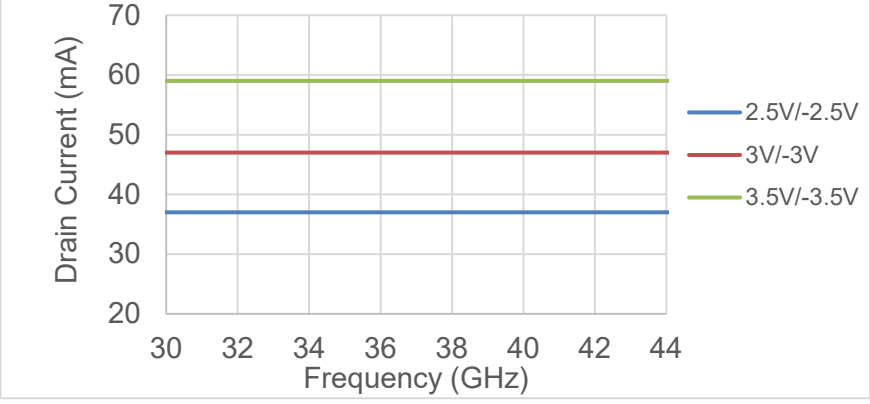
Input return loss vs. frequency and Bias



Output return loss vs. frequency and Bias



Drain Current vs. frequency vs. Bias



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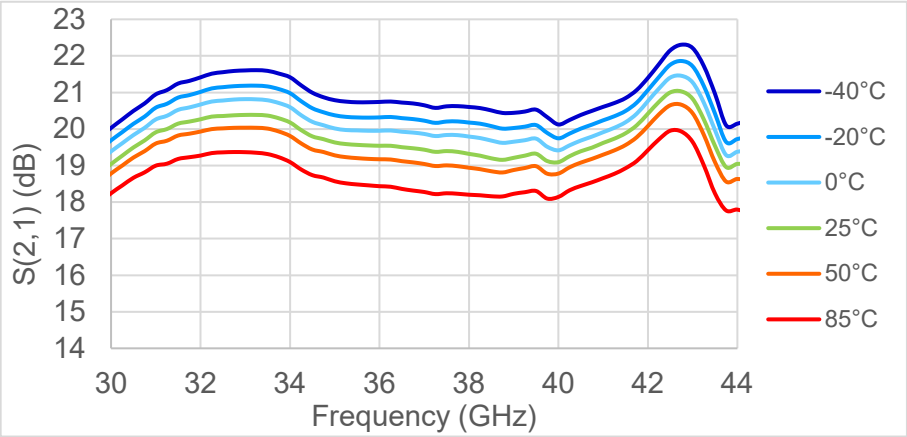
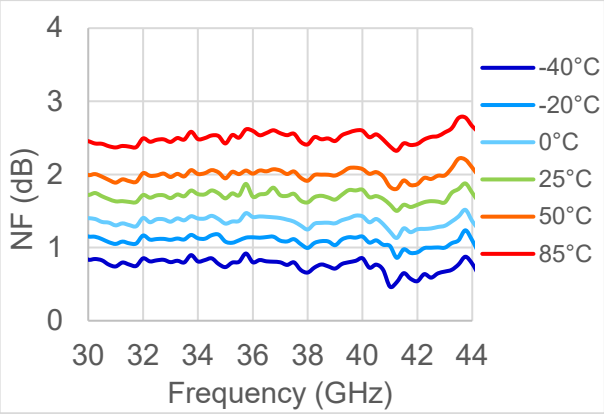
Typical Board Measurements

Board losses are de-embedded. Measurements are given in the package reference planes.
Test conditions : CW, T_{case} = -40°C/-20°C/0°C/25°C/50°C/85°C, Vdd /Vss= -3V/3V

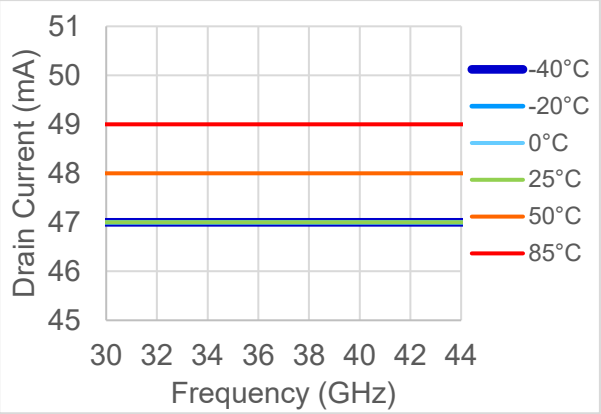
Linear Gain over temperature



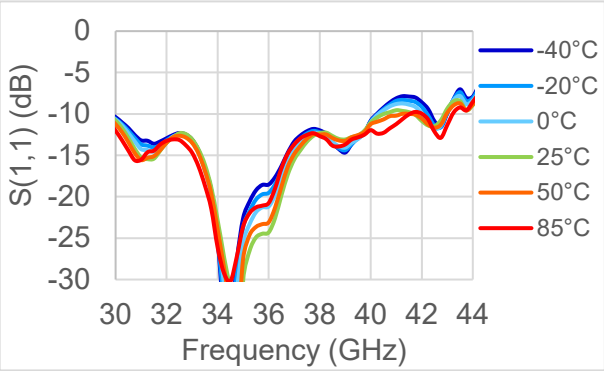
Noise Factor vs. frequency and Temp



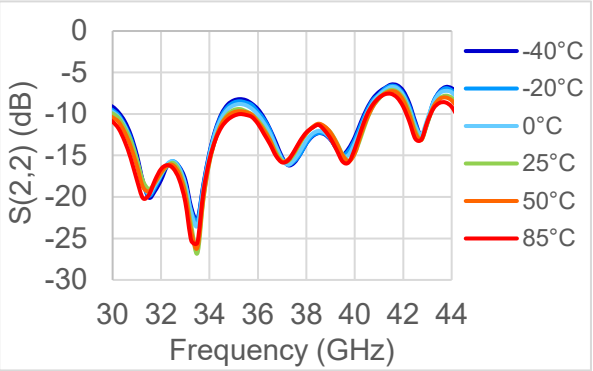
Drain Current vs. frequency and Temp



Input return loss vs. frequency and Temp



Output return loss vs. frequency and Temp



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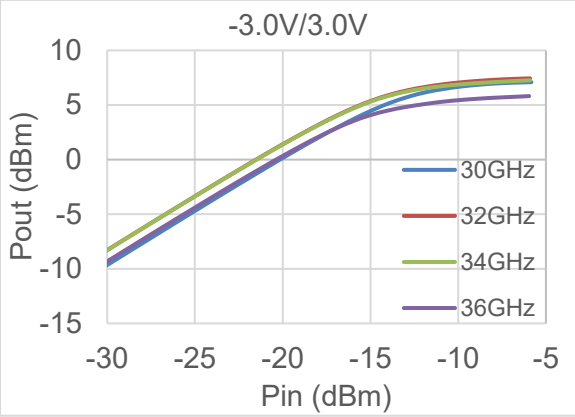
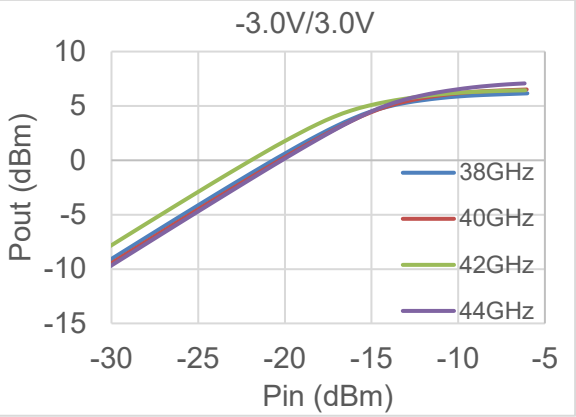
Typical Board Measurements

Board losses are de-embedded. Measurements are given in the package reference planes.
Test conditions : CW, T_{case} = -40°C/25°C/85°C, Vdd /Vss=-3V/3V

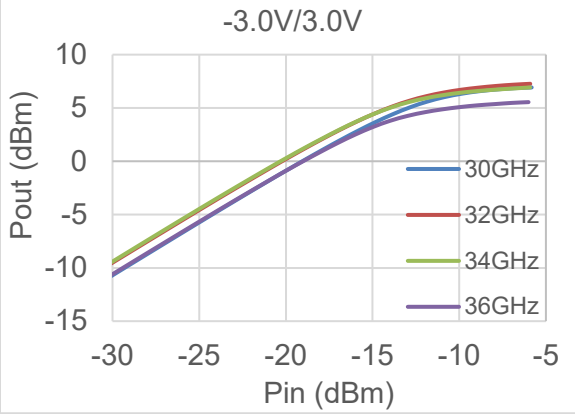
Output Power vs. Input Power @ -40°C



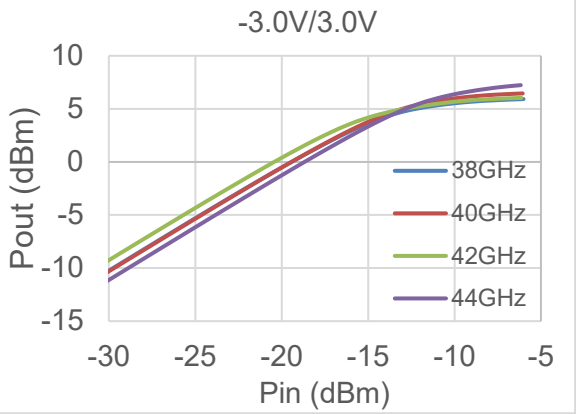
Output Power vs. Input Power@ -40°C



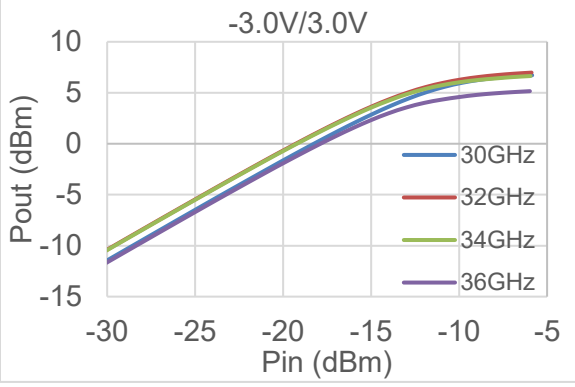
Output Power vs. Input Power @ 25°C



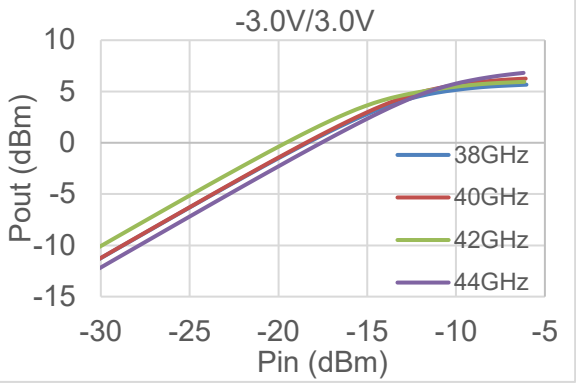
Output Power vs. Input Power @ 25°C



Output Power vs. Input Power @ 85°C



Output Power vs. Input Power @ 85°C



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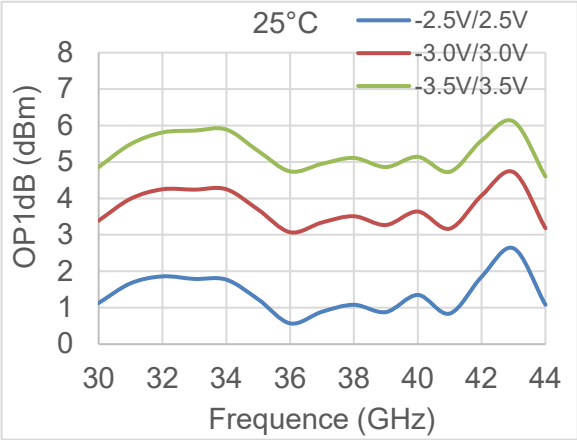
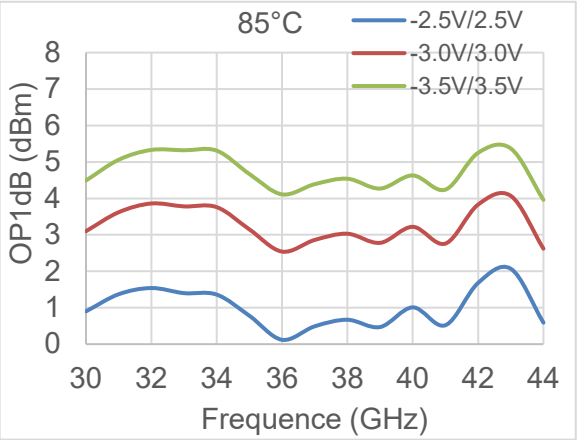
Typical Board Measurements

Board losses are de-embedded. Measurements are given in the package reference planes.
Test conditions : CW, T_{case} = -40°C/25°C/85°C, Vdd /Vss=-2.5V/2.5V ; -3V/3V ; -3.5V/3.5V

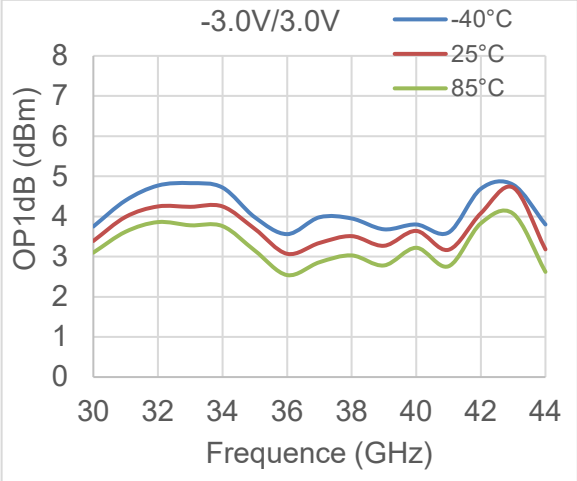
OP1dB vs. frequency @ 25°C and Bias



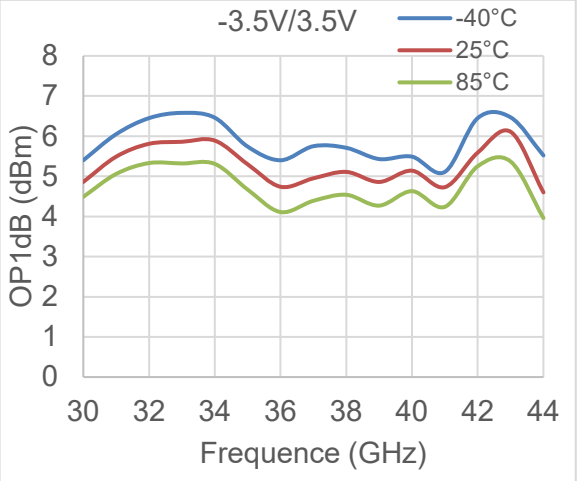
OP1dB vs. frequency @ 85°C and Bias



OP1dB vs. frequency @ -3V/3V and Temp



OP1dB vs. frequency @ -3.5V/3.5V and Temp



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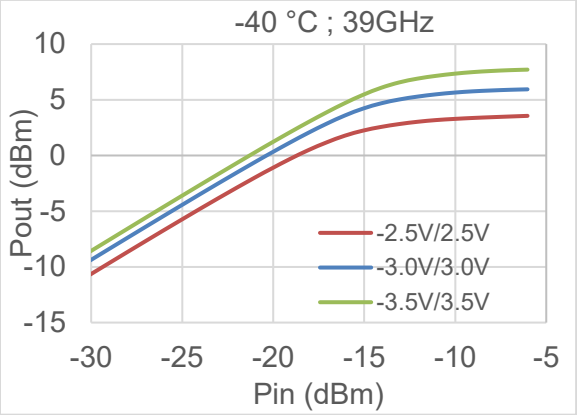
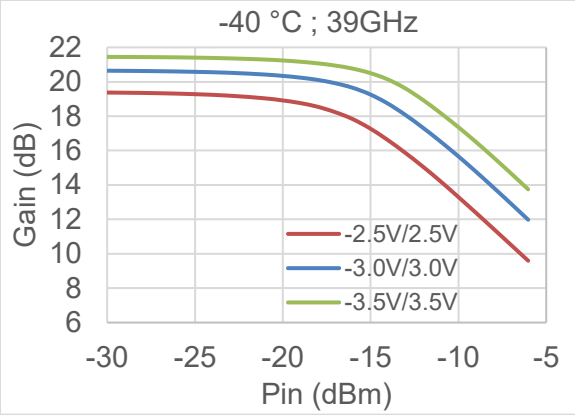
Typical Board Measurements

Board losses are de-embedded. Measurements are given in the package reference planes.
Test conditions : CW, T_{case} = -40°C/25°C/85°C, Vdd /Vss=-2.5V/2.5V ; -3V/3V ; -3.5V/3.5V

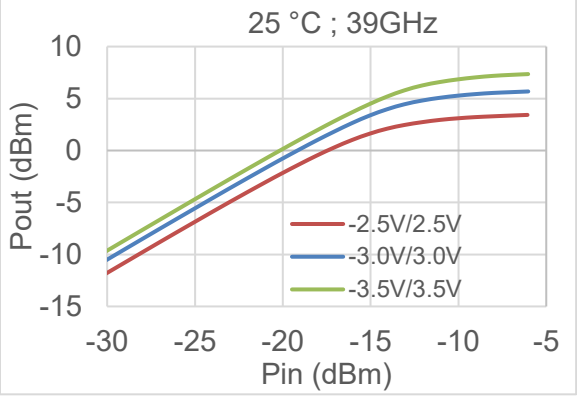
Output Power vs. Input Power



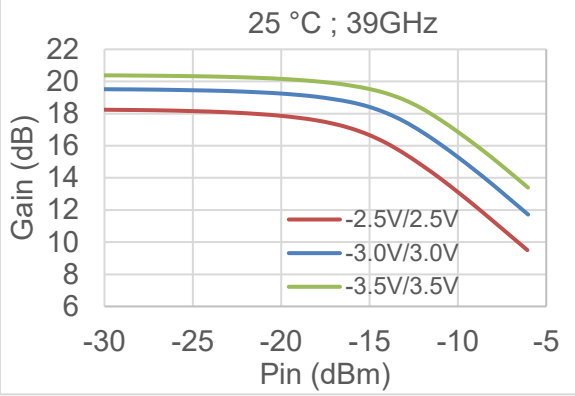
Power Gain vs. Input Power



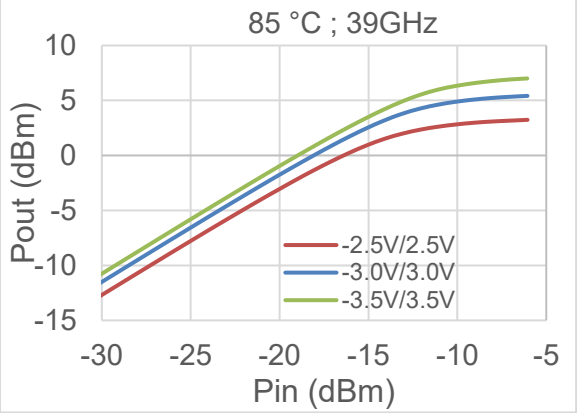
Output Power vs. Input Power



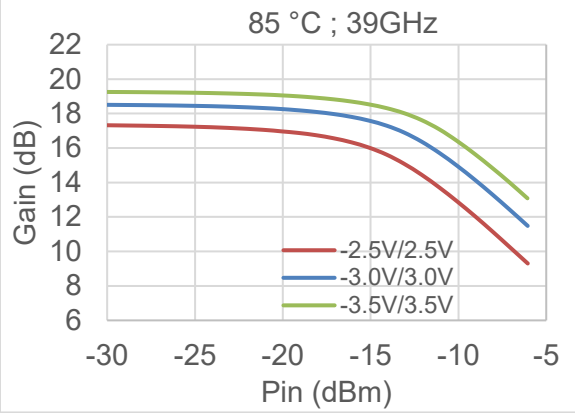
Power Gain vs. Input Power



Output Power vs. Input Power



Power Gain vs. Input Power



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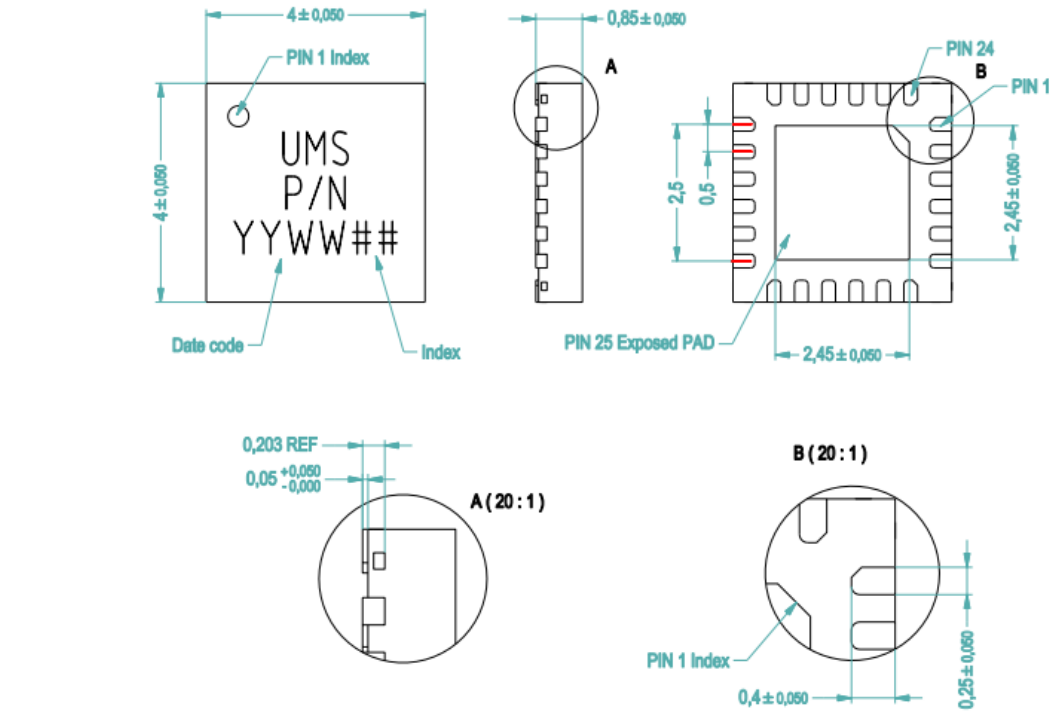
Package outline (1)



Finish:	Matt tin Lead Free (Green)	1- NC	9- Vg	17- GND(2)
Units :	mm	2- GND(2)	10- Vd	18- NC
From the standard :	JEDEC MO-220	3- GND(2)	11- NC	19- NC
	(VGGD)	4- RF in	12- GND(2)	20- NC
25-	GND	5- GND(2)	13- GND(2)	21- NC
		6- GND(2)	14- GND(2)	22- NC
		7- NC	15- RF out	23- NC
		8- NC	16- GND(2)	24- NC

(1) Refer to the application note AN0017 (https://www.ums-rf.com) for general consideration and recommendations for Molded Plastic QFN/DFN packages.

(2) It is strongly recommended to ground all pins marked “GND” through the PCB.
Ensure that the PCB is designed to provide the best possible ground to the package.

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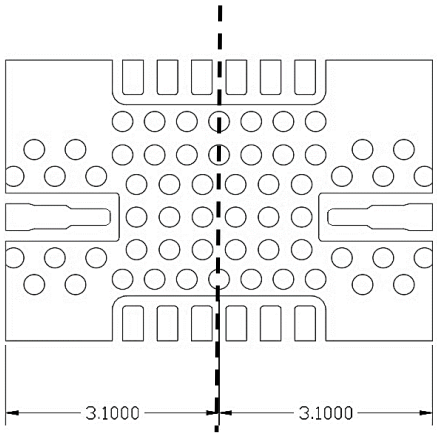
Definition of measurements reference planes

The reference planes used measurements given above are symmetrical from the symmetrical axis of the package (see drawing beside). The input and output reference planes are located at 3.1mm offset (input wise and output wise respectively) from this axis.



Package Information

Parameter	Value
Package body material	RoHS-compliant
	Low stress Injection Molded Plastic
Lead finish	Matt tin
MSL Rating	MSL3

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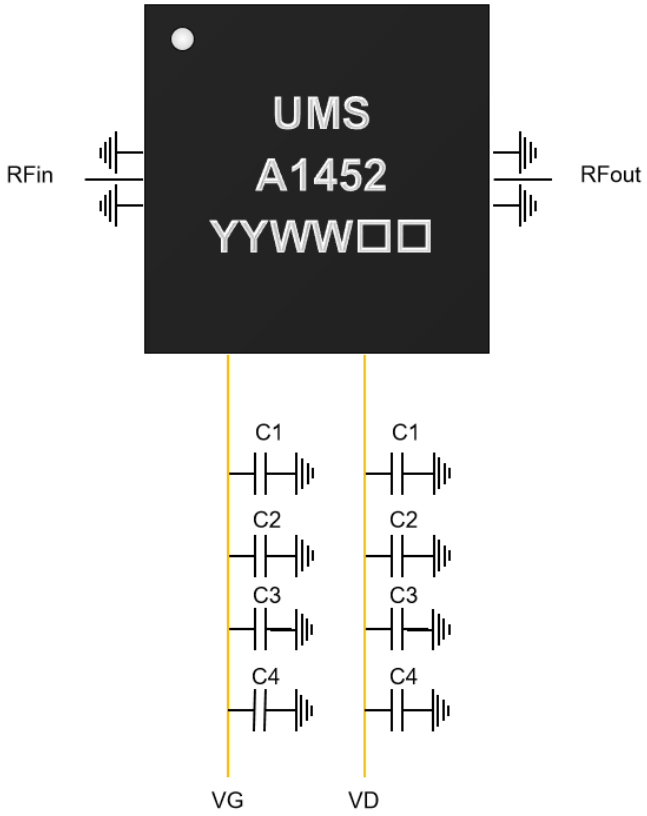
Recommended Assembly Plan



Bill of Materials

Label	Value	Description
C1	RF	Capacitor 120pF ±15% 20V
C2	RF	Capacitor 10nF ±10% 20V
C3	RF	Capacitor 1µF ±10% 20V
C4	RF	Capacitor 10µF ±10% 20V

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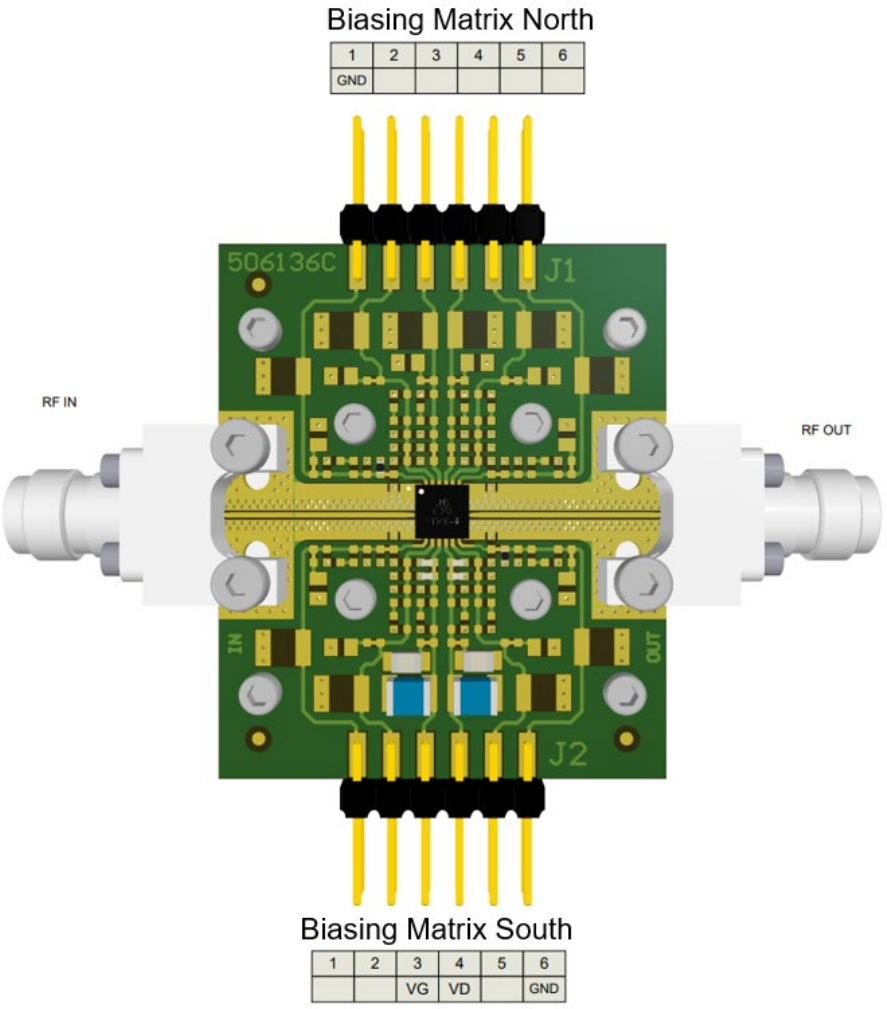
Evaluation Board

- Compatible with the proposed footprint.
- Based on typically Ro4350 / 8mils or equivalent.
- Using a micro-strip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 120pF, 10nF, 1µF, 10µF ±10% are recommended for all DC accesses.
- See application note AN0017 for details.



Notes:
All board measurements are performed using shielded cables, even for DC bias, to ensure safe operation.

Refer to the application note AN0031 available at http://www.ums-rf.com for the description of Evaluation Board for Packaged Die and recommendations for this UMS package.

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Notes

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Recommended package footprint

Refer to the application note AN0017 available at http://www.ums-rf.com for package foot print recommendations.

SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017 available at http://www.ums-rf.com.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at http://www.ums-rf.com.

Recommended ESD management

Refer to the application note AN0020 available at http://www.ums-rf.com for ESD sensitivity and handling recommendations for the UMS package products.

Maturity Level

Maturity Level	Product status	Documentation	Reliability	Usage in a system
Lab Sample (LS)	Decision to develop the product is not confirmed	Technical Information	No commitment	Lab demonstrator
Engineering Sample (ES)	**Design may change**	**Advanced Information**	**The design is within the recommended temperature, current and voltage ranges as regards the technology used.**	**Engineering demonstrator**
Product Representative Unit (PRU)	Design is frozen	Data-sheet	Tests results are available on the foreseen product or on an similar one	Production

Sampling request reference

Package: ES- CHA1452-QDG
Demo board: EVB-CHA1452-QDG

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+1 (781) 791-5078 (USA)
+65 9298 8316 (Singapore)

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