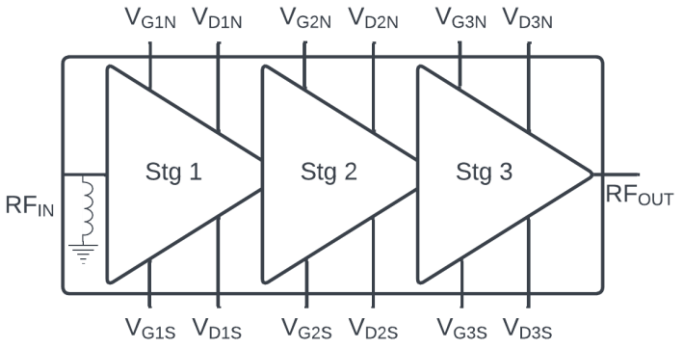
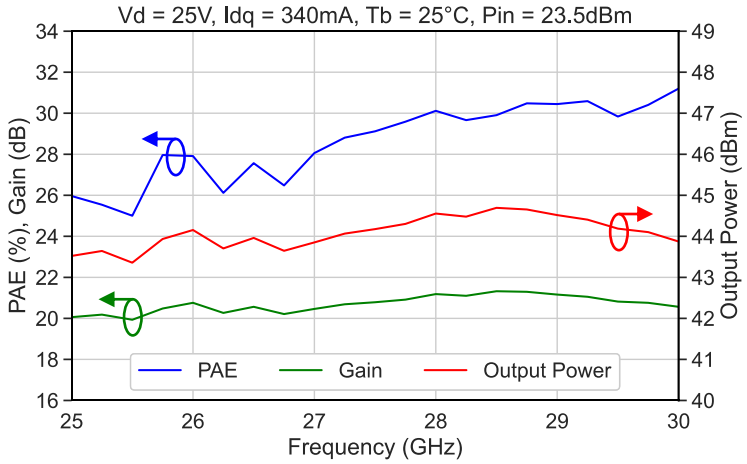
Advanced Information: AI2509

25-29GHz 25W High Power Amplifier

GaN Monolithic Microwave IC



The CHA8682-98F is a 3-stage high power amplifier operating between 25 and 29GHz and providing typically 25W of saturated output power associated to 28% of Power Added Efficiency at 25V drain voltage. It exhibits 8W of linear power with -25dBc IMD3. This HPA is dedicated to 5G and SatCom applications and well suited for a wide range of microwave applications and systems. The circuit is manufactured on a robust GaN-on-SiC HEMT process and is available in bare die form with mechanical protection. Input and output are 50Ω matched. The drain bias range, from 18V to 25V, offers a saturated output power from 15W to 25W.



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Electrical Characteristics

Tb = 25°C, Vd = 25V, Idq = 340mA, CW mode (Tb: Die backside temperature)

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	25		29	GHz
Gain	Linear gain		27		dB
Pout	Saturated output power		44		dBm
PAE	Power added efficiency		28		%
Id	Drain current at saturation		3.8		A
S11	Input return loss		-8		dB
S22	Output return loss		-8		dB
Idq	Quiescent current		340		mA
Vd	Drain voltage		25		V

These values are representative of on-board measurements. Measurement is de-embedded at the wire-bonding plane of the RF lines.

Absolute Maximum Ratings (1)

Tb = 25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	27	V
Idq	Quiescent drain current (without RF signal)	1000	mA
Vg	Gate bias voltage	-7 to -1.5	V
Pin	Maximum input power	30	dBm

(1) Operation of this device above anyone of these parameters may cause permanent damage.

Recommended Operating Range (2), (3)

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	18 to 25	V
Idq	Quiescent drain current (without RF signal)	300 to 700	mA
Vg	Gate bias voltage	-5 to -2.5	V
Tj	Maximum junction temperature(4)	200	°C
Pin	Maximum input power	28	dBm

(2) Electrical performance is defined for specified test conditions.
(3) Electrical performance is not guaranteed over all recommended operating conditions.
(4) See Device Thermal Performance section.

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Temperature Range

Tb	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +150	°C

Typical Bias Conditions

Tb = 25°C

Symbol	Pad Number	Description	Values	Unit
Vg	4, 8, 12, 20, 24, 28	Gate voltage	-3	V
Vd	6, 10, 14, 18, 22, 26	Drain voltage	25	V

“Power ON” Sequence

1. Bias HPA gate voltage at Vg close to Vpinch-off (Typically: Vg ≈ -5V)
2. Apply Vd bias voltage (Typically: Vd = 25V)
3. Increase gate voltage Vg up to quiescent bias drain current Idq
4. Apply RF signal

“Power OFF” Sequence

1. Turn off RF signal
2. Bias HPA gate voltage at Vg close to Vpinch-off (Typically: Vg ≈ -5V)
3. Check that quiescent bias drain current Idq is close to 0mA
4. Turn Vd bias voltage to 0V
5. Check that quiescent bias drain current Idq is close to 0mA
6. Turn Vg bias voltage to 0V

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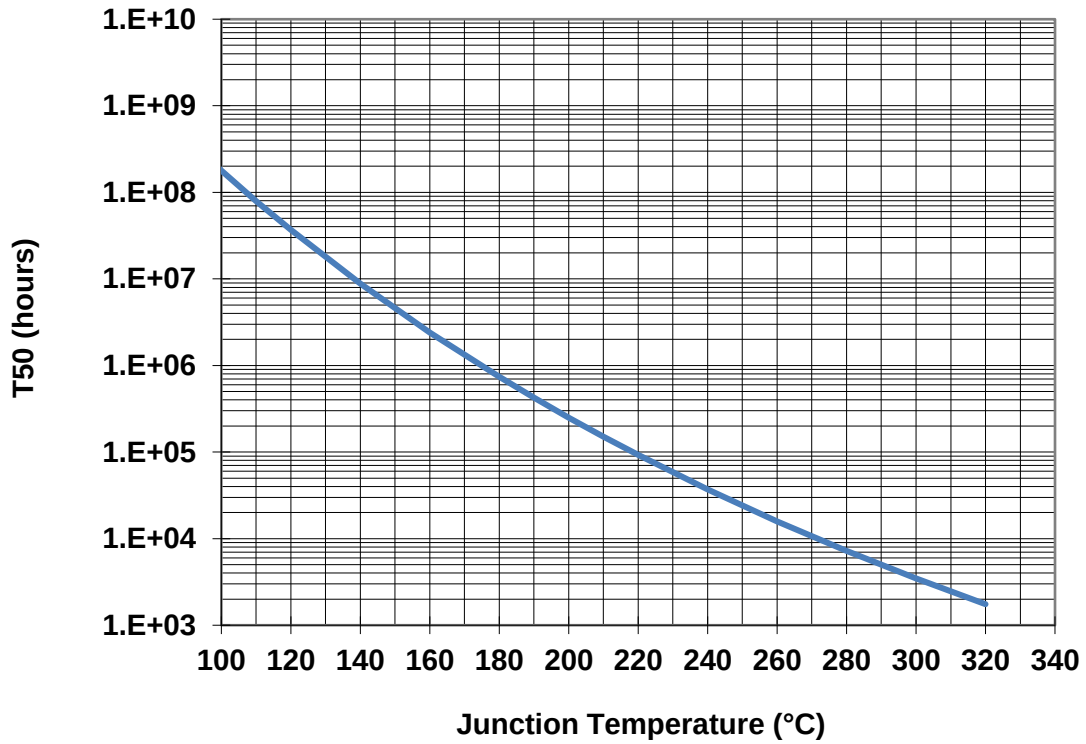
Device Thermal Performance

The device thermal performance below is based on UMS rules to evaluate the junction temperature. This same procedure is the basis for junction temperature evaluation of the samples used to derive the median lifetime and activation energy for the particular technology on which the CHA8682-98F is manufactured. The temperature Tb is defined as the die backside temperature. The thermal resistance (Rth), given in the following table, is for the full circuit in CW mode.

Parameter	Conditions	Tjunction (°C)	Rth (°C/W)	T50 (hours)
Rth[1] Thermal Resistance (Junction to die backside)	Vd = 20V Idq = 340mA Pout = 42.5dBm Pdiss = 51.1W	157	1.41	3.0E+06
	Vd = 25V Idq = 340mA Pout = 44dBm Pdiss = 69.0W	190	1.51	4.4E+05

[1] Assuming Tb = 85°C



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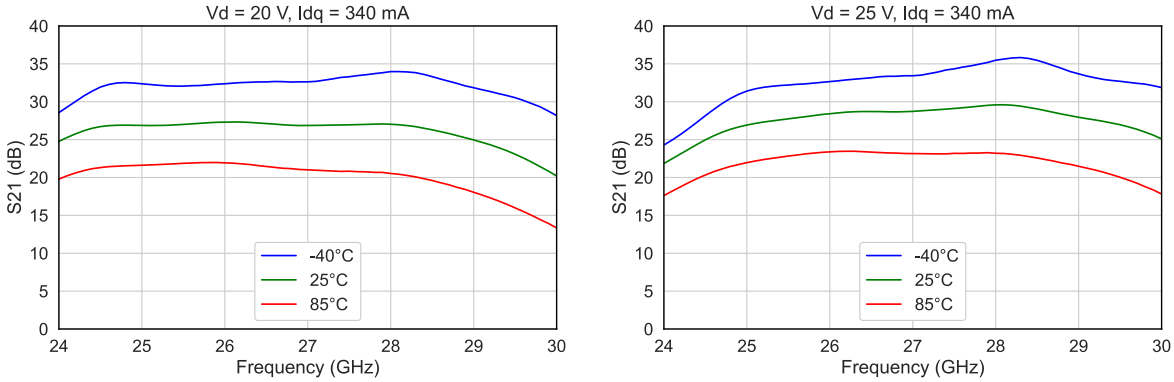
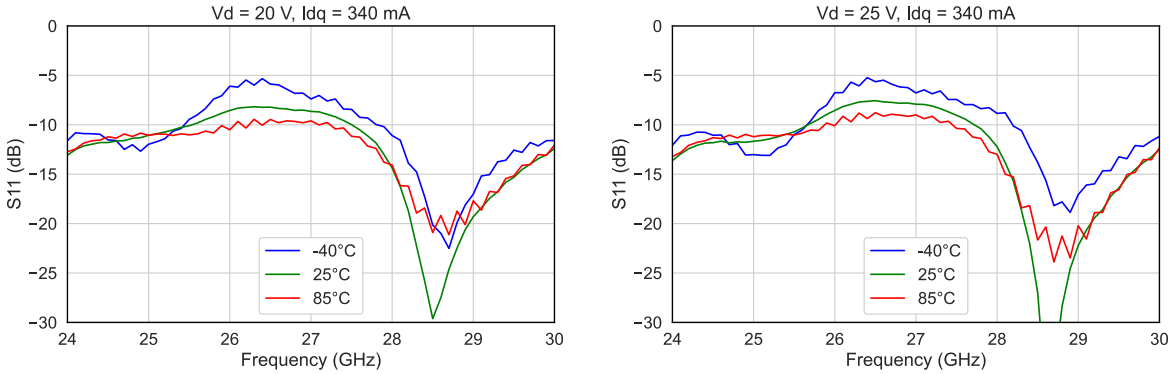
Typical Board Measurements: Small Signal Performance

Test conditions: CW, Vd = 20V / 25V, Idq = 340mA, Tb = -40°C / 25°C / 85°C
Measurement reference is at the connector plane for S11 and S22, and de-embedded at the wire-bonding plane of the RF lines for S21.

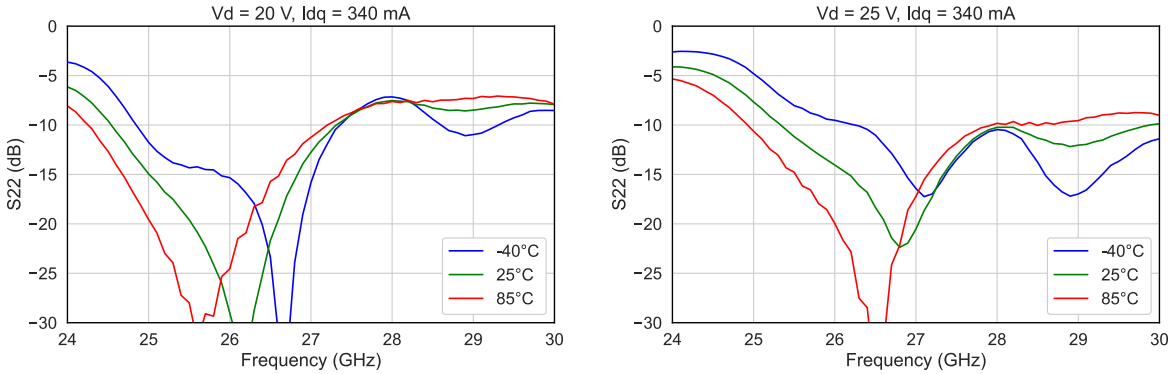
Linear Gain vs. Frequency vs. Temperature



Input Return Loss vs. Frequency vs. Temperature



Output Return Loss vs. Frequency vs. Temperature



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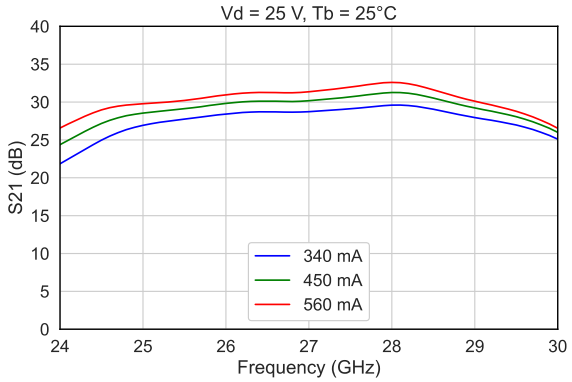
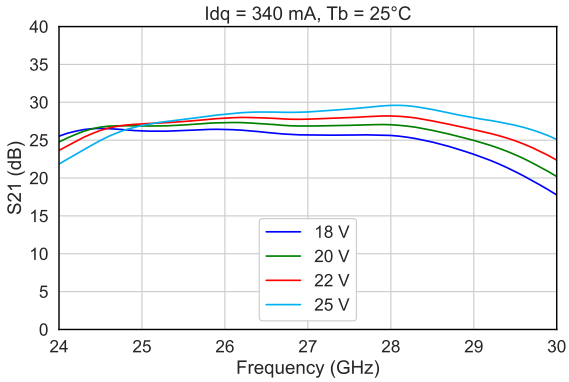
Typical Board Measurements: Small Signal Performance

Test conditions: CW, Tb = 25°C
Measurement reference is at the connector plane for S11 and S22, and de-embedded at the wire-bonding plane of the RF lines for S21.

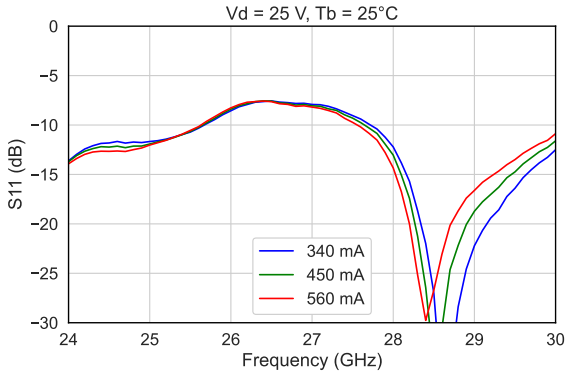
Linear Gain vs. Frequency vs. Idq



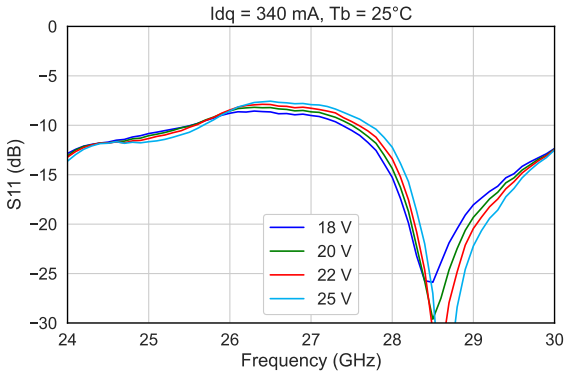
Linear Gain vs. Frequency vs. Vd



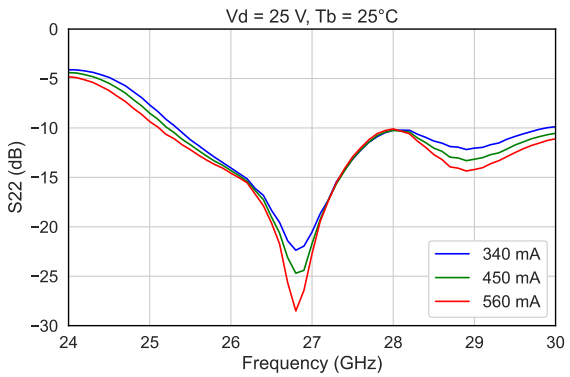
Input Return Loss vs. Frequency vs. Idq



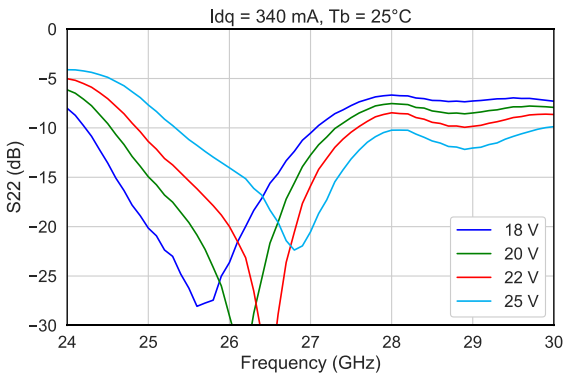
Input Return Loss vs. Frequency vs. Vd



Output Return Loss vs. Freq vs. Idq



Output Return Loss vs. Frequency vs. Vd



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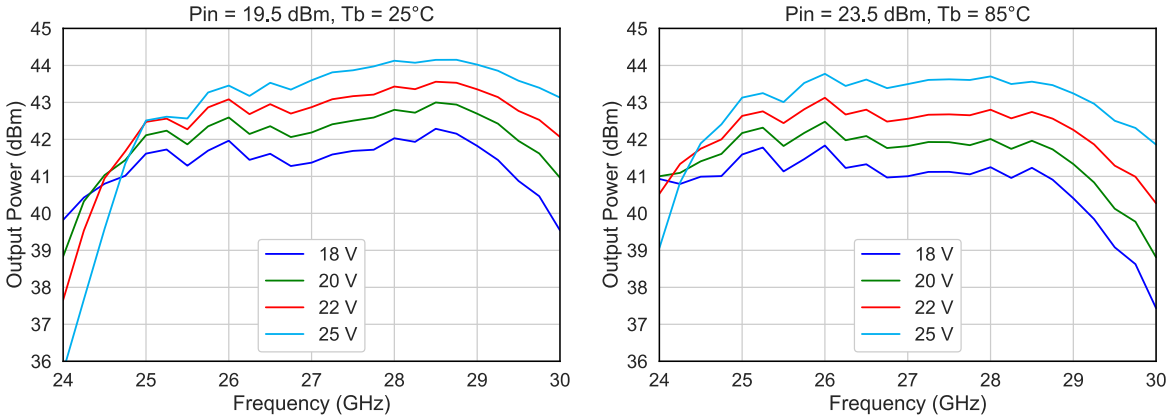
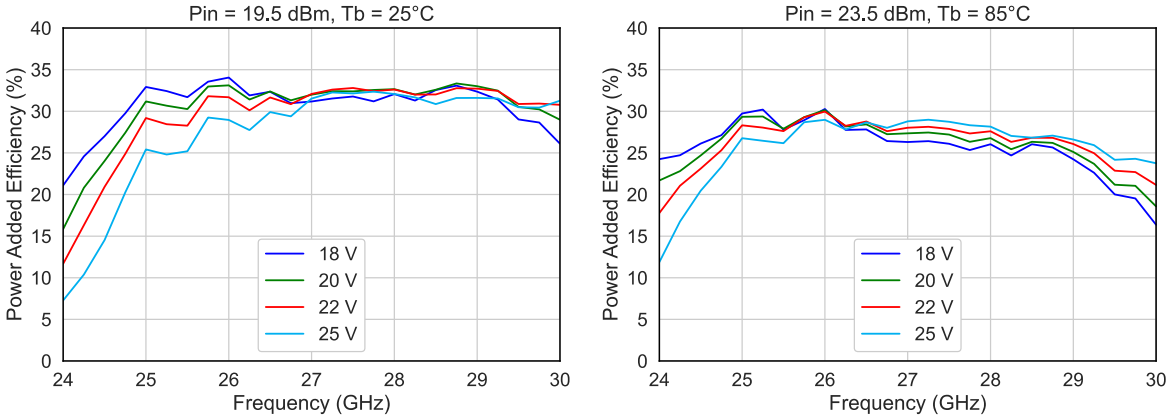
Typical Board Measurements: Large Signal Performance

Test conditions: CW, Idq = 340mA, Tb = 25°C / 85°C
Measurement reference plane is de-embedded at the wire-bonding plane of the RF lines.

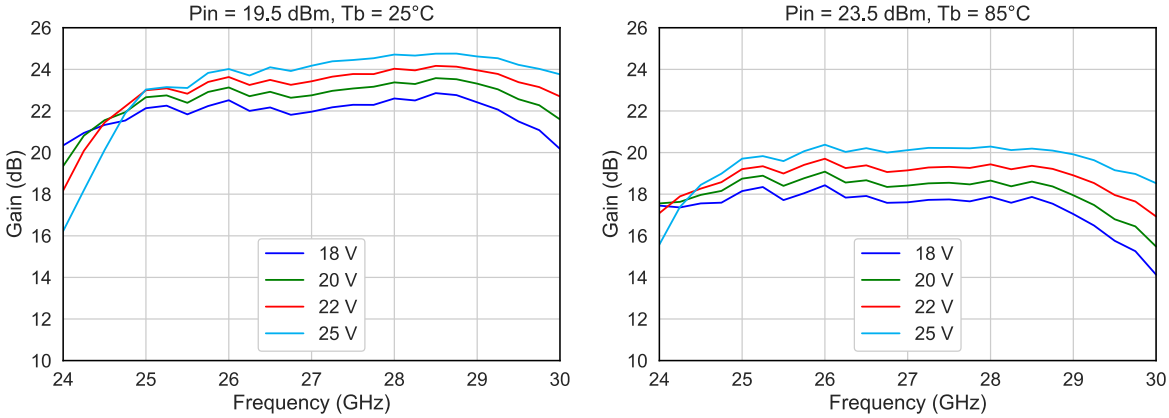
Output Power vs. Frequency vs. Drain Voltage



Power Added Efficiency vs. Frequency vs. Drain Voltage



Gain vs. Frequency vs. Drain Voltage



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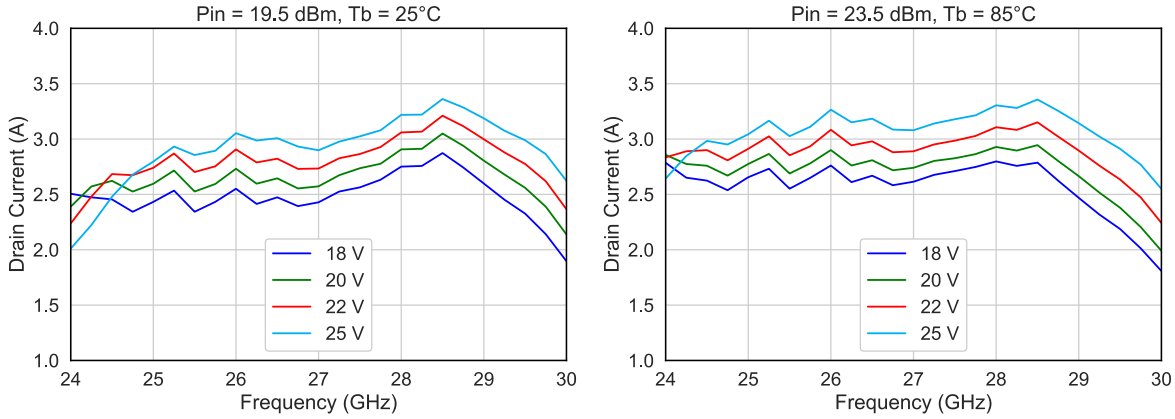
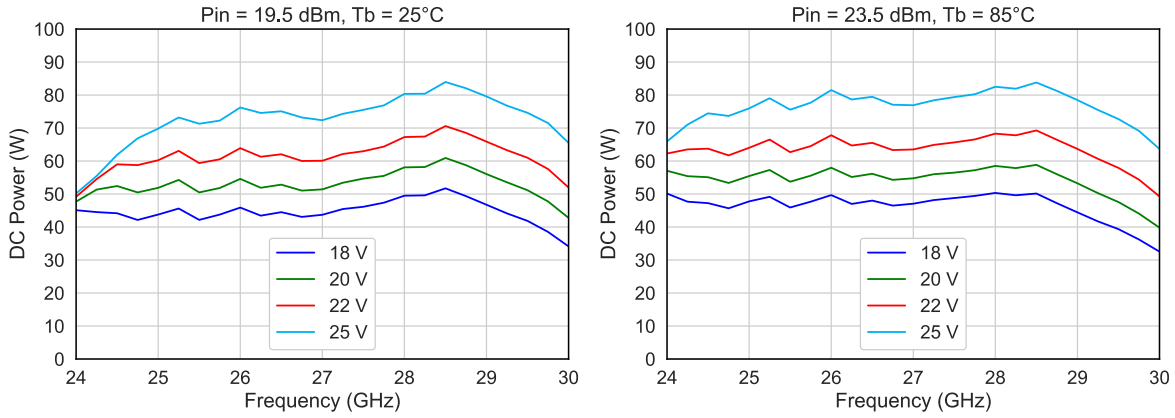
Typical Board Measurements: Large Signal Performance

Test conditions: CW, Idq = 340mA, Tb = 25°C / 85°C
Measurement reference plane is de-embedded at the wire-bonding plane of the RF lines.

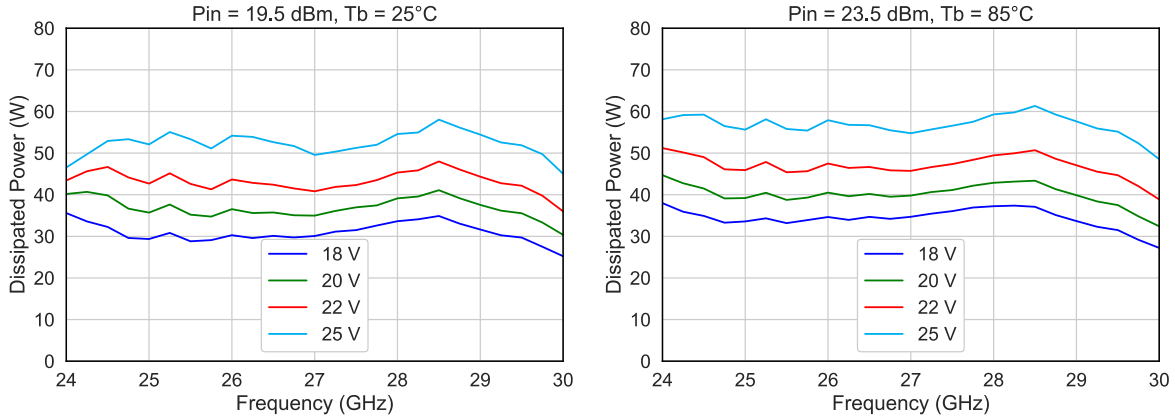
Drain Current vs. Frequency vs. Drain Voltage



DC Power Consumption vs. Frequency vs. Drain Voltage



Dissipated Power vs. Frequency vs. Drain Voltage



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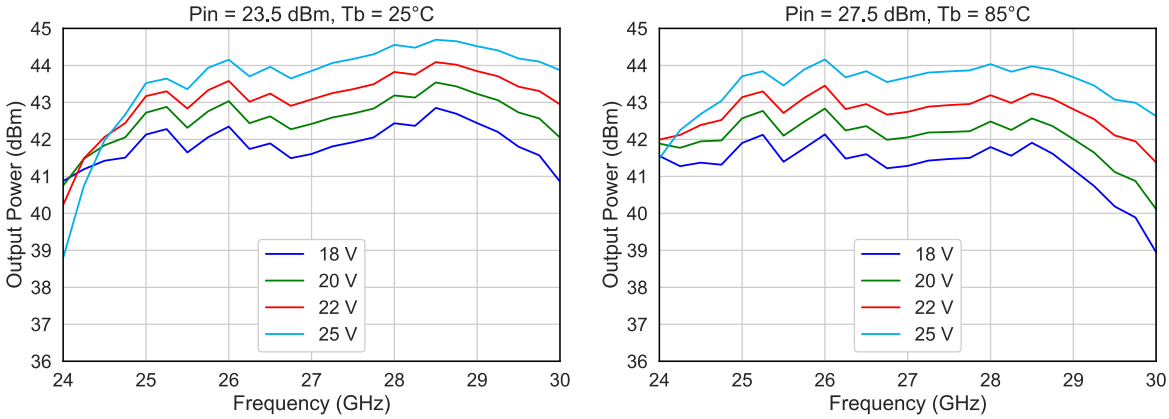
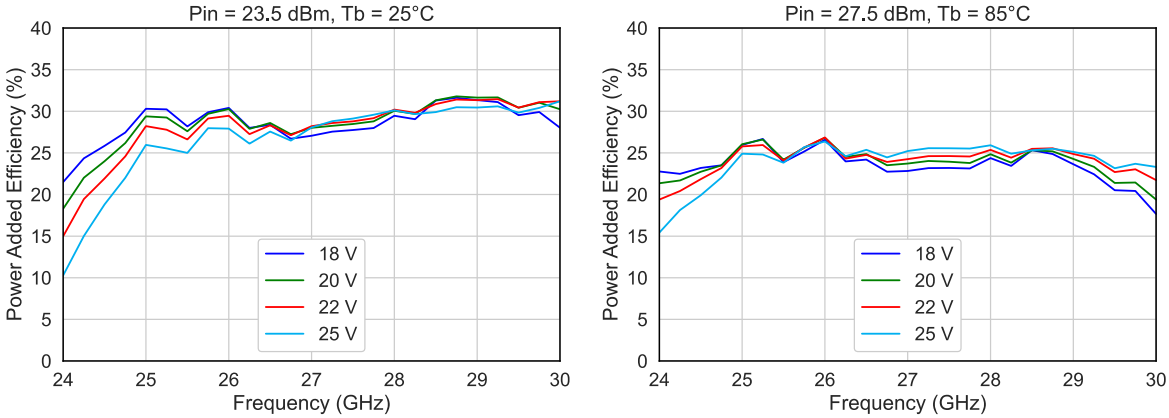
Typical Board Measurements: Large Signal Performance

Test conditions: CW, Idq = 340mA, Tb = 25°C / 85°C
Measurement reference plane is de-embedded at the wire-bonding plane of the RF lines.

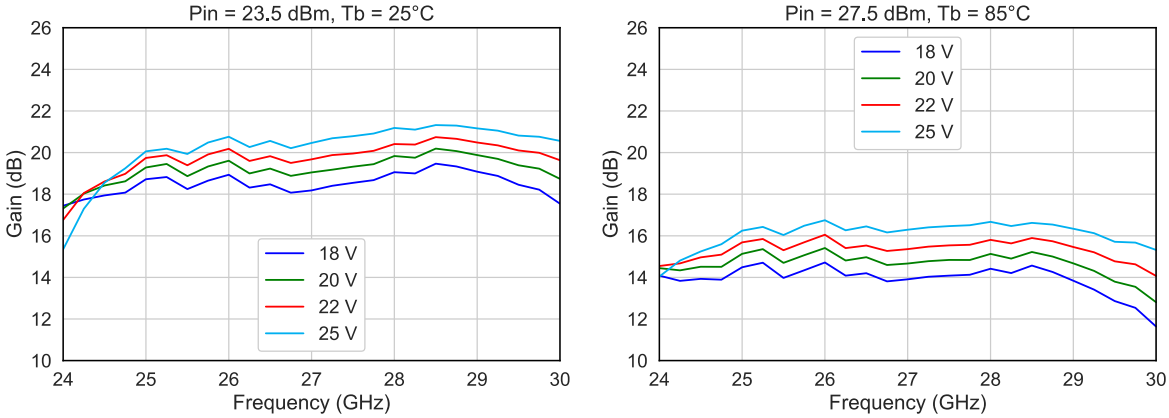
Output Power vs. Frequency vs. Drain Voltage



Power Added Efficiency vs. Frequency vs. Drain Voltage



Gain vs. Frequency vs. Drain Voltage



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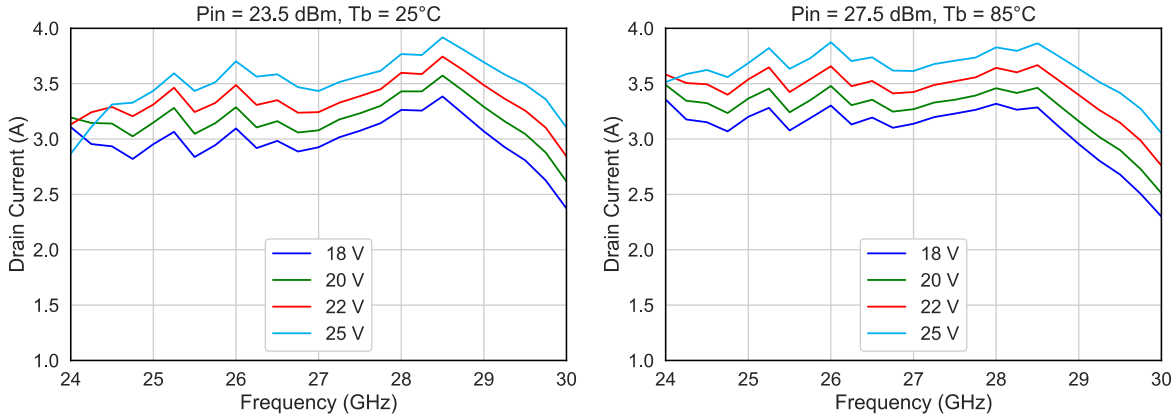
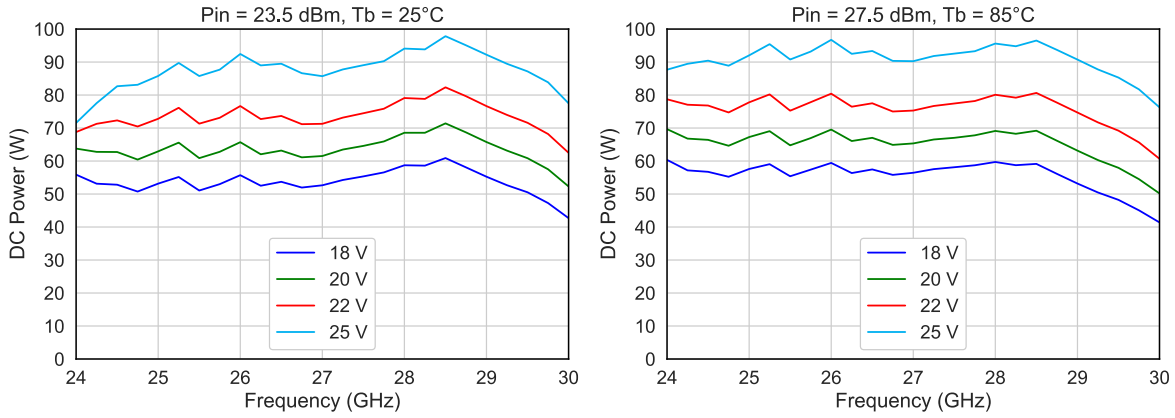
Typical Board Measurements: Large Signal Performance

Test conditions: CW, Idq = 340mA, Tb = 25°C / 85°C
Measurement reference plane is de-embedded at the wire-bonding plane of the RF lines.

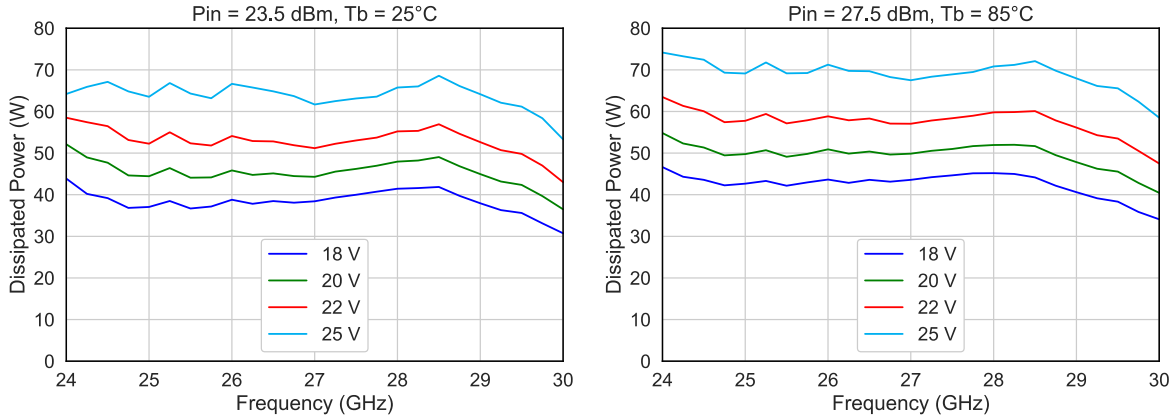
Drain Current vs. Frequency vs. Drain Voltage



DC Power Consumption vs. Frequency vs. Drain Voltage



Dissipated Power vs. Frequency vs. Drain Voltage



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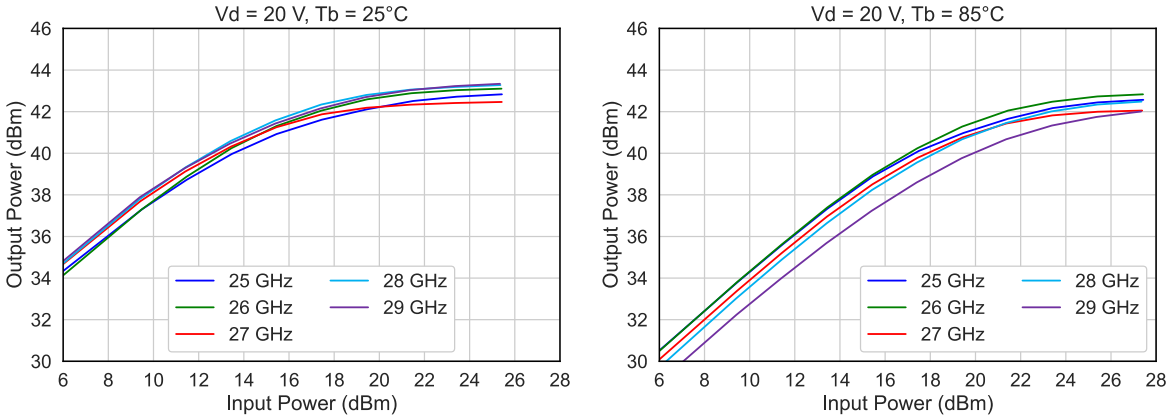
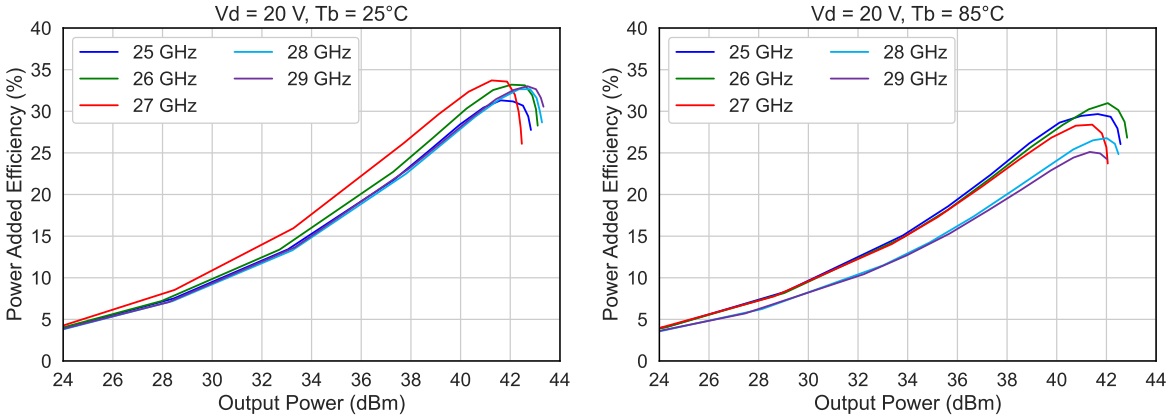
Typical Board Measurements: Large Signal Performance

Test conditions: CW, Vd = 20V, Idq = 340mA, Tb = 25°C / 85°C
Measurement reference plane is de-embedded at the wire-bonding plane of the RF lines.

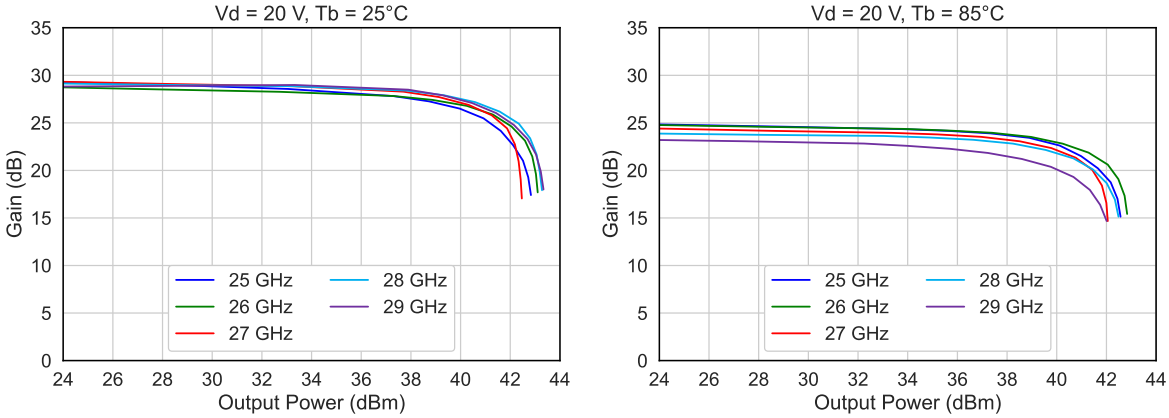
Output Power vs. Input Power vs. Frequency



Power Added Efficiency vs. Output Power vs. Frequency



Gain vs. Output Power vs. Frequency



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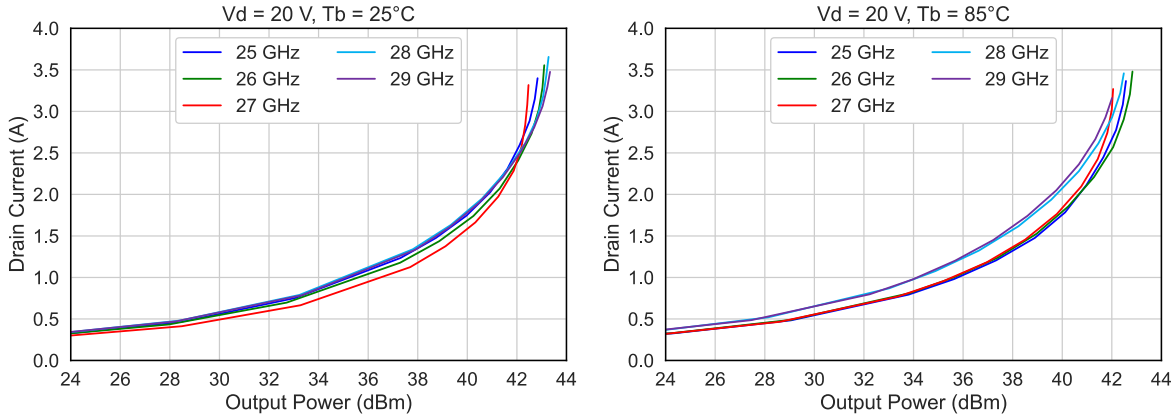
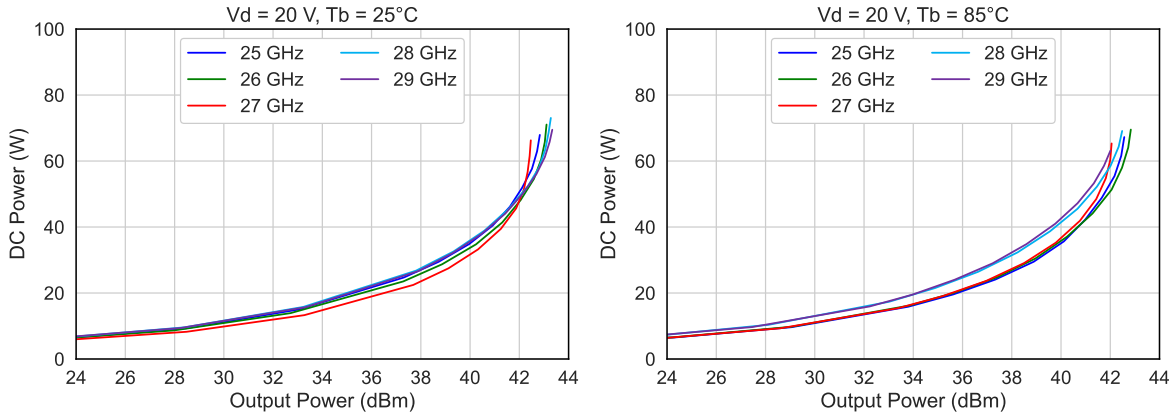
Typical Board Measurements: Large Signal Performance

Test conditions: CW, Vd = 20V, Idq = 340mA, Tb = 25°C / 85°C
Measurement reference plane is de-embedded at the wire-bonding plane of the RF lines.

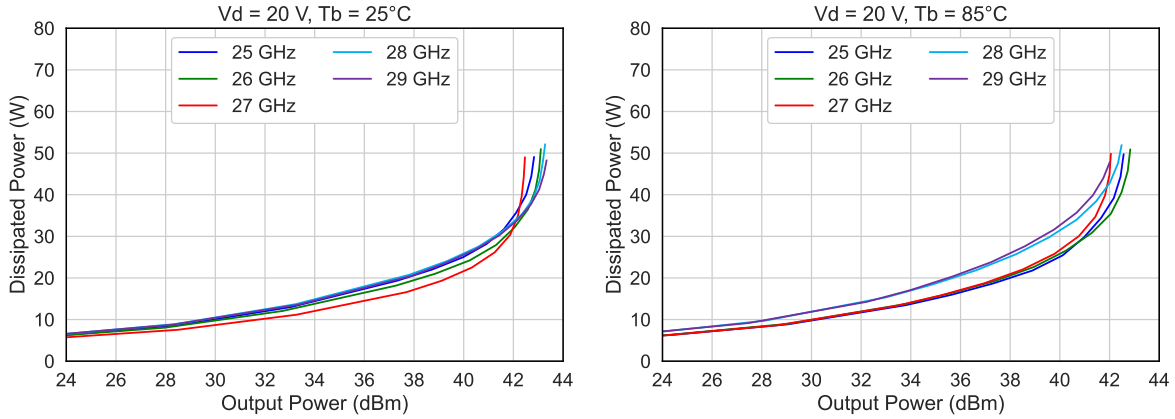
Drain Current vs. Output Power vs. Frequency



DC Power Consumption vs. Output Power vs. Frequency



Dissipated Power vs. Output Power vs. Frequency



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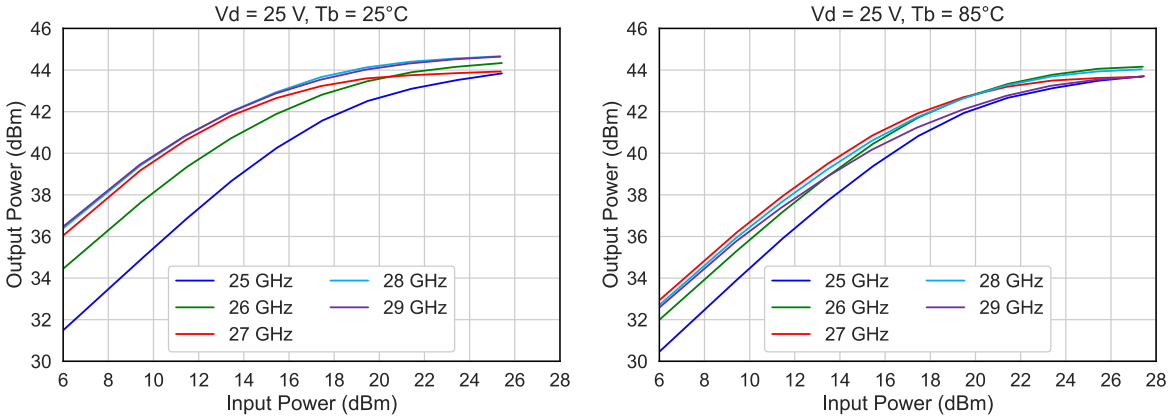
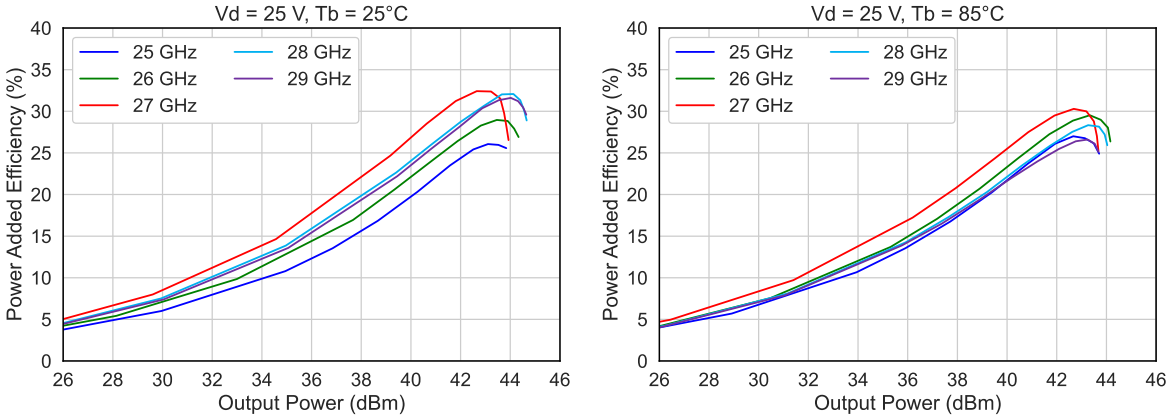
Typical Board Measurements: Large Signal Performance

Test conditions: CW, Vd = 25V, Idq = 340mA, Tb = 25°C / 85°C
Measurement reference plane is de-embedded at the wire-bonding plane of the RF lines.

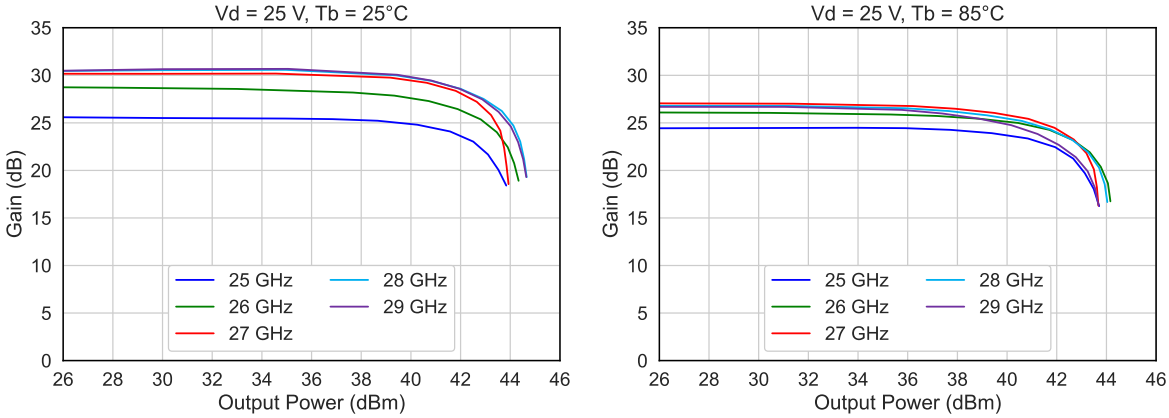
Output Power vs. Input Power vs. Frequency



Power Added Efficiency vs. Output Power vs. Frequency



Gain vs. Output Power vs. Frequency



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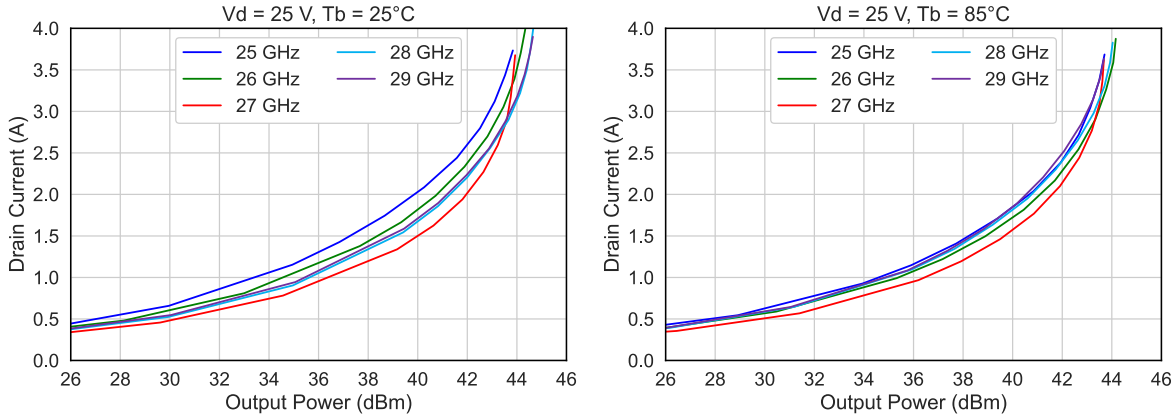
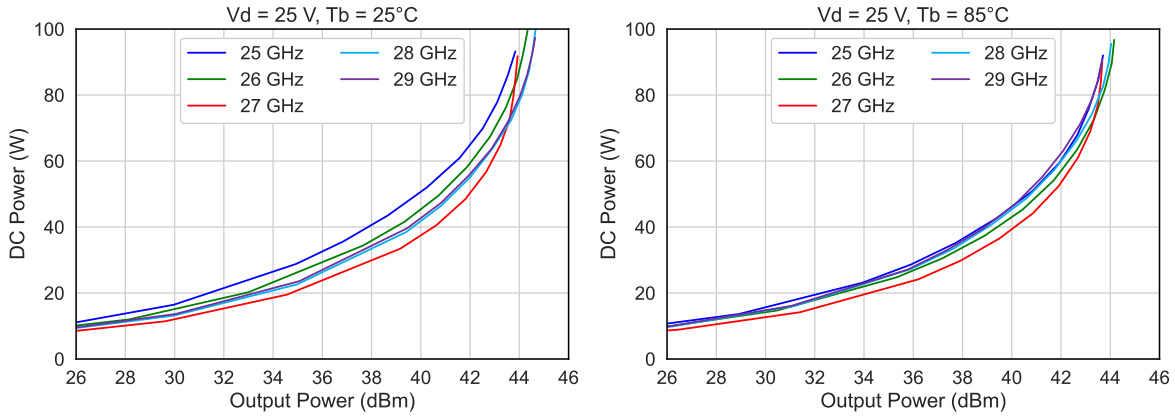
Typical Board Measurements: Large Signal Performance

Test conditions: CW, Vd = 25V, Idq = 340mA, Tb = 25°C / 85°C
Measurement reference plane is de-embedded at the wire-bonding plane of the RF lines.

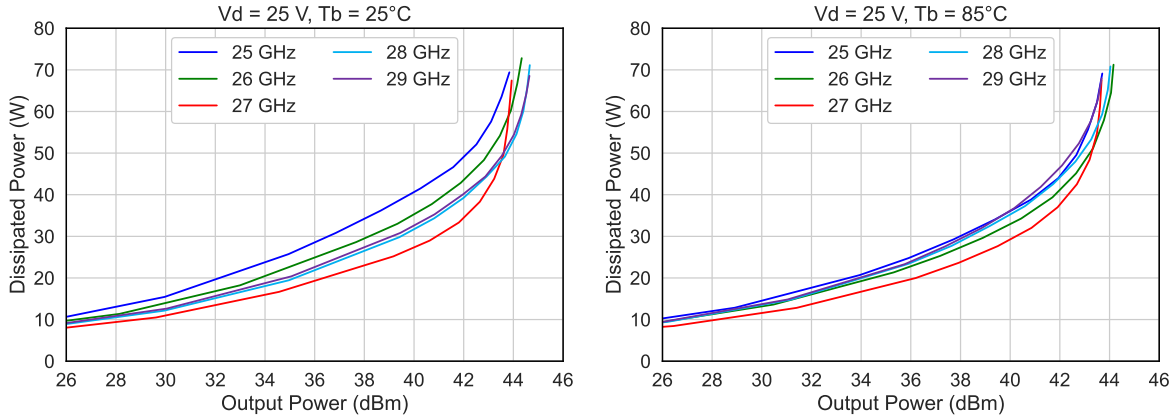
Drain Current vs. Output Power vs. Frequency



DC Power Consumption vs. Output Power vs. Frequency



Dissipated Power vs. Output Power vs. Frequency



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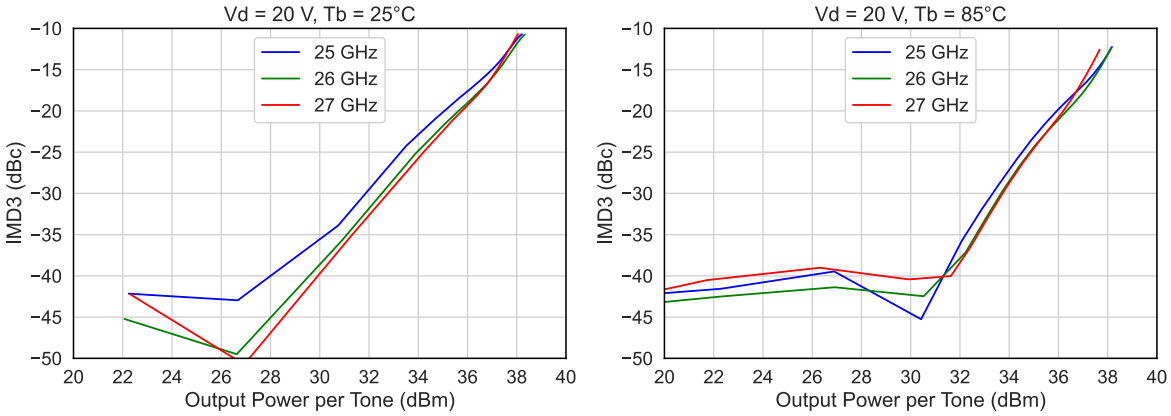
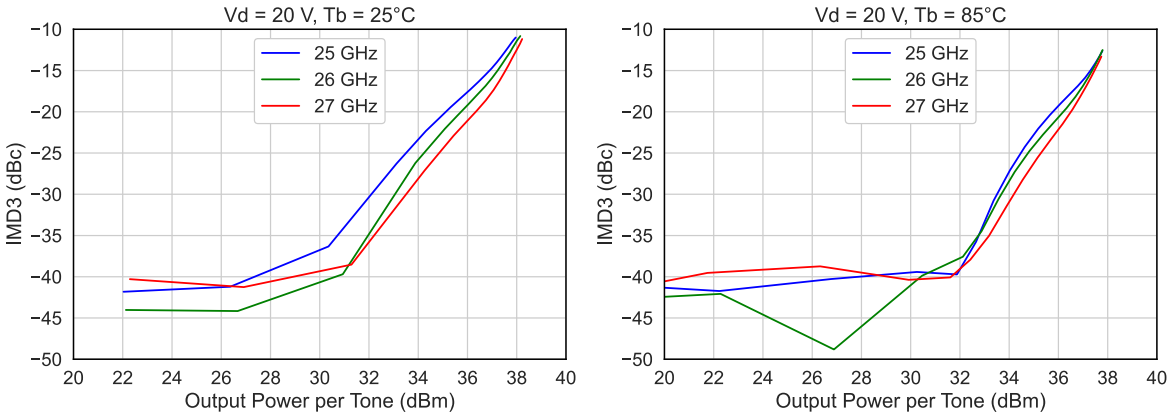
Typical Board Measurements: Intermodulation Distortion

Test conditions: CW, Vd = 20V, Idq = 340mA, Tb = 25°C / 85°C
Measurement reference plane is de-embedded at the wire-bonding plane of the RF lines.

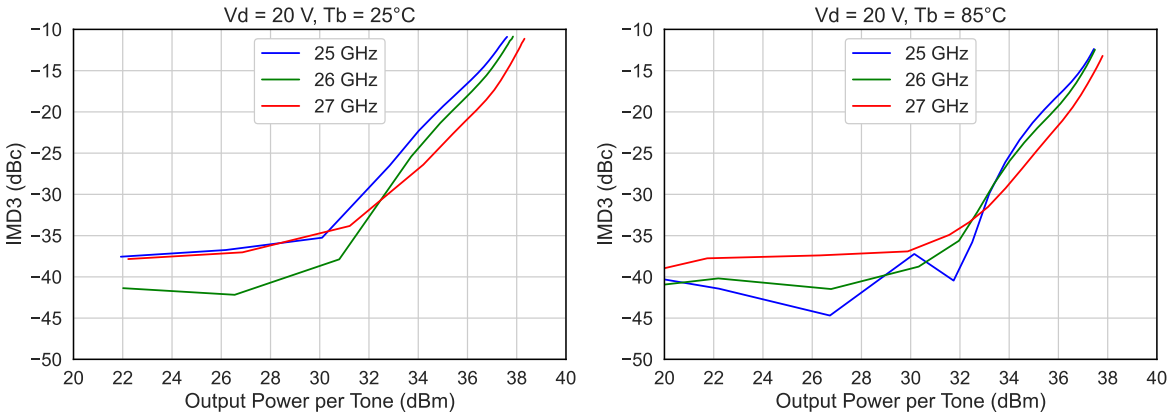
IMD3 at 10MHz Tone Separation vs. Output Power per Tone vs. Frequency



IMD3 at 100MHz Tone Separation vs. Output Power per Tone vs. Frequency



IMD3 at 200MHz Tone Separation vs. Output Power per Tone vs. Frequency



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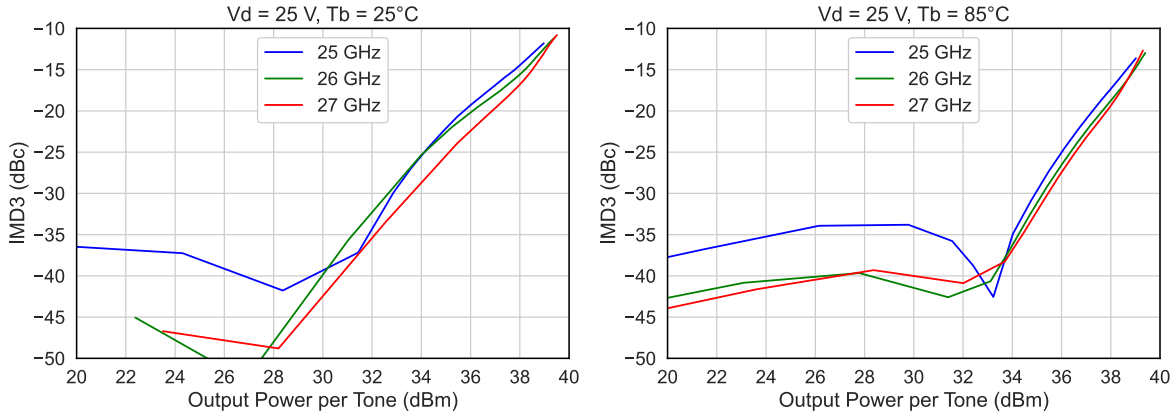
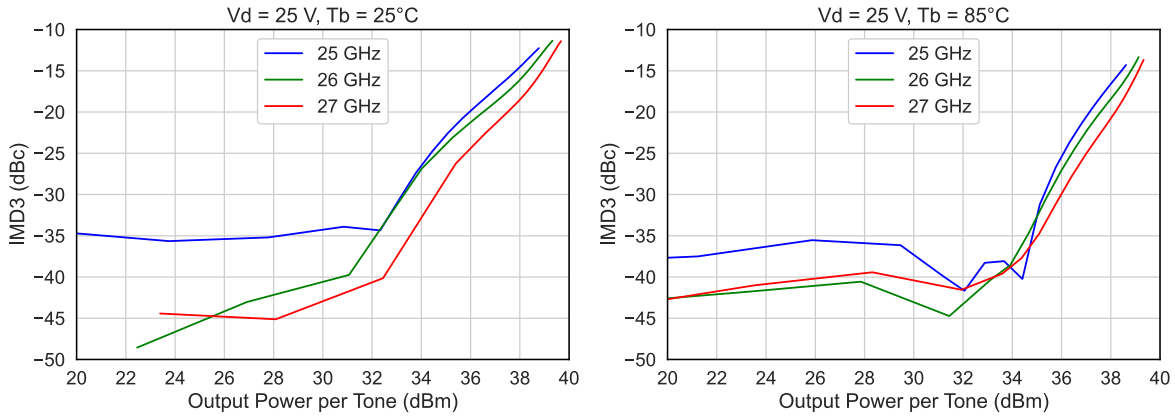
Typical Board Measurements: Intermodulation Distortion

Test conditions: CW, Vd = 25V, Idq = 340mA, Tb = 25°C / 85°C
Measurement reference plane is de-embedded at the wire-bonding plane of the RF lines.

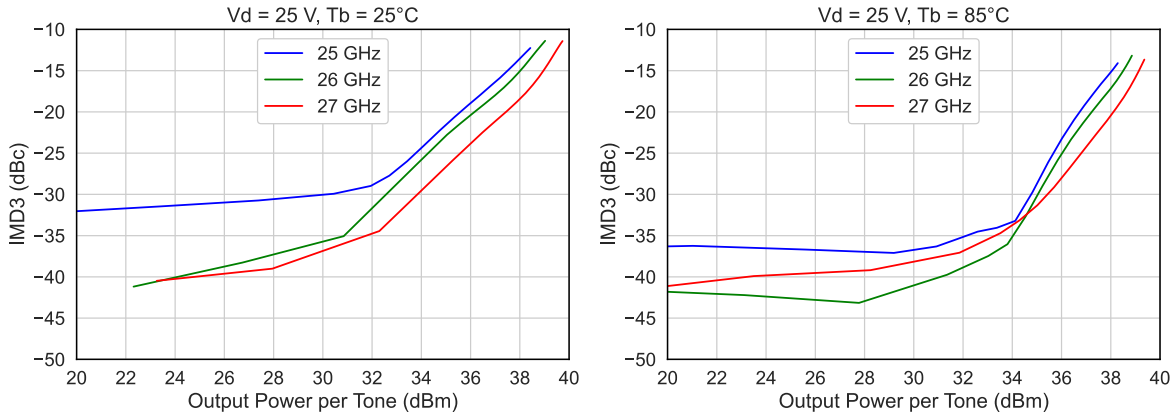
IMD3 at 10MHz Tone Separation vs. Output Power per Tone vs. Frequency



IMD3 at 100MHz Tone Separation vs. Output Power per Tone vs. Frequency



IMD3 at 200MHz Tone Separation vs. Output Power per Tone vs. Frequency



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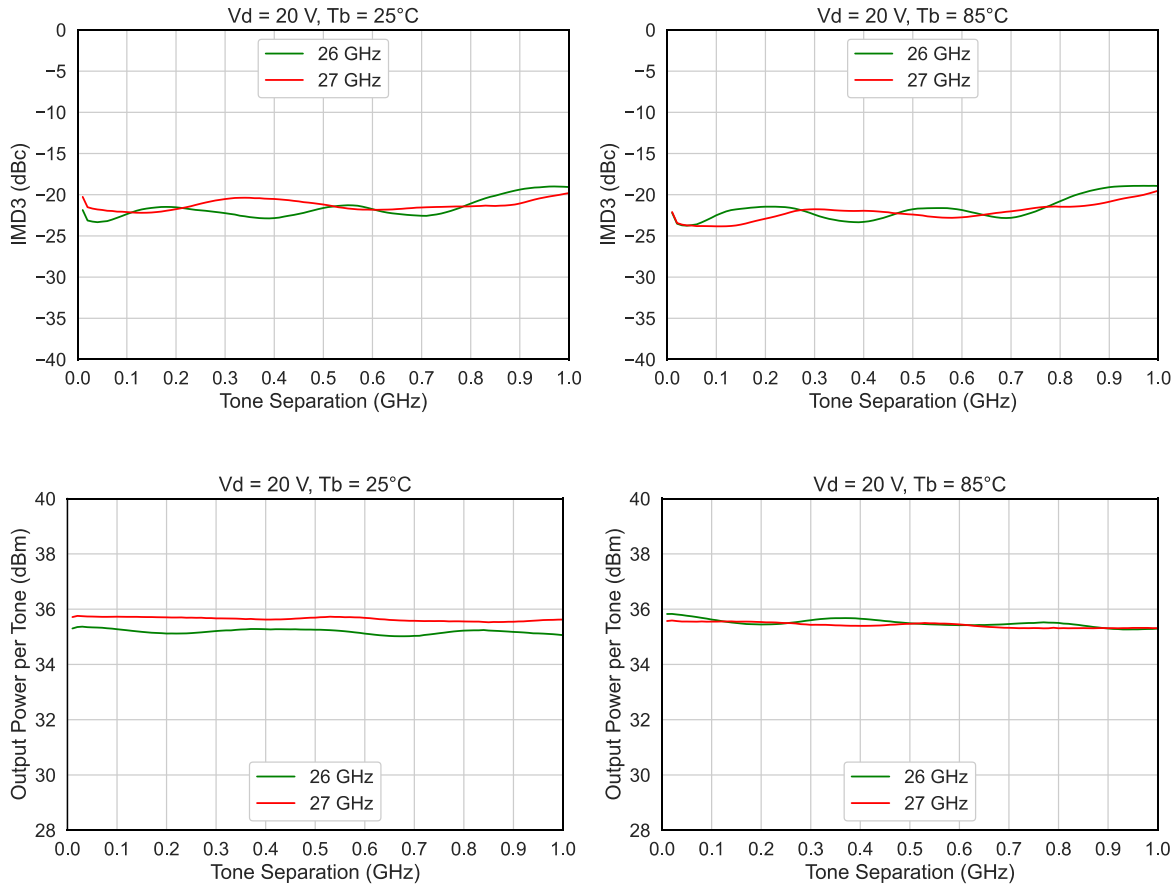
Typical Board Measurements: Intermodulation Distortion

Test conditions: CW, Vd = 20V, Idq = 340mA, Tb = 25°C / 85°C
Measurement reference plane is de-embedded at the wire-bonding plane of the RF lines.

IMD3 with associated Output Power per Tone vs. Tone Separation vs. Frequency



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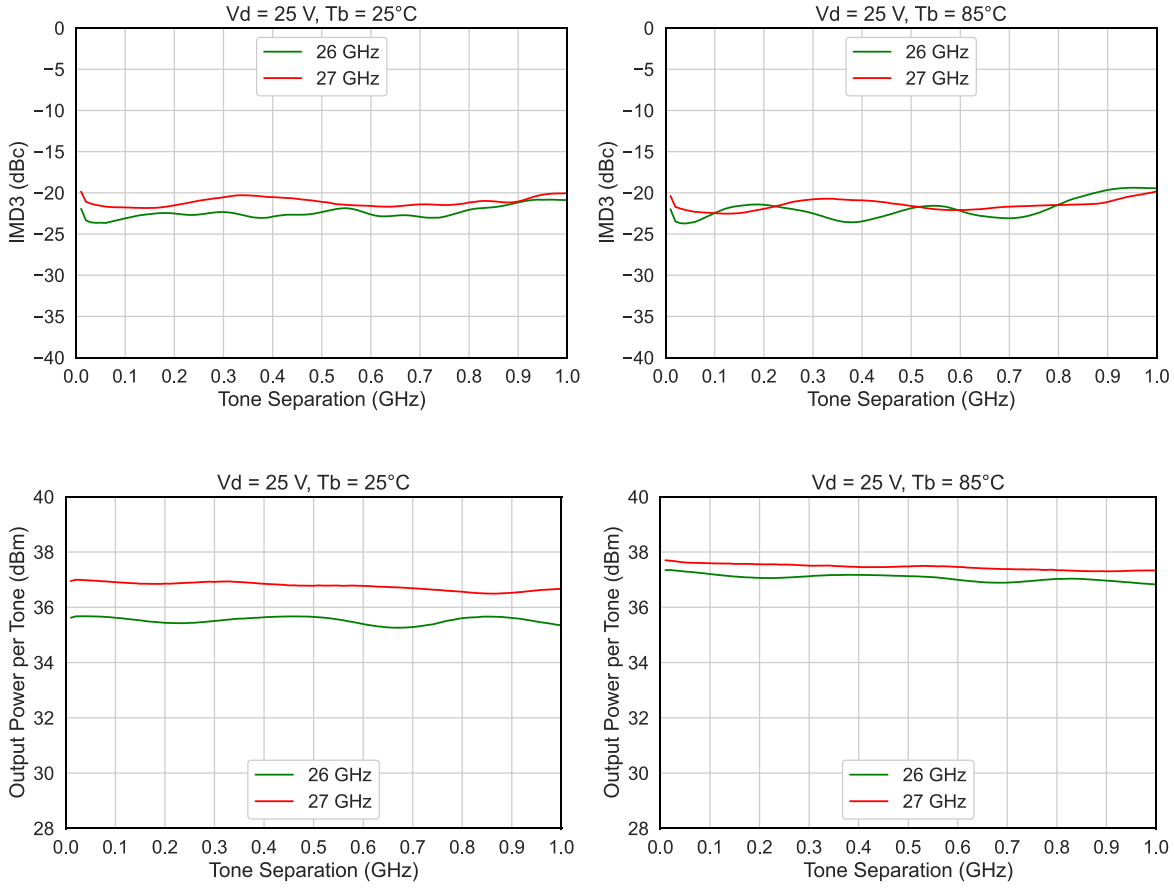
Typical Board Measurements: Intermodulation Distortion

Test conditions: CW, Vd = 25V, Idq = 340mA, Tb = 25°C / 85°C
Measurement reference plane is de-embedded at the wire-bonding plane of the RF lines.

IMD3 with associated Output Power per Tone vs. Tone Separation vs. Frequency



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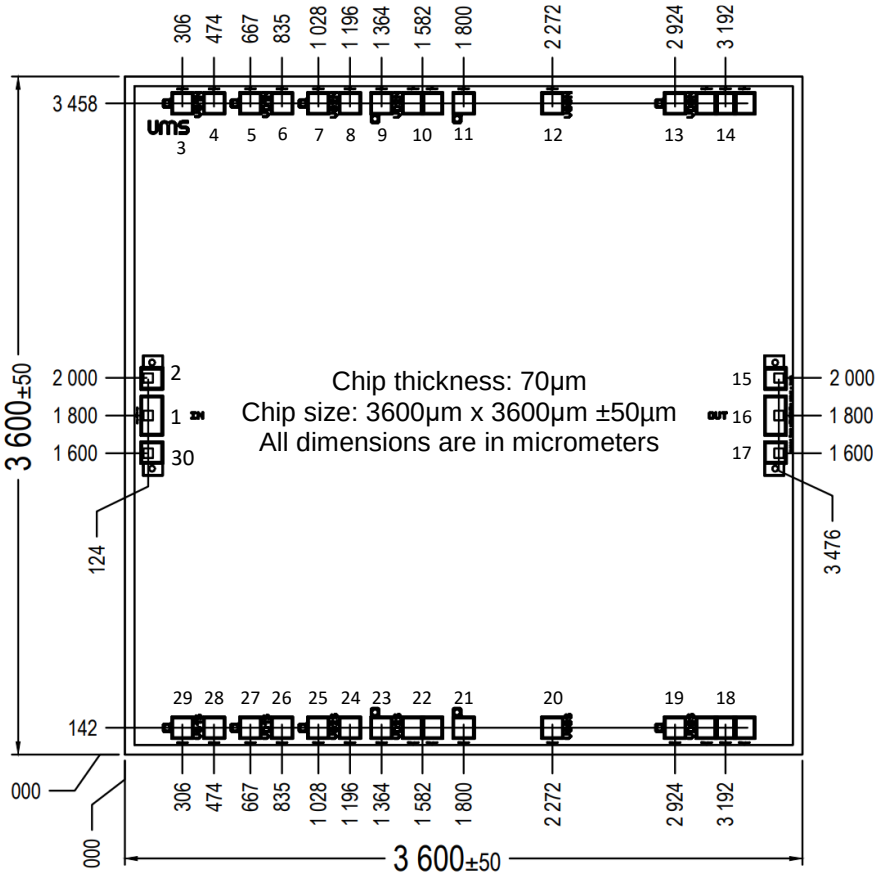
Mechanical data



Pad Number	Name	Description	Pad Opening Size
1	RF IN	Input RF port	194µm x 102µm
4	VG1N	DC Gate voltage, 1st stage, North	100µm x 100µm
6	VD1N	DC Drain voltage 1st stage, North	100µm x 100µm
8	VG2N	DC Gate voltage 2nd stage, North	100µm x 100µm
10	VD2N	DC Drain voltage, 2nd stage, North	200µm x 100µm
12	VG3N	DC Gate voltage 3rd stage, North	100µm x 100µm
14	VD3N	DC Drain voltage 3rd stage, North	300µm x 100µm
16	RF OUT	Output RF port	194µm x 102µm
18	VD3S	DC Drain voltage 3rd stage, South	300µm x 100µm
20	VG3S	DC Gate voltage 3rd stage, South	100µm x 100µm
22	VD2S	DC Drain voltage, 2nd stage, South	200µm x 100µm
24	VG2S	DC Gate voltage 2nd stage, South	100µm x 100µm
26	VD1S	DC Drain voltage 1st stage, South	100µm x 100µm
28	VG1S	DC Gate voltage, 1st stage, South	100µm x 100µm
2, 3, 5, 7, 9, 11, 13, 15, 17, 19, 21, 23, 25, 27, 29, 30	GND	Ground	100µm x 100µm

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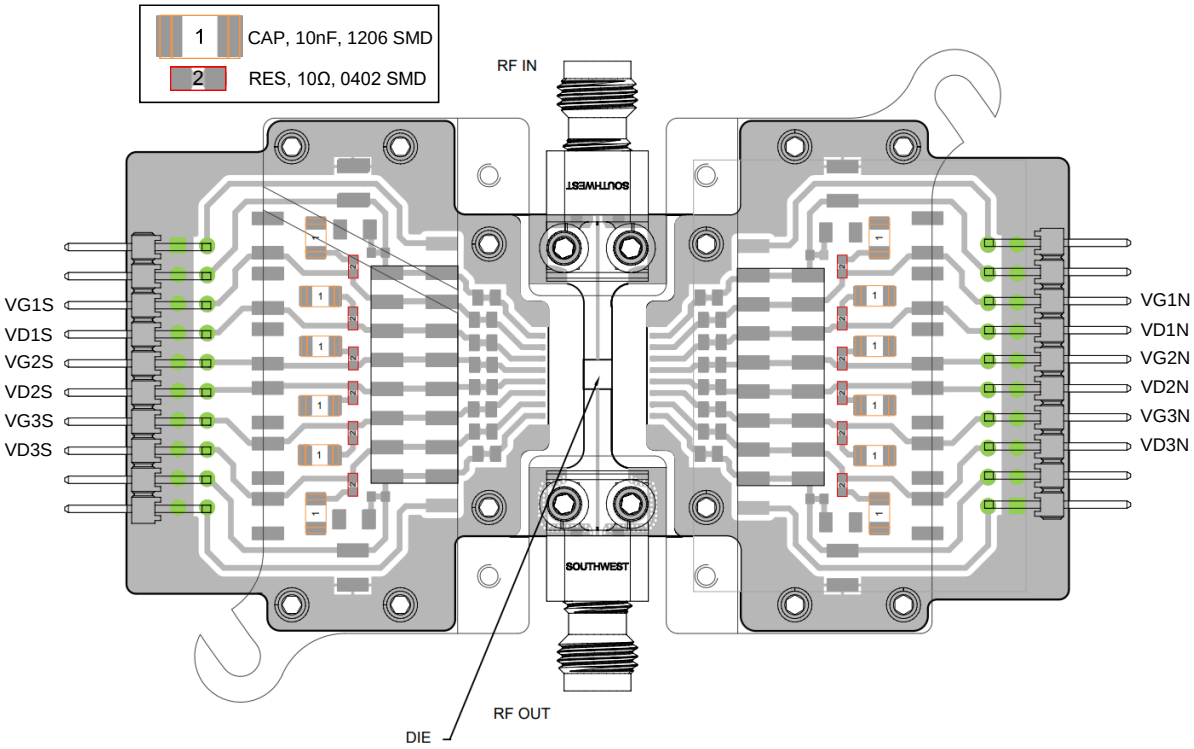
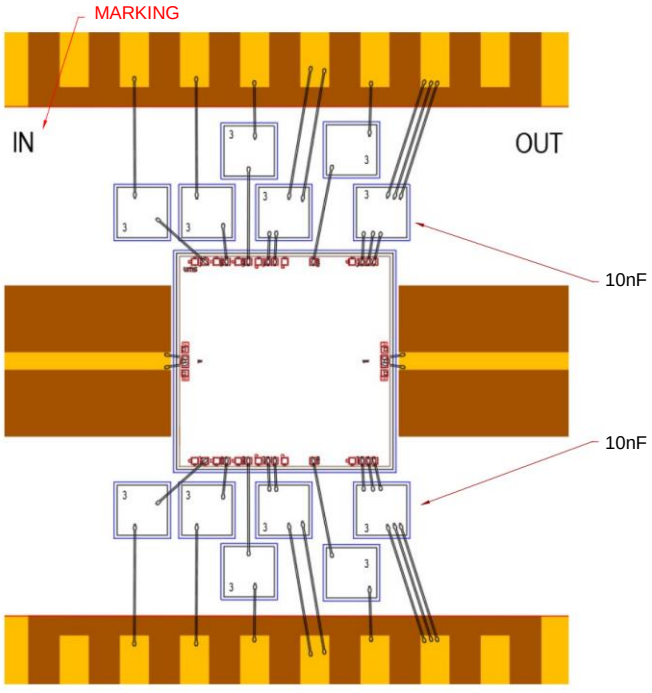
Recommended Assembly Plan





Two levels of decoupling capacitors are recommended, one on the tab and the other on the PCB. The first level is composed of 10nF chip capacitors, the second level is composed of 1µF SMD capacitors with 10Ω SMD series resistance. The first level should be as close as possible to the die.

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Recommended reflow process assembly

Refer to the application note AN0001 available at http://www.ums-rf.com for die attach.

Evaluation Board (EVB)

Refer to the application note AN0030 available at http://www.ums-rf.com for information and recommendations related to the evaluation board.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at http://www.ums-rf.com.

Recommended ESD management

Refer to the application note AN0020 available at http://www.ums-rf.com for ESD sensitivity and handling recommendations for the UMS products.

Maturity Level

Maturity Level	Product status	Documentation	Reliability	Usage in a system
Lab Sample (LS)	Decision to develop the product is not confirmed	Technical Information	No commitment	Lab demonstrator
Engineering Sample (ES)	**Design may change**	**Advanced Information**	**The design is within the recommended temperature, current and voltage ranges as regards the technology used.**	**Engineering demonstrator**
Product Representative Unit (PRU)	Design is frozen	Data-sheet	Tests results are available on the foreseen product or on an similar one	Production

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Notes

Sampling request reference

Die: ES-CHA8682-98F/00
Demo board: EVB-CHA8682-98F

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