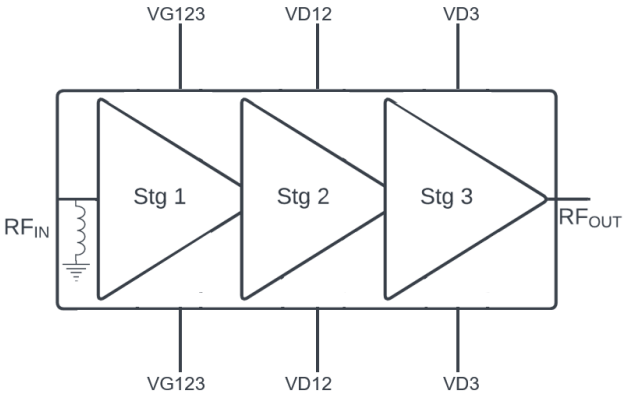
Advanced Information: AI2504

27.5-31GHz 10W Power Amplifier

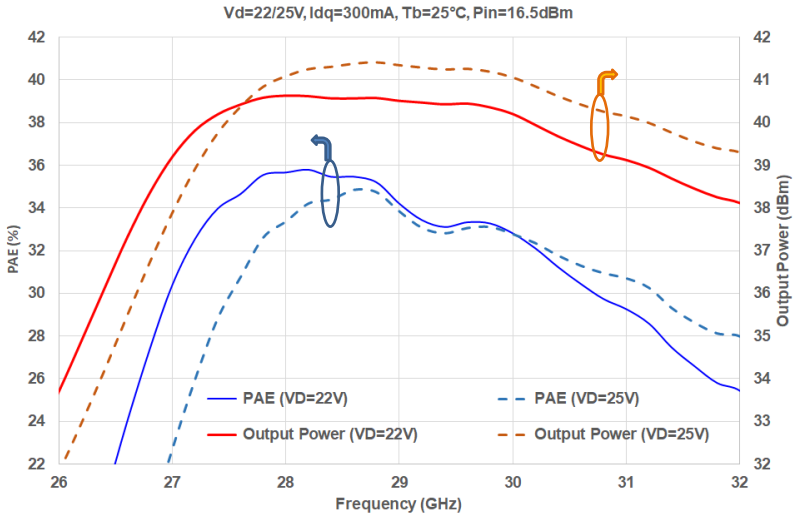
GaN Monolithic Microwave IC



The CHA8282-99F is a three-stage GaN High Power Amplifier in the frequency band 27.5-31GHz. This HPA typically provides 10W output power associated to 33% of Power Added Efficiency. The circuit exhibits a typical small signal gain of 27dB. The overall power supply is 22V/300mA.

The circuit is dedicated to Satcom and is also well suited for a wide range of microwave and millimetre wave applications and systems.

It is developed on a robust GaN-on-SiC HEMT process and will be available as a bare die. The input and output are matched to 50Ω and integrate ESD RF protection.



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Electrical Characteristics

Tbackside= +25°C, Vd = +22V

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	27.5		31	GHz
Gain	Linear Gain		27		dB
S_{11}(1)	Input return loss		12		dB
S_{22}(1)	Output return loss		12		dB
P_{sat}	Saturated output Power (Pin=16.5dBm)		40		dBm
PAE	Power Added Efficiency (Pin=16.5dBm)		33		%
Id	Drain current at saturation		1.5		A
Idq	Quiescent Current		300		mA
ACPR	ACPR at Pout = 36dBm with 8PSK (100MHz Modulation Bandwidth)		-30		dBc
EVM	EVM at Pout = 36dBm with 8PSK (100MHz Modulation Bandwidth)		4		%

These values are representative of on-board measurements as defined on the drawing in the Evaluation Board section.

(1) Input and Output Return Losses are given at Evaluation Board connectors' reference planes as defined in the Measurement Reference Planes section

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Absolute Maximum Ratings (1)

Tbackside= +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	27	V
Id	Drain bias current	2.3	A
Vg	Gate bias voltage	-7 to -2	V
Pin	Maximum input power	28	dBm

(1) Operation of this device above anyone of these parameters may cause permanent damage.

Recommended Operating Range (2), (3)

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	22 to 25	V
Idq	Quiescent drain current (without RF signal)	200 to 350	mA
Tj	Maximum Junction Temperature(4)	200	°C

(2) Electrical performances are defined for specified test conditions

(3) Electrical performances are not guaranteed over all recommended operating conditions

(4) See Device Thermal Performances section

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Temperature Range

Tbackside	Operating Temperature Range	-40 to +85	°C
Tstg	Storage Temperature Range	-55 to +150	°C

Typical Bias Conditions

Tbackside = 25°C

Symbol	Pin Number	Description	Values	Unit
Vg	3, 11	Gate Voltage	-3	V
Vd	4, 6, 8, 10	Drain Voltage	22	V

"Power ON" Sequence

1. Bias HPA gate voltage at Vg close to Vpinch-off (Typically: Vg ≈ -5V)
2. Apply Vd bias voltage (Typically: Vd = 22V)
3. Increase gate voltage Vg up to quiescent bias drain current Idq
4. Apply RF signal

"Power OFF" Sequence

1. Turn off RF signal
2. Bias HPA gate voltage at Vg close to Vpinch-off (Typically: Vg ≈ -5V)
3. Check that quiescent bias drain current Idq is close to 0mA
4. Turn Vd bias voltage to 0V
5. Check that quiescent bias drain current Idq is close to 0mA
6. Turn Vg bias voltage to 0V

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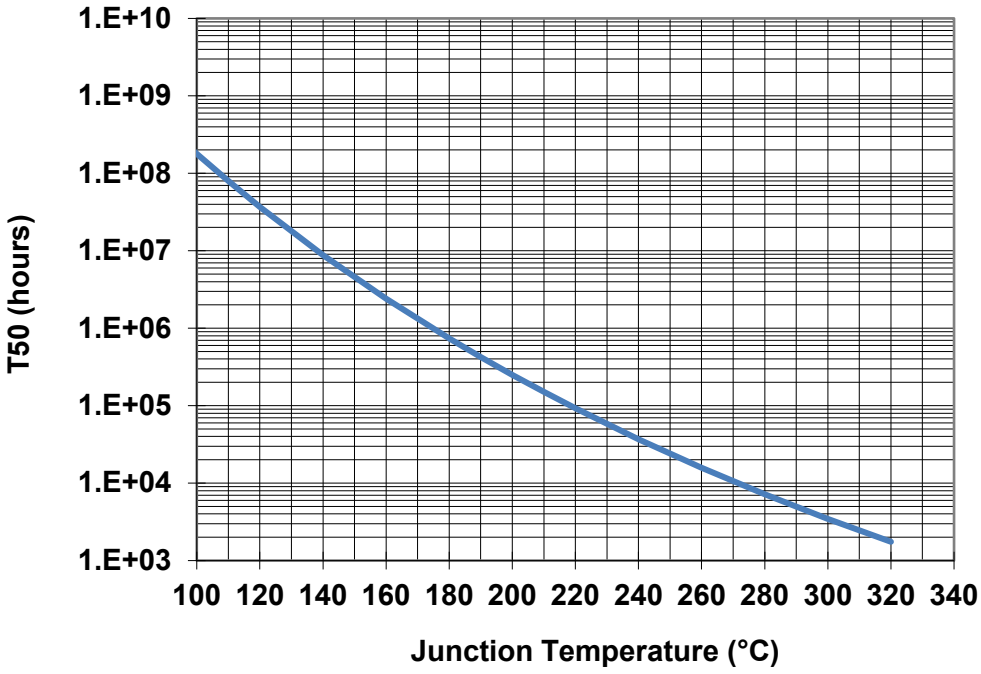
Device Thermal Performance

The device thermal performances below are based on UMS rules to evaluate the junction temperature.
This same procedure is the basis for junction temperature evaluation of the samples used to derive the Median lifetime and activation energy for the particular technology on which the CHA8282-99F is manufactured (GaN HEMT 0.15µm).
The temperature T_{BS} is defined as the chip backside temperature. The thermal resistance (Rth), given in the following table, is for the full circuit in CW mode.
The system maximum temperature must be adjusted in order to guarantee that Tjunction remains below the maximum value specified in the Recommended Operating Range table. The system PCB must be designed to comply with this requirement.

Parameter	Conditions	Tjunction (°C)	Rth (°C/W)	T50 (hours)
Rth(1) Thermal Resistance	Vd = 22V Idq = 300mA Pout = 39dBm Dissipated power = 22.7W	153.9	3.04	$3.53x10^6$
	Vd = 25V Idq = 300mA Pout = 39.8dBm Dissipated power = 27.1W	170.3	3.15	$1.29x10^6$

(1) Thermal resistance measured to backside of the chip with Tbackside=85°C



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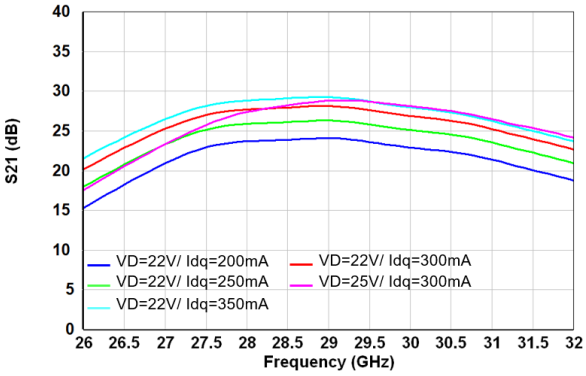
Typical Board Measurements : Small signal performance

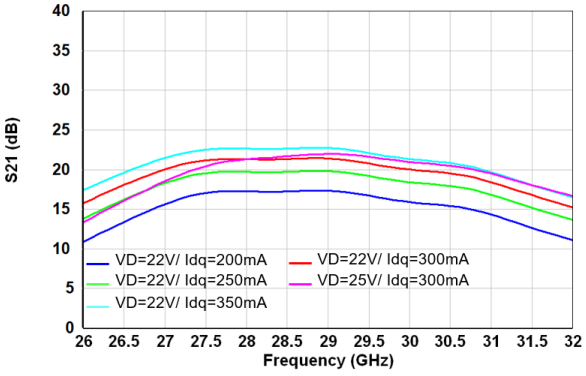
Tbackside = -40°C / 25°C / 85°C, Vd = 22V / 25V, Idq = 200mA / 250mA / 300mA / 350mA

Linear Gain vs. Frequency vs. IDq and Drain voltage

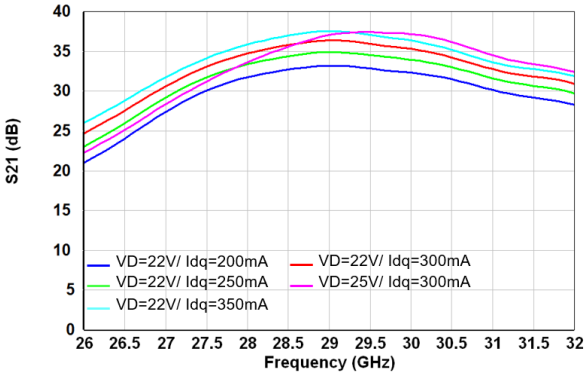
Tbackside=25°C



Tbackside=85°C



Tbackside=-40°C



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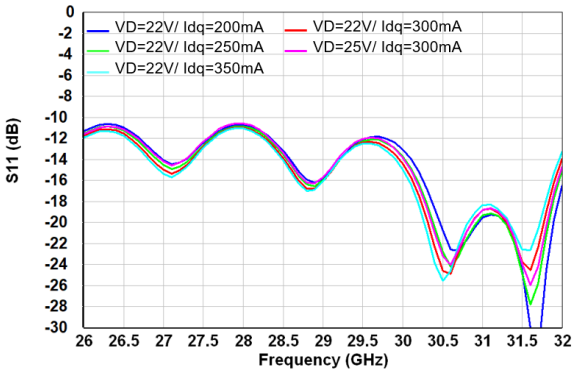
Typical Board Measurements : Small signal performance

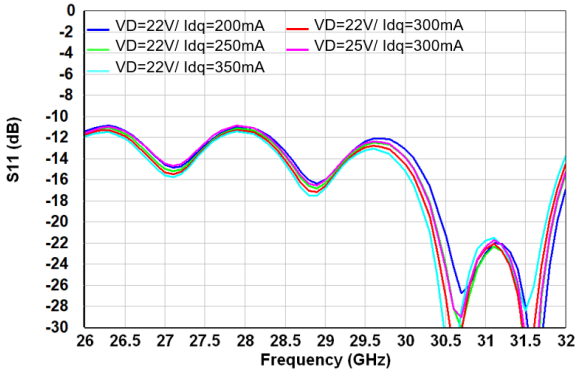
Tbackside = -40°C / 25°C / 85°C, Vd = 22V / 25V, Idq = 200mA / 250mA / 300mA / 350mA

Input Return Loss vs. Frequency vs. IDq and Drain voltage

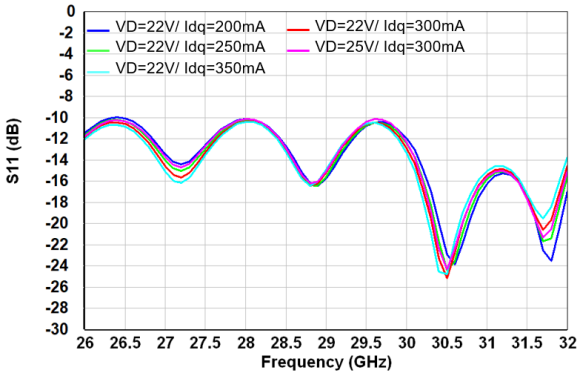
Tbackside=25°C



Tbackside=85°C



Tbackside=-40°C



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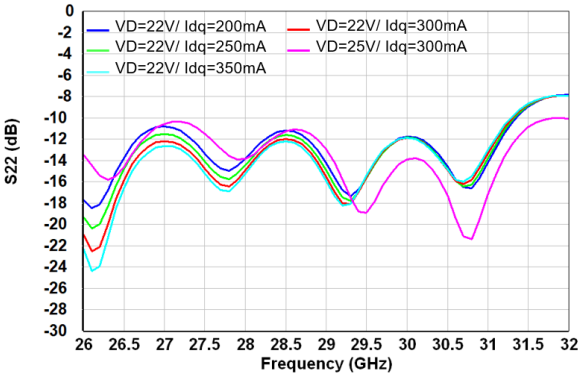
Typical Board Measurements : Small signal performance

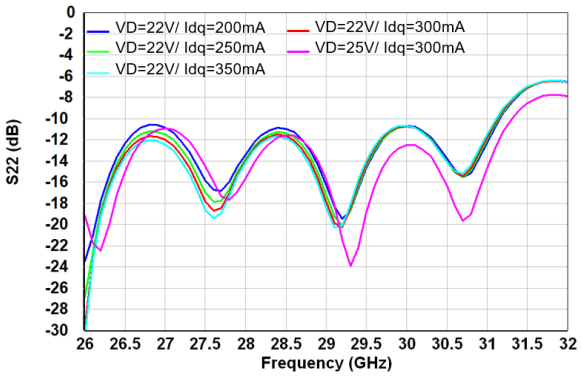
Tbackside = -40°C / 25°C / 85°C, Vd = 22V / 25V, Idq = 200mA / 250mA / 300mA / 350mA

Output Return Loss vs. Frequency vs. IDq and Drain voltage

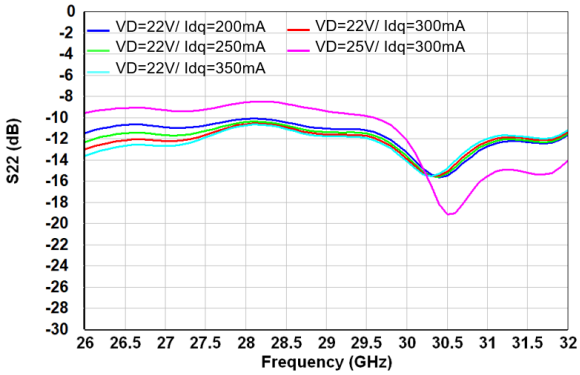
Tbackside=25°C



Tbackside=85°C



Tbackside=-40°C



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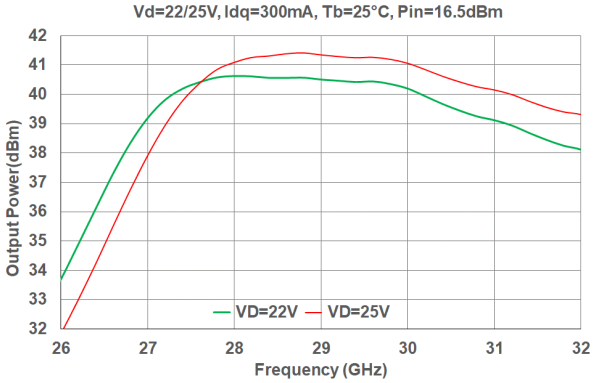
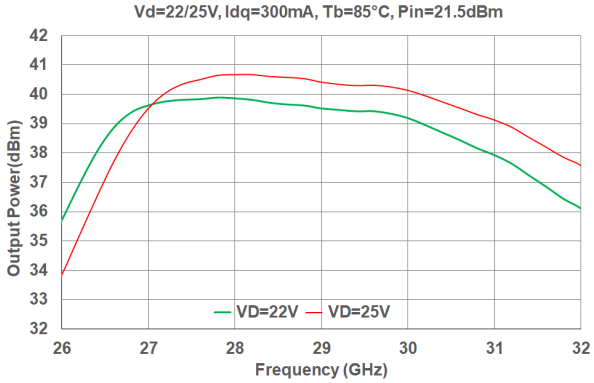
Typical Board Measurements: Large Signal Performance

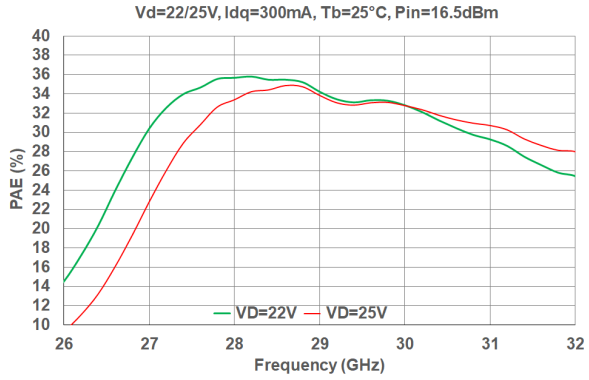
Test conditions: CW, VD=22V / 25V, Idq = 300mA, Tbackside = 25°C / 85°C

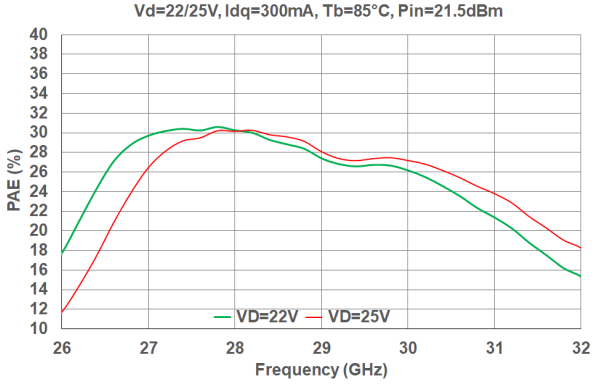
Output Power vs. Frequency vs. Drain Voltage





Power Added Efficiency vs. Frequency vs. Drain Voltage





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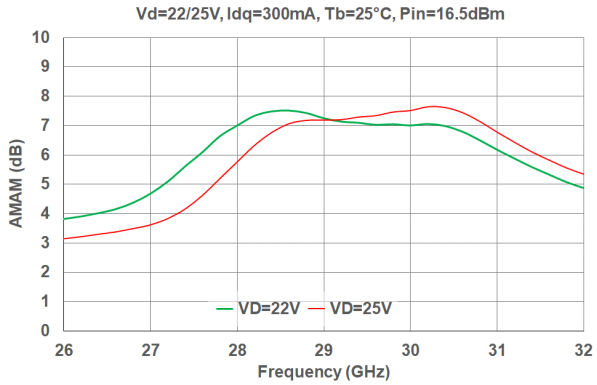
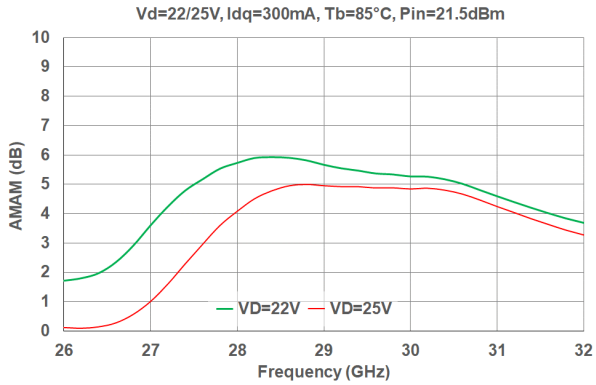
Typical Board Measurements: Large Signal Performance

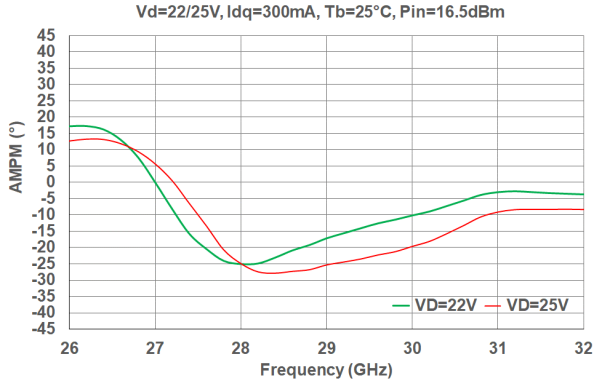
Test conditions: CW, VD=22V / 25V, Idq = 300mA, Tbackside = 25°C / 85°C

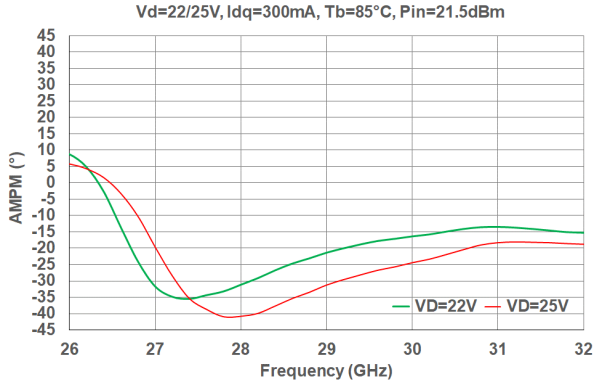
AMAM vs. Frequency vs. Drain Voltage





AMPM vs. Frequency vs. Drain Voltage





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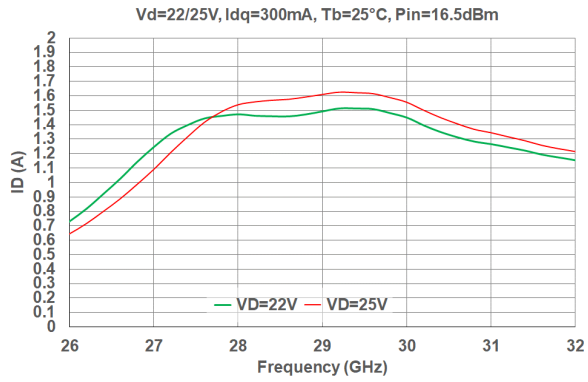
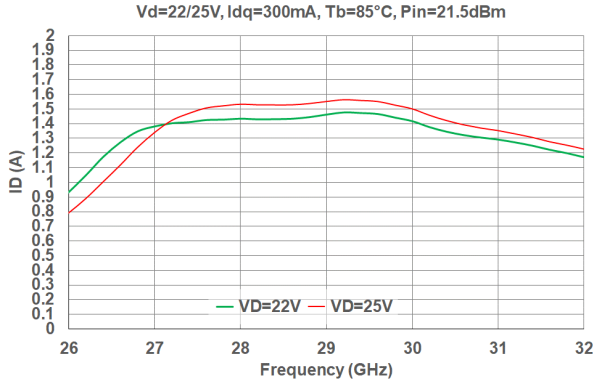
Typical Board Measurements: Large Signal Performance

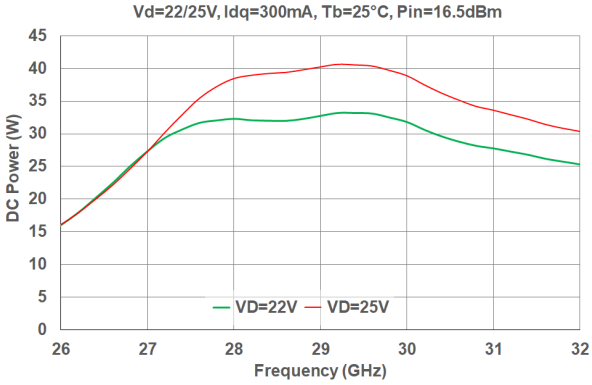
Test conditions: CW, VD=22V / 25V, Idq = 300mA, Tbackside = 25°C / 85°C

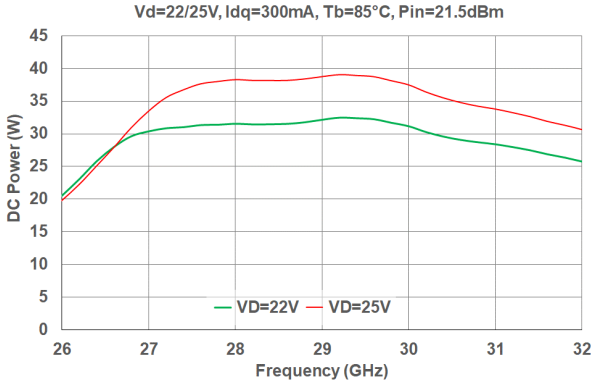
Drain Current vs. Frequency vs. Drain Voltage



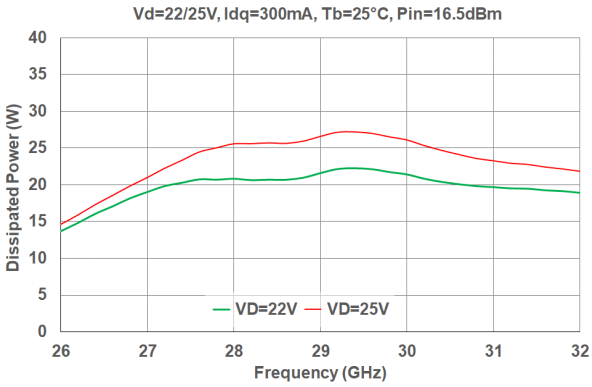


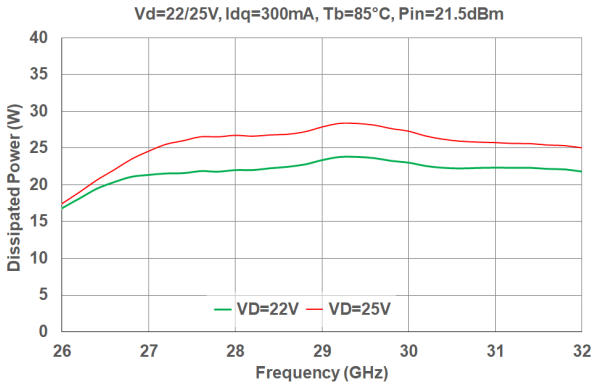
DC Power Consumption vs. Frequency vs. Drain Voltage





Dissipated Power vs. Frequency vs. Drain Voltage





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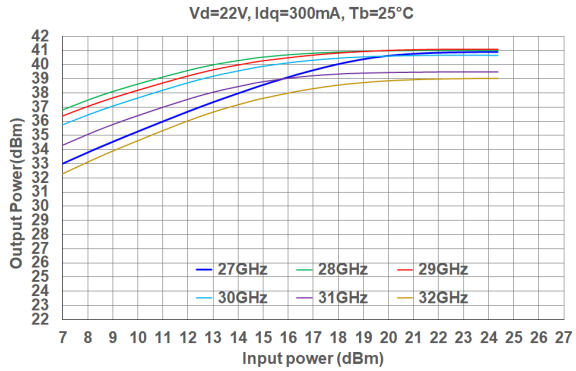
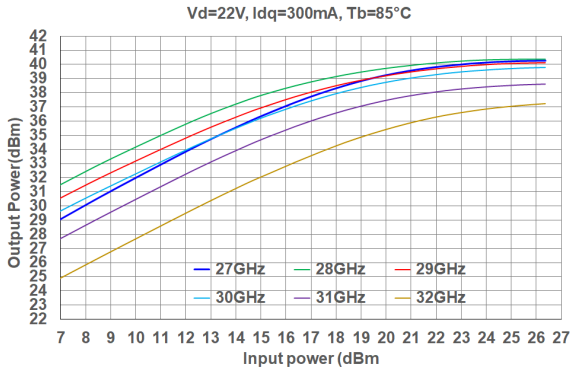
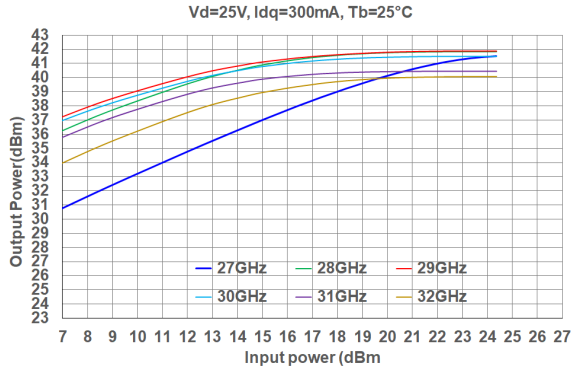
Typical Board Measurements: Large Signal Performance

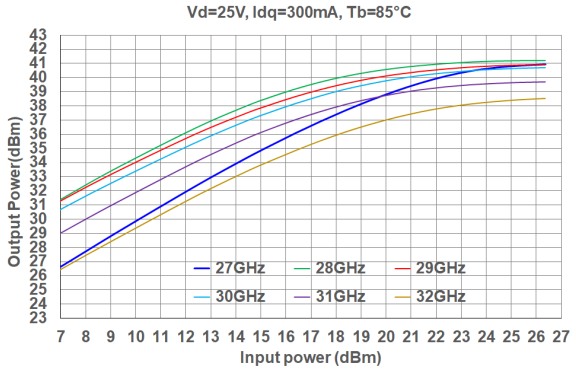
Test conditions: CW, Vd = 22 / 25V, Idq = 300mA, Tbackside = 25°C / 85°C

Output Power vs. Input Power vs. Frequency

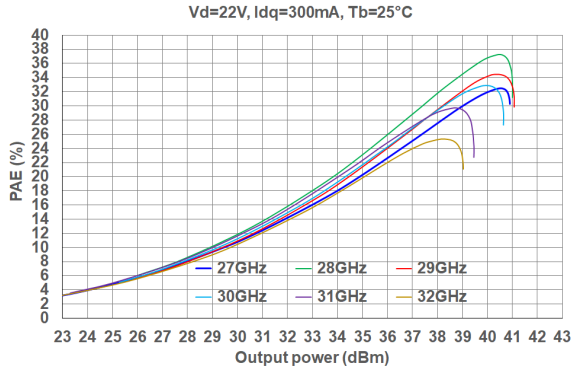


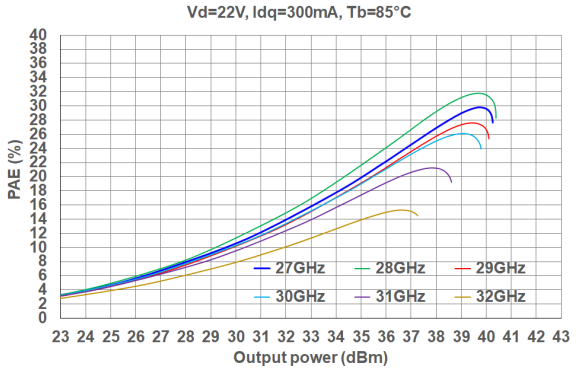


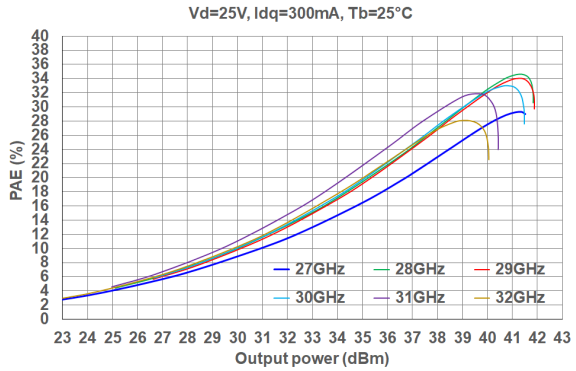


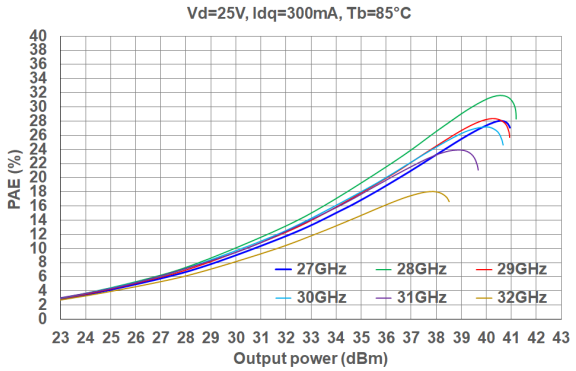


Power Added Efficiency vs. Output Power vs. Frequency









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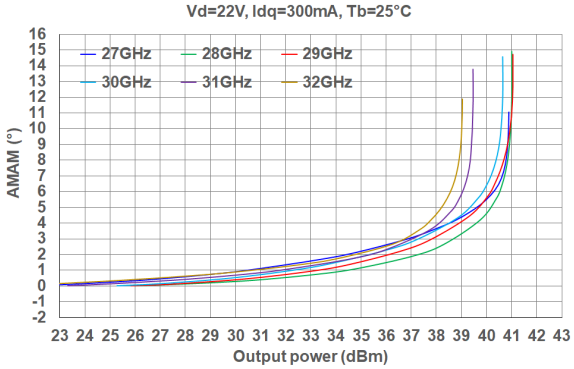
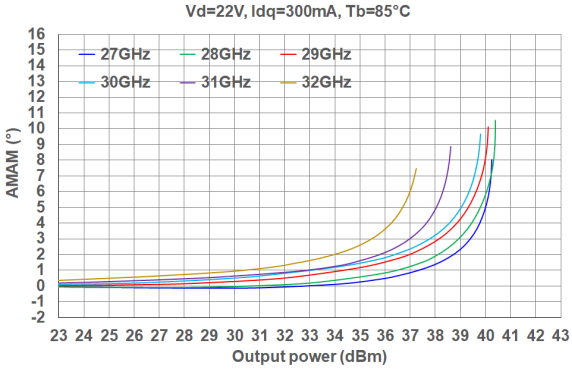
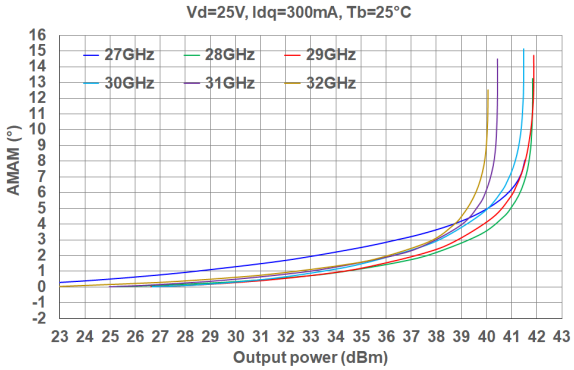
Typical Board Measurements: Large Signal Performance

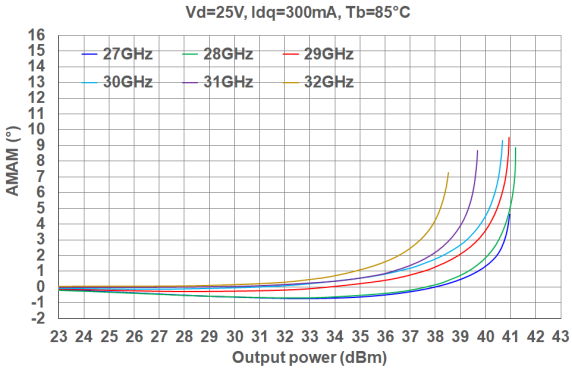
Test conditions: CW, Vd = 22V / 25V, Idq = 300mA, Tbackside = 25°C / 85°C

AMAM vs. Output Power vs. Frequency

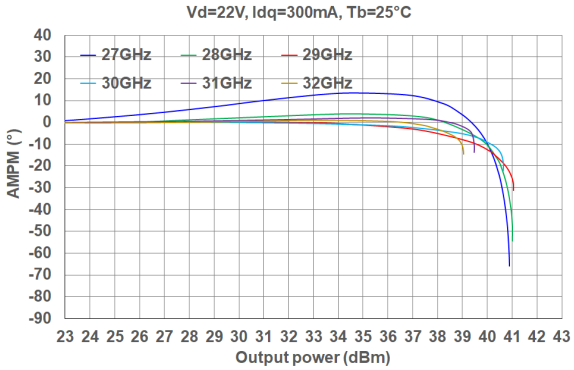


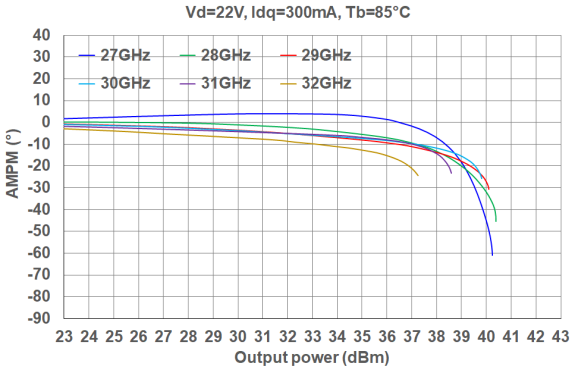


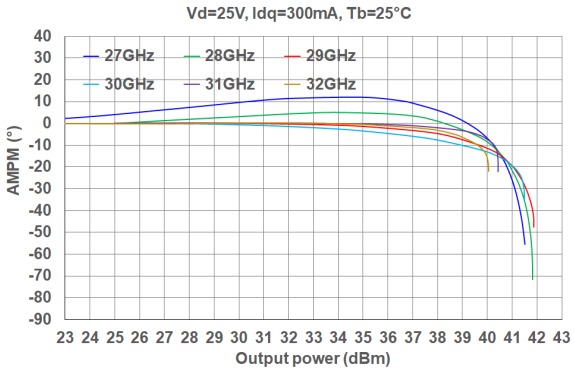


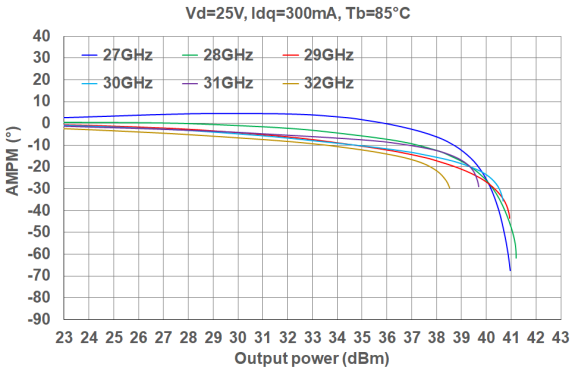


AMPM vs. Output Power vs. Frequency









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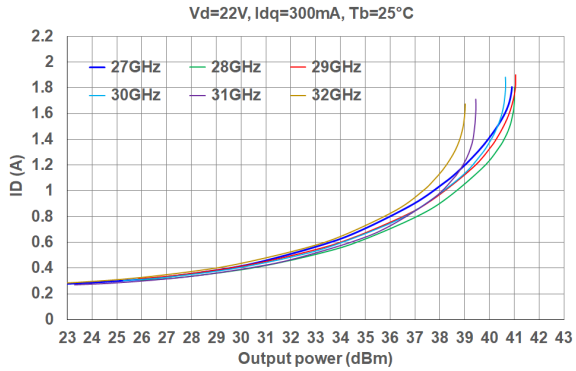
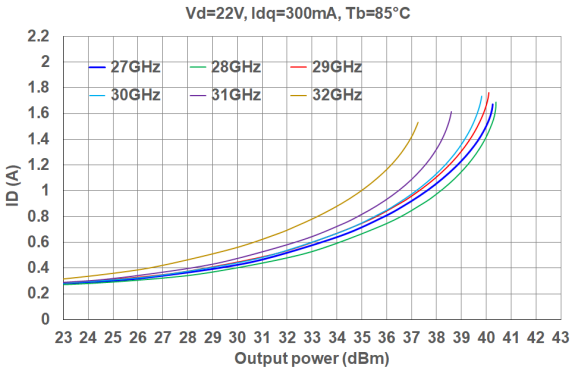
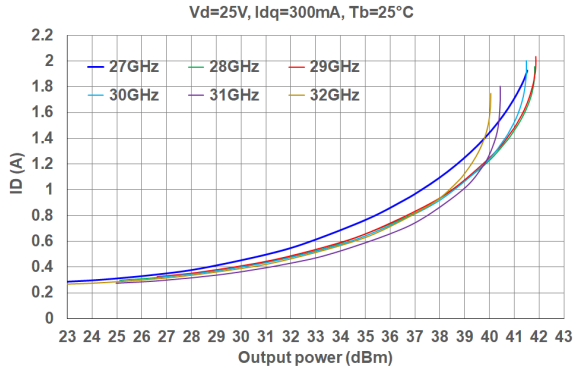
Typical Board Measurements: Large Signal Performance

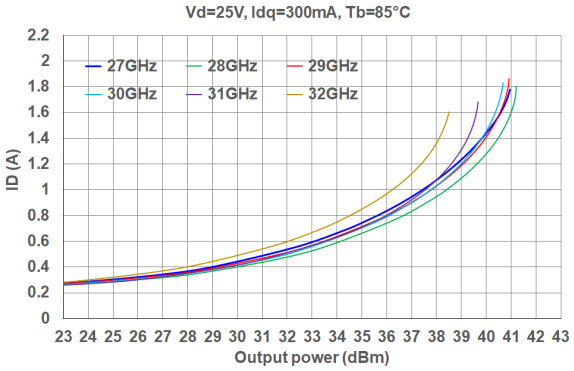
Test conditions: CW, Vd = 22V / 25V, Idq = 300mA, Tbackside = 25°C / 85°C

Drain Current vs. Output Power vs. Frequency

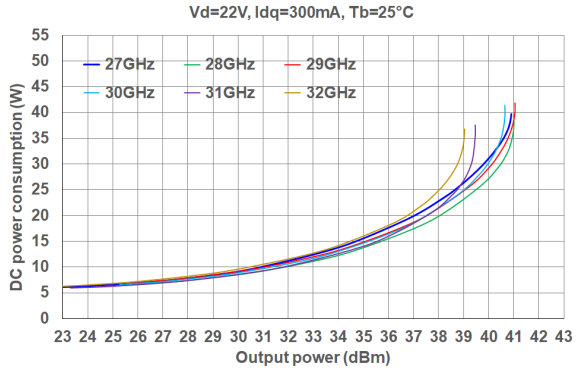


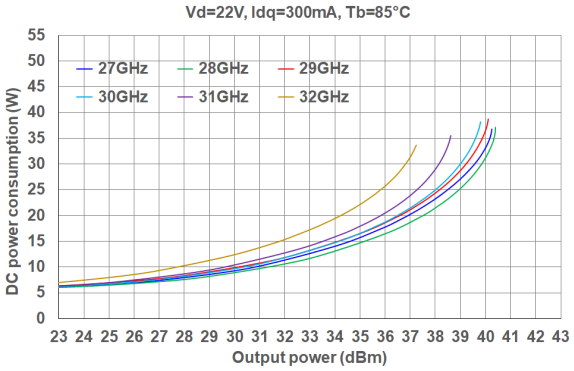


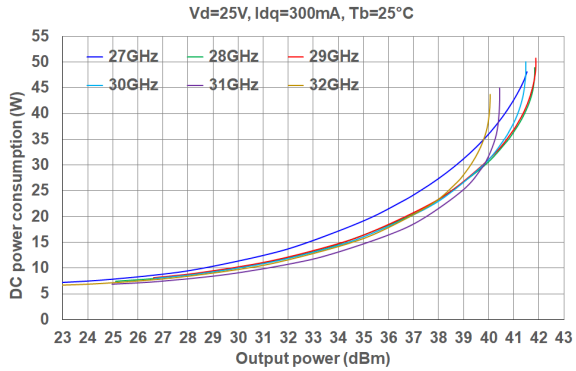


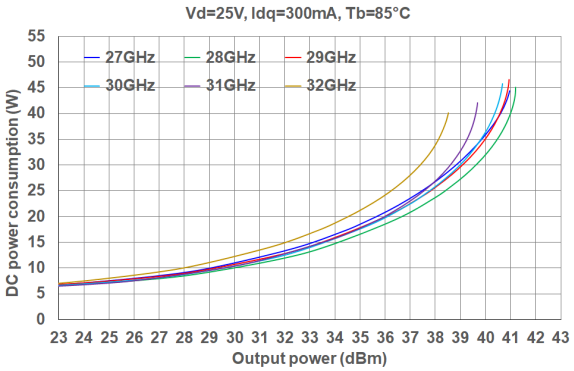


DC Power Consumption vs. Output Power vs. Frequency









Advanced Information

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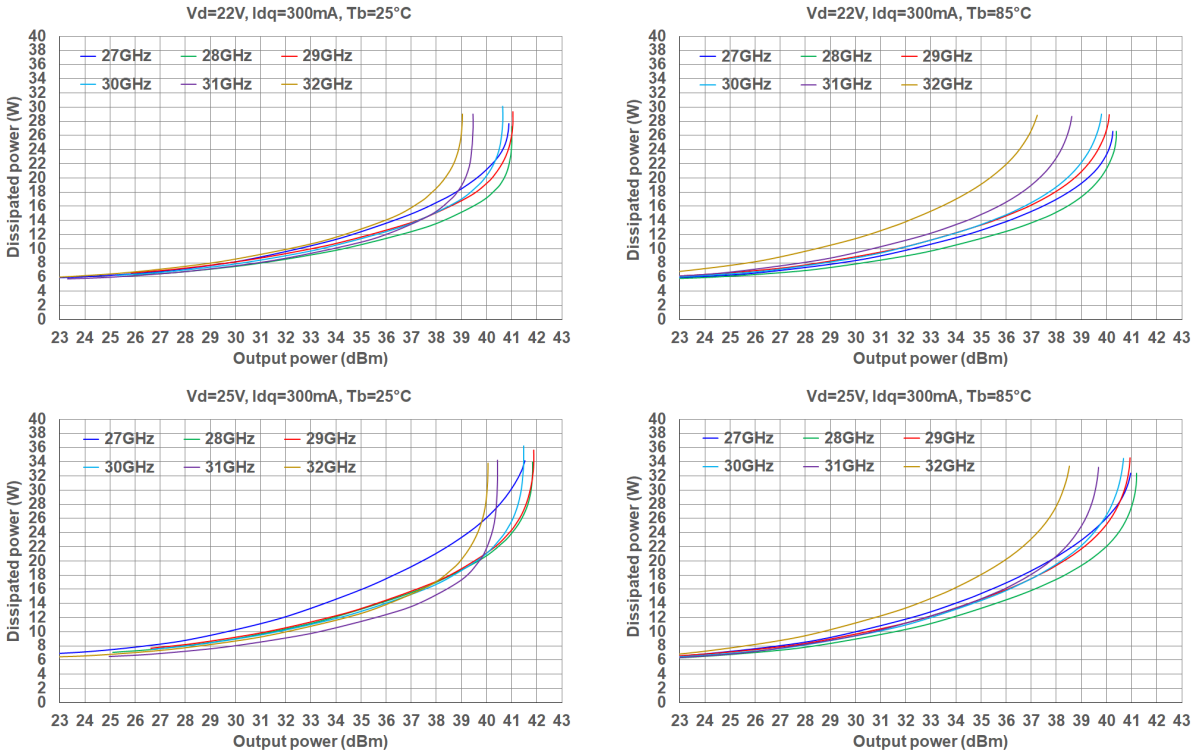
Typical Board Measurements: Large Signal Performance

Test conditions: CW, Vd = 22V / 25V, Idq = 300mA, Tbackside = 25°C / 85°C

Dissipated Power vs. Output Power vs. Frequency



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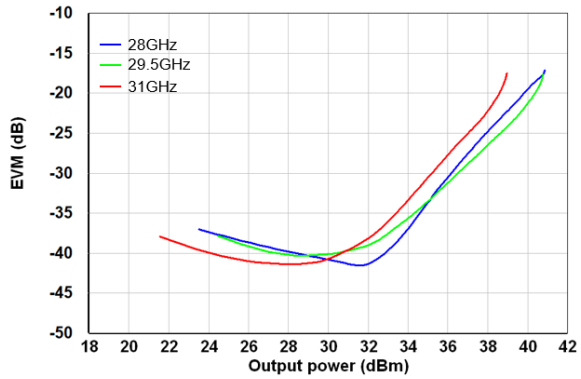
Typical Board Measurements: Linearity - Modulated Signal

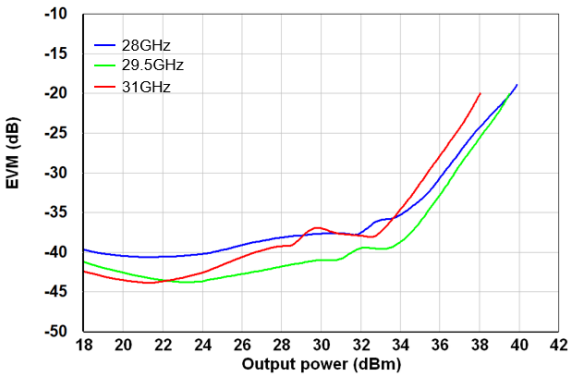
Test conditions: Vd = 22V, Idq = 300mA, 8PSK, BW = 100MHz, Roll-off = 0.2, PAPR = 5.1dB

EVM vs. Output Power vs. Frequency

Tbackside=25°C

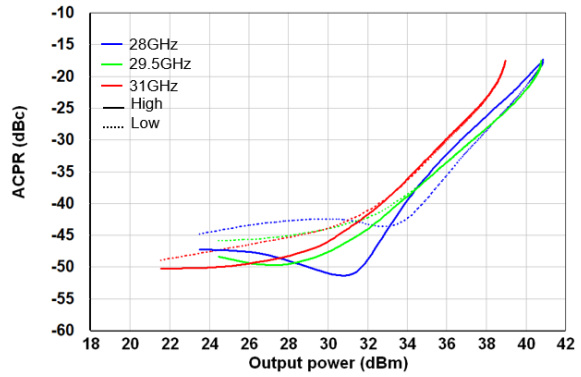


Tbackside=85°C

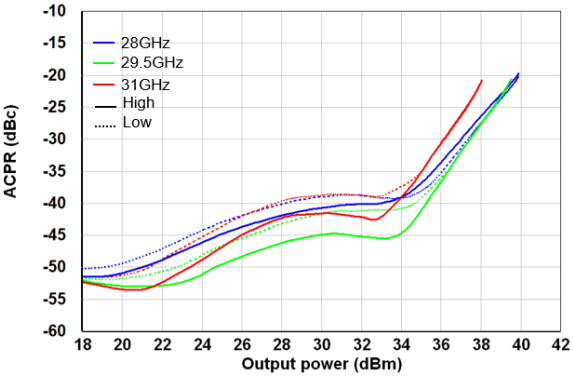


ACPR vs. Output Power vs. Frequency

Tbackside=25°C

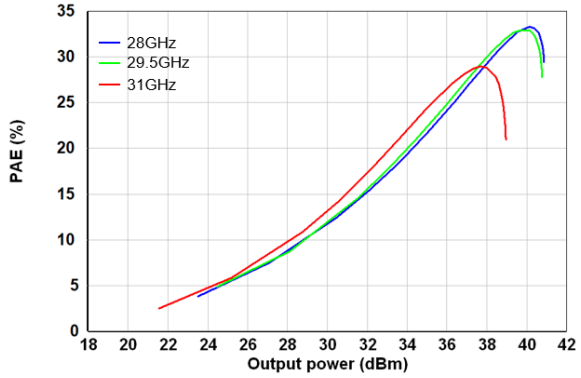


Tbackside=85°C

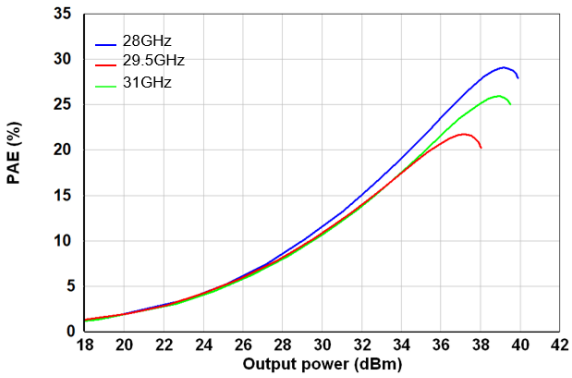


Power Added Efficiency vs. Output Power vs. Frequency

Tbackside=25°C



Tbackside=85°C



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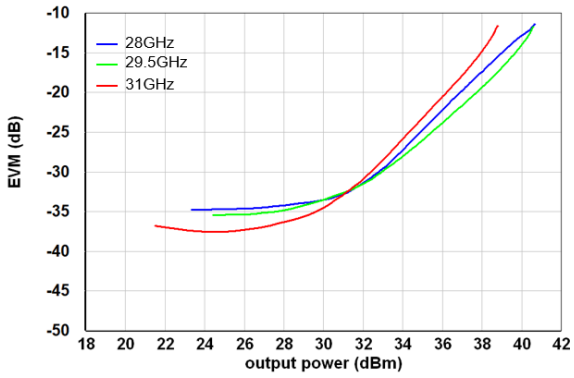
Typical Board Measurements: Linearity - Modulated Signal

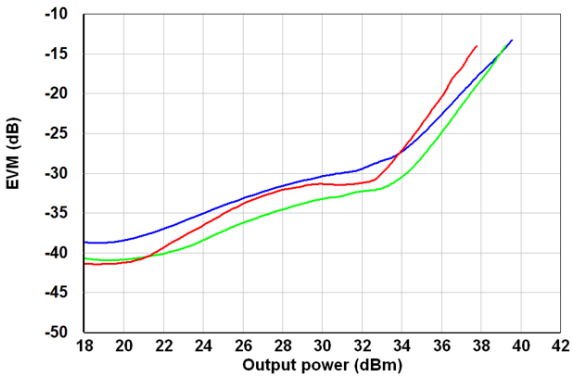
Test conditions: Vd=22V, Idq =300mA, 256QAM, BW=100MHz, Roll-off=0.2, PAPR=7.2dB

EVM vs. Output Power vs. Frequency

Tbackside=25°C

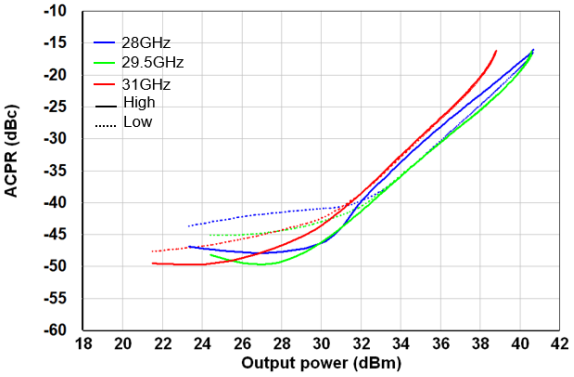


Tbackside=85°C

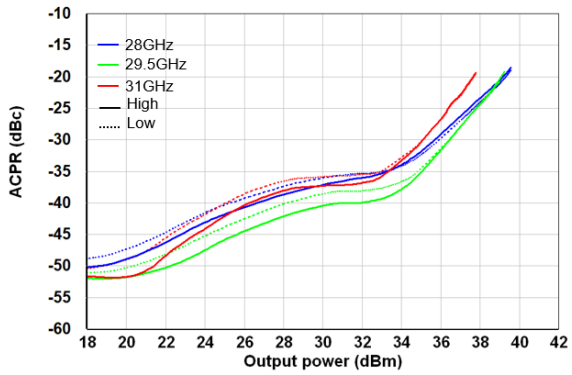


ACPR vs. Output Power vs. Frequency

Tbackside=25°C

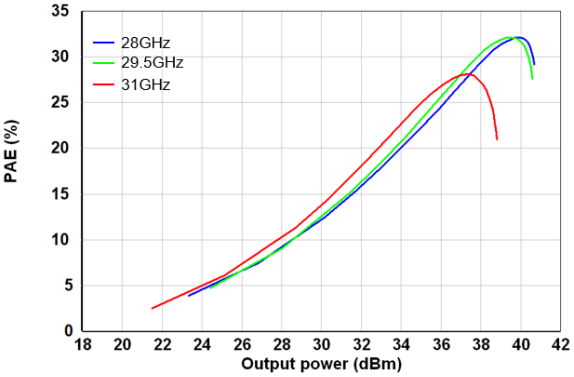


Tbackside=85°C

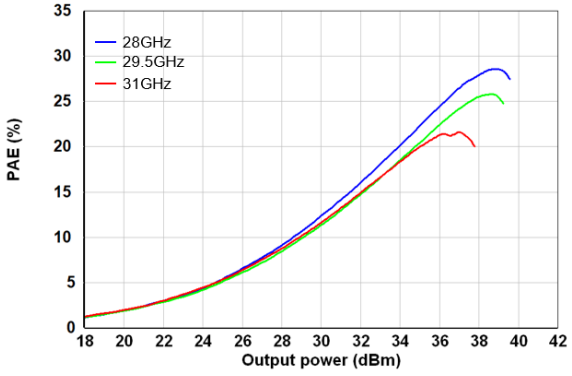


Power Added Efficiency vs. Output Power vs. Frequency

Tbackside=25°C



Tbackside=85°C



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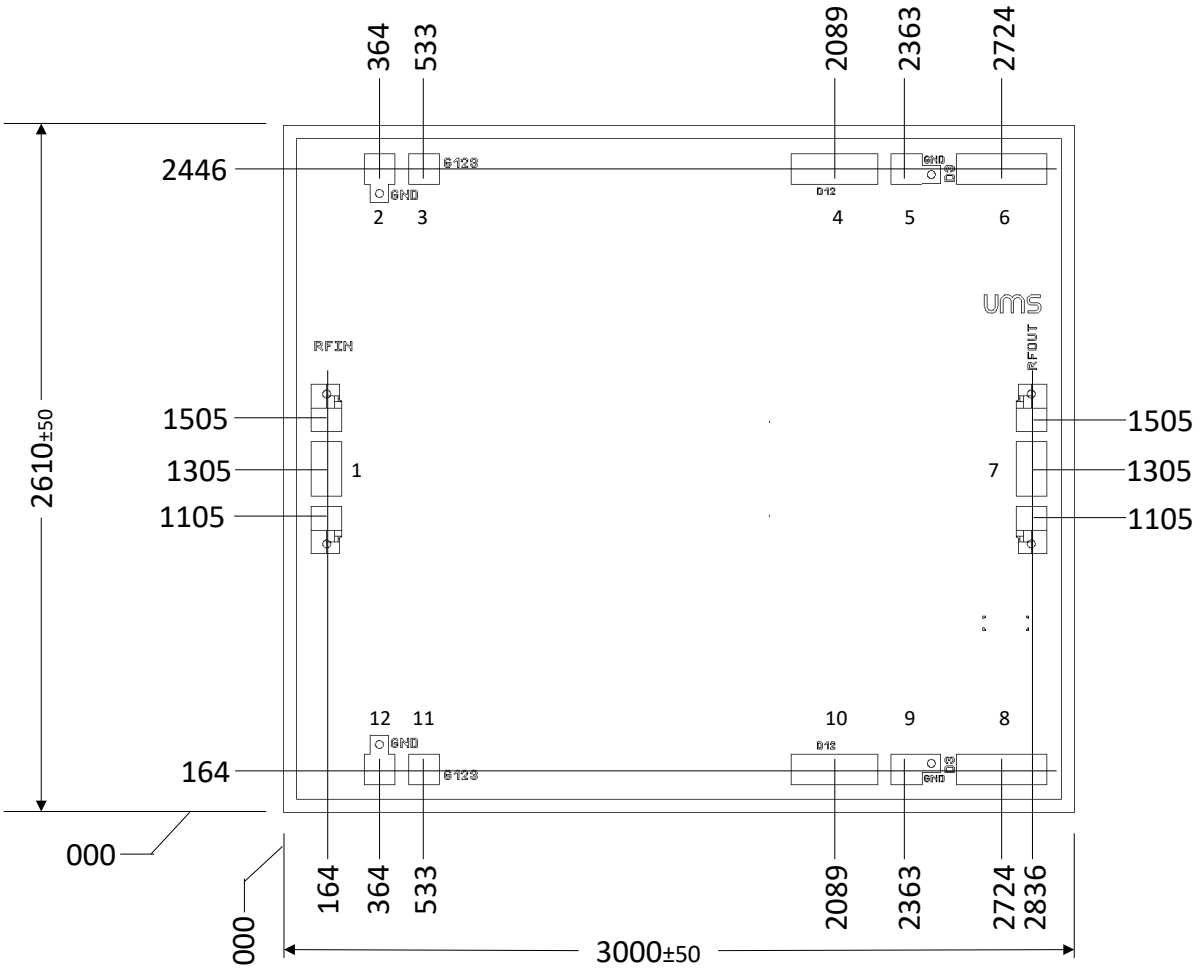
Mechanical data



Chip thickness: 70µm.
Chip size: 3000x2610 ±50µm
All dimensions are in micrometers
DC pads (2,3,5,9,11,12) size is 116x116 µm²
DC pads (4,10) size is 328x116 µm²
DC pads (6,8) size is 341x116 µm²
RF pad (1, 7) opening is 206x116 µm²

1-	RF_IN	8-	VD3S		
2-	GND (1)	9-	GND(1)		
3-	VG123N	10-	VD12S		
4-	VD12N	11-	VG123S		
5-	GND(1)	12-	GND(1)		
6-	VD3N				
7-	RF_OUT				

(1) Ground all pins marked “GND” through the PCB board is strongly recommended. Ensure that the PCB board is designed to provide the best possible ground to the die.

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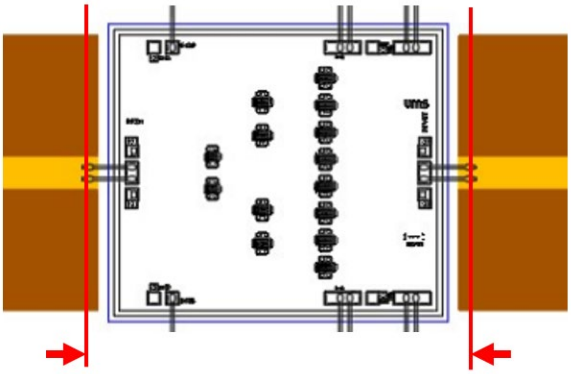
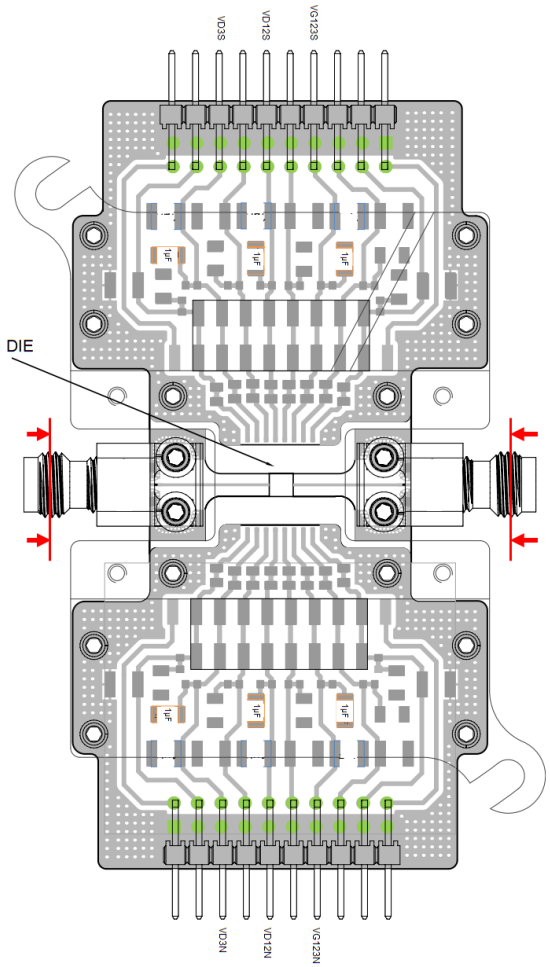
Measurement Reference Planes

The reference planes used for S21, power and linearity measurements given above are located at input and output of the MMIC as defined on the drawing opposite.



Input and Output Return Loss (S11 and S22) are given at Evaluation Board connectors' reference planes as defined on the drawing opposite.



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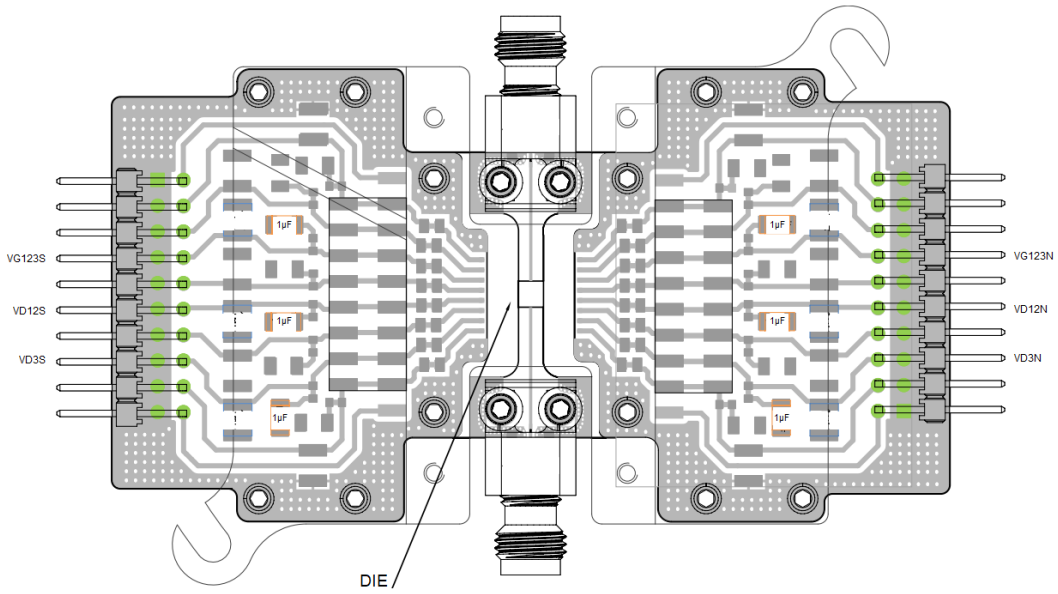
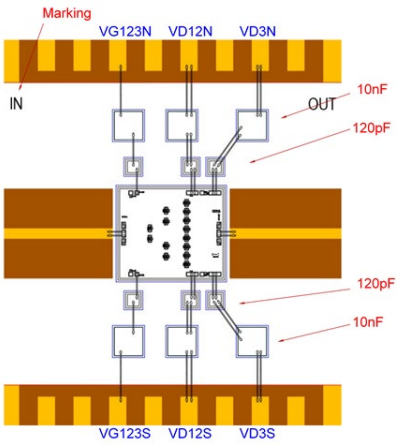
Recommended Assembly Plan





The decoupling network used is composed of 3 levels of parallel capacitors. The first level is 120pF chip capacitor, the second level is 10nF chip capacitor, the third level is 1µF SMD capacitor. The first two levels should be as close as possible to the die.

Recommended circuit bonding and decoupling table

Label	Bonding (25µm diameter)	External Capacitor
RFin//RFout	Two parallel bond wires on input and output RF accesses	Not required
VG123N, VG123S	Inductance ≤ 1nH (mainly for first decoupling level)⇒1.2mm length	C1 ~ 120pF C2 ~ 10nF C3 ~ 1µF
VD12N, VD3N, VD12S, VD3S	Inductance ≤ 1nH (mainly for first decoupling level)⇒1.2mm length	C1 ~ 120pF C2 ~ 10nF C3 ~ 1µF

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Notes

Due to ESD protection circuits on RF input and output, an external capacitance might be requested to isolate the product from external voltage that could be present on the RF accesses

Recommended reflow process assembly

Refer to the application note AN0001 available at https://www.ums-rf.com for die attach.

Recommended ESD management

Refer to the application note AN0020 available at https://www.ums-rf.com for ESD sensitivity and handling recommendations.

Recommended Evaluation board assembly

Refer to the application note AN0030 available at https://www.ums-rf.com Evaluation board.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at http://www.ums-rf.com.

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Maturity Level

Maturity Level	Product status	Documentation	Reliability	Usage in a system
Lab Sample (LS)	Decision to develop the product is not confirmed	Technical Information	No commitment	Lab demonstrator
Engineering Sample (ES)	**Design may change**	**Advanced Information**	**The design is within the recommended temperature, current and voltage ranges as regards the technology used.**	**Engineering demonstrator**
Product Representative Unit (PRU)	Design is frozen	Data-sheet	Tests results are available on the foreseen product or on an similar one	Production

Sampling request reference

Die: ES-CHA8282-99F
Demo board: EVB-CHA8282-99F

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