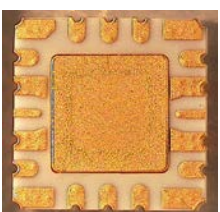
AN0024

Application Note for Surface Mount Hermetic Package FAB Type

1. FAB type package general presentation

FAB type package is ideal for application requiring enhanced reliability and electrical performances. This surface mount square no lead package (QFN like) is fully hermetic and is designed to operate at very high frequency above 30GHz with a very low thermal resistance at the same time.
This package is perfectly adapted to defence and space applications and can also be used for power devices.
Its very compact ceramic metal body with outline dimensions of 6x6 mm² is designed to be compatible with standard automatic SMT assembly and tests industrial equipments massively used for QFN packages.
This package includes two 50Ω accesses for millimetre-wave signals and ten accesses for DC, control or RF signals. A large ground pad is managed at the package's bottom side in order to improve the electrical and thermal performances.

Top view



Bottom view

Figure 1: FAB package top and bottom views.

Main features:

	Unit	Typical Value
Package type	-	QFN
Body dimensions	mm²	6 x 6
Package thickness	mm	2.2
Number of millimetre-wave leads	-	2
Number of low frequency leads	-	10
Metallic ground pad surface	mm²	3.7 x 3.7
Package's ground pad thermal resistance	°C/W	<0.2
MSL	-	1
Hermetic sealing (fine leak compliant Mil-Std-883 Method 1014.10 Condition A4, tracer gas He at 1atm)	ccHe/s/atm	$1x10^{-8}$
Package leads finish is gold (Au)	µm	0.8 min.
Solderability (Mil-Std-883 Method 2003.7, aging operation omitted)		Under x10 magnification, at least 95% coverage by continuous solder coating

United Monolithic Semiconductors S.A.S.
Bât. Charmille - Parc SILIC - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34

2. Package outline

The package outline is given at the Annex 1.
Please periodically refer to the UMS web site: http://www.ums-gaas.com to get the latest drawings.

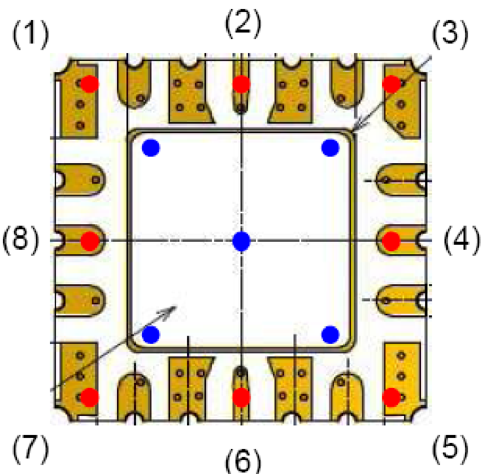
3. Assembly recommendations

FAB type package is defined to be compatible with most of the standard surface mount assembly techniques (SMT). This section gives some recommendations to implement the package assembly on PCB.

3.1. Package bottom-side coplanarity

In despite of its large ground/thermal pad at the center, the bottom side of this package is very flat in order to ease the assembly process on PCB. The coplanarity between the large ground and the signal leads is better than +/-50µm at CPK>1.9 (see Table 1). The calculation of this coplanarity is described at the Figure 2.

$$Coplanarity = \frac{1}{5}\sum Blue_points_altitude - \frac{1}{8}\sum Red_points_altitude$$



< - (negative) value> = CuMo is retracted from Ceramic

< + (positive) value> = CuMo is protruded from Ceramic

Figure 2: Package's bottom side coplanarity control points

Bât. Charmille - Parc SILIC - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34

No.	Ceramic height (red point) from reference plane (CuMo)								MAX. (positive)	MAX. (negative
	(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)		
1	-0.0190	0.0005	-0.0090	-0.0005	-0.0105	-0.0050	-0.0165	-0.0065	0.0005	-0.0190
2	-0.0120	0.0050	-0.0075	0.0000	-0.0060	0.0090	-0.0060	-0.0025	0.0090	-0.0120
3	-0.0140	0.0100	-0.0045	0.0010	-0.0095	0.0110	-0.0070	0.0015	0.0110	-0.0140
4	-0.0145	0.0000	-0.0180	-0.0095	-0.0180	0.0100	0.0050	0.0050	0.0100	-0.0180
5	-0.0110	0.0040	-0.0010	0.0080	-0.0015	0.0125	0.0040	0.0045	0.0125	-0.0110
6	-0.0075	0.0125	-0.0090	0.0005	-0.0135	0.0100	0.0085	0.0140	0.0140	-0.0135
7	-0.0215	-0.0030	-0.0080	-0.0055	-0.0125	0.0000	-0.0210	-0.0115	0.0000	-0.0215
8	-0.0050	0.0090	-0.0035	-0.0005	-0.0070	0.0125	0.0040	0.0050	0.0125	-0.0070
9	-0.0100	0.0045	-0.0030	0.0020	-0.0090	0.0045	-0.0120	0.0010	0.0045	-0.0120
10	-0.0220	-0.0030	-0.0195	-0.0080	-0.0110	0.0040	-0.0100	0.0005	0.0040	-0.0220
11	-0.0275	-0.0010	-0.0065	0.0095	0.0005	0.0120	-0.0130	-0.0050	0.0120	-0.0275
12	-0.0075	0.0110	-0.0050	0.0020	-0.0105	0.0095	-0.0055	0.0060	0.0110	-0.0105
13	-0.0030	0.0045	-0.0030	-0.0020	-0.0095	0.0030	-0.0060	0.0070	0.0070	-0.0095
14	-0.0080	0.0090	-0.0095	-0.0060	-0.0140	0.0105	-0.0120	-0.0005	0.0105	-0.0140
15	-0.0085	0.0115	-0.0030	0.0045	-0.0060	0.0105	-0.0055	0.0015	0.0115	-0.0085
16	-0.0235	-0.0040	-0.0095	-0.0020	-0.0050	0.0030	-0.0125	-0.0015	0.0030	-0.0235
17	-0.0060	0.0100	-0.0140	-0.0045	-0.0110	0.0140	0.0020	0.0025	0.0140	-0.0140
18	-0.0075	0.0065	-0.0060	0.0015	-0.0090	0.0100	0.0045	0.0115	0.0115	-0.0090
19	-0.0070	0.0090	-0.0100	0.0055	-0.0020	0.0130	0.0070	0.0130	0.0130	-0.0100
20	-0.0225	-0.0075	-0.0175	-0.0105	-0.0205	-0.0055	-0.0105	-0.0045	-0.0045	-0.0225
21	-0.0030	0.0030	-0.0175	-0.0065	-0.0180	0.0010	0.0015	0.0100	0.0100	-0.0180
22	-0.0225	-0.0030	-0.0215	-0.0095	-0.0205	-0.0045	-0.0155	-0.0080	-0.0030	-0.0225
23	-0.0215	0.0045	0.0020	0.0010	-0.0085	0.0010	-0.0210	-0.0070	0.0045	-0.0215
24	-0.0190	0.0105	-0.0010	0.0055	-0.0105	0.0075	-0.0125	0.0055	0.0105	-0.0190
25	-0.0190	-0.0005	-0.0115	-0.0050	-0.0150	0.0055	-0.0140	-0.0035	0.0055	-0.0190
26	-0.0130	0.0060	-0.0080	-0.0005	-0.0090	0.0070	-0.0090	0.0000	0.0070	-0.0130
27	-0.0015	0.0120	-0.0040	0.0005	-0.0055	0.0120	0.0030	0.0095	0.0120	-0.0055
28	-0.0265	-0.0090	-0.0155	-0.0095	-0.0140	-0.0055	-0.0225	-0.0095	-0.0055	-0.0265
29	-0.0095	0.0065	-0.0200	-0.0055	-0.0105	0.0080	0.0045	0.0095	0.0095	-0.0200
30	-0.0115	0.0040	-0.0170	-0.0035	-0.0120	-0.0005	-0.0145	-0.0005	0.0040	-0.0170
							MAX. (positive)		0.0140	-
							MAX. (negative)		-	-0.0275
							AVE.		0.0074	-0.0160
							STDEV		0.0056	0.0059
							Cpk	0.03MAX.	1.3579	
								0.04MAX.	1.9583	
								0.05MAX.	2.5587	
								0.06MAX.	3.1592	
							Cpk	-0.03MAX.		0.7846
								-0.04MAX.		1.3464
								-0.05MAX.		1.9082
								-0.06MAX.		2.4700

Table 1 : Coplanarity measurement results and CPK calculation.

3.2. Solder past selection

The FAB type package is designed to comply with standard surface mount assembly processes. Leaded (SnPb) or RoHS leadless solder pasts (like SnAgCu) can be used with this package which has gold platted terminations with 0.8µm minimum of gold (Au).

Bât. Charmille - Parc SILIC - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34

In case of a leadless solder past is selected (RoHS), an example of standard reflow profile is given at Figure 3. This profile is given for indication and has to be carefully adjusted depending on the actual PCB design and the selected solder past.

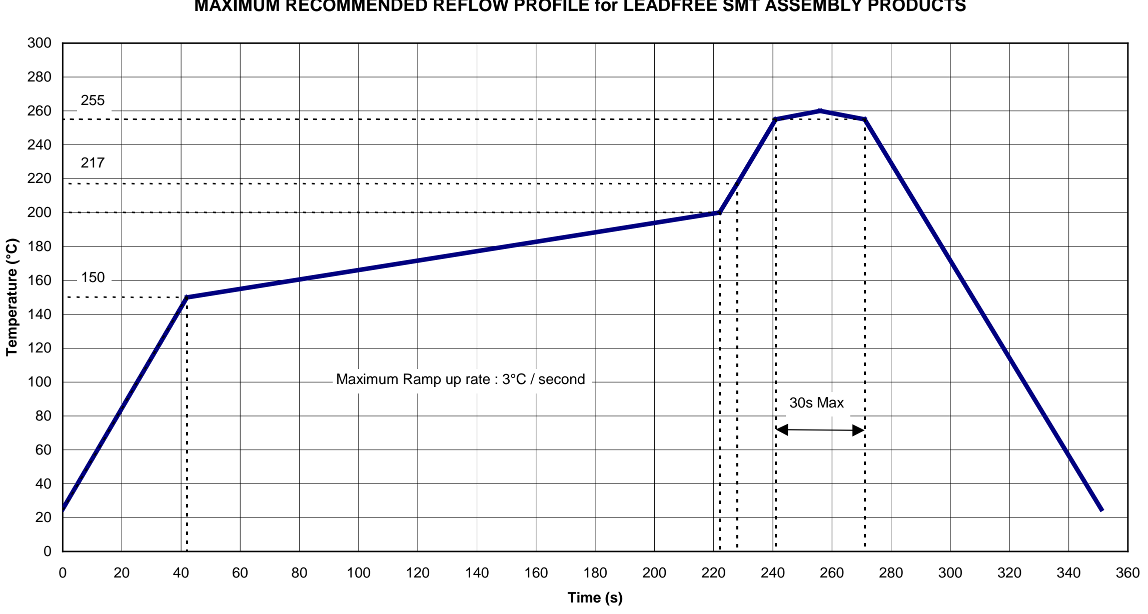


Figure 3 : Recommended reflow temperature profile for leadless solder (RoHS).

3.3. Recommendations for solder past printing process selection

Solder past deposition process and calibration should be defined according to the coplanarity parameters indicated at section 3.1. Three solder past deposition methods can be considered:

Dispensing

This process offers a lot of flexibility and is well adapted to medium production volume. The possibility to calibrate the amount of solder past dispensed on each land pattern enable to easily manage the coplanarity of the package's bottom side.

Screen printing and **stencil printing** processes are preferred for mass production. Apertures for screen and stencil design are critical and have to be done by considering the following parameters:

1. Land pattern dimensions on PCB. Generally a solder mask is also recommended to stop the solder during wetting.
2. Solder past viscosity
3. PCB design
4. Package leads and ground pad coplanarity

A design of experiment (DOE) is recommended in order to define the appropriated parameters.

Bât. Charmille - Parc SILIC - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34

3.3.1. Solder mask design recommendations

For compact and low pitch packages it is necessary to prevent the solder bridging. Generally, a solder mask is used to avoid this kind of issues in production. The solder mask will also help to define the areas where the solder can flow and control the solder homogeneity under the package contacts (leads and exposed pad). Then the quality and the reliability of the solder joins are enhanced.

The recommended solder mask clearance around the copper pads on the PCB for land pads is 70µm [2.8mils] as shown on the Figure 4.
Concerning the package ground pad, it is recommended to manage an overlap of 70µm [2.8mils] minimum on the solder mask over the copper pad (see Figure 5). This configuration is suitable for self-centring of the package on the PCB foot-print during reflow process.

Remark: The information given in this paragraph are only indicative and should not replace the design rules of the PCB manufacturer. Furthermore, the solder mask design must also take into account the final SMT assembly process used for module as well as the selected solder past characteristics.

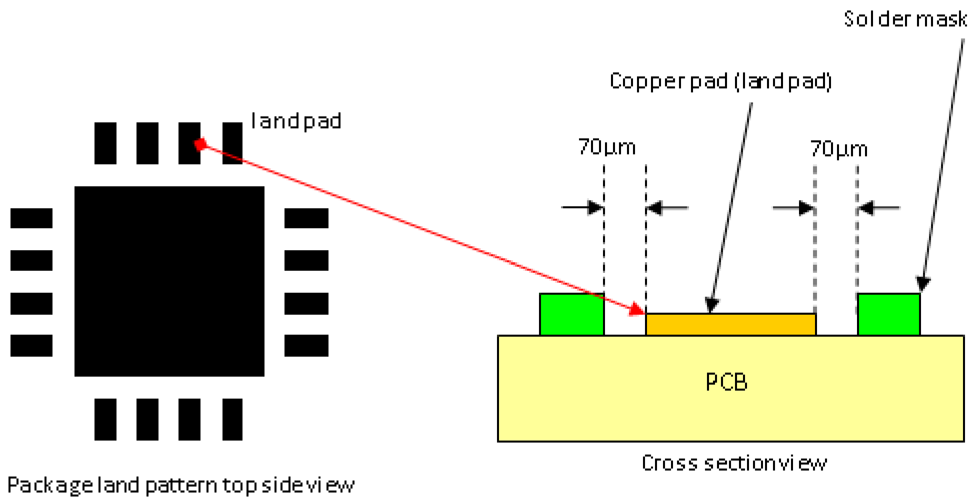


Figure 4 : Solder mask clearance around the land pads.

Bât. Charmille - Parc SILIC - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34

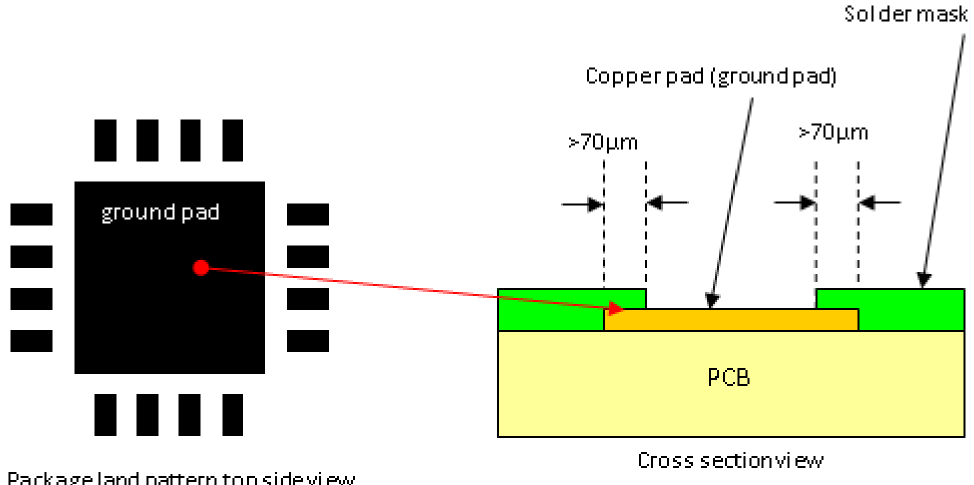


Figure 5 : Solder mask clearance around the ground pad.

3.3.2. Stencil printer recommendations

The choice of the stencil printer is very critical and must be done by the SMT assembler. The design of the stencil should be done in accordance with the solder paste material selected and the printing equipment capability. The guide lines given below are very general and only the assembler's design rules might be considered for the product industrialization.

The solder paste deposition for a small pitch package is very sensitive to the process, and should fit with the deposition on very small surfaces like the land pads (lead contact surface is less than 0.1mm²) but also on large surfaces as for the ground pad.
The squeegee blade used to deposit the solder paste into the stencil cavities could bend in the larger cavities and then limit the amount of solver paste deposited. A very convenient method used to solve this issue is to split the exposed pad surface into an array more compatible with the smallest zones defined for the land pads.
Generally the stencil aperture opening above the land pad is smaller than the copper land pad (about 50µm [2 mils] in the two directions, see Figure 6).
The stencil design for the ground pad region results from trials and evaluations on pre-serial batches in order to define the optimum pattern. Two examples of configuration are given on Figure 7.

Bât. Charmille - Parc SILIC - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34

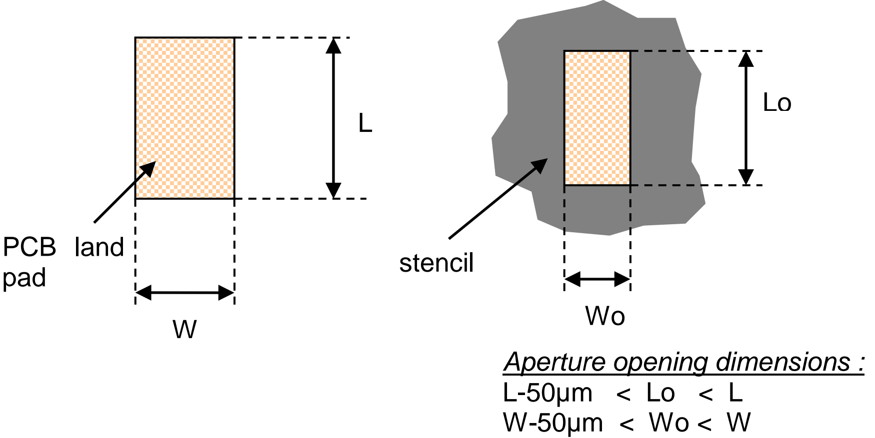


Figure 6 : Stencil aperture opening for land pads.

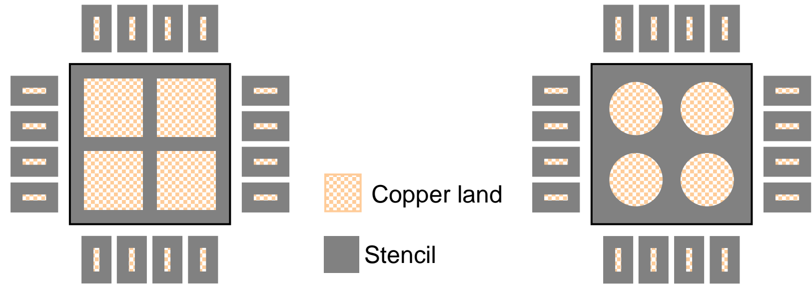


Figure 7 : ground pad stencil examples.

Take the following items into account when setting the solder paste supply amount:

1. **Solder paste printing thickness:**

In setting the solder paste printing thickness, consider the planarity of the package pins and investigate the minimum solder paste printing thickness as follows.
Minimum solder paste printing thickness = Package pin coplanarity + 0 to 30 µm

2. **Solder paste printing diameter:**

In setting the solder paste printing diameter, take the following items into consideration. Provide a stencil aperture spacing of at least 0.3 mm to prevent the occurrence of solder bridges. To prevent open solder connections, set the solder paste printing diameter to be a value larger than the minimum solder paste printing thickness as stipulated above.

Bât. Charmille - Parc SILIC - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34

4. Recommended PCB design

A demonstration printed circuit board design is available (PCB reference is 99622) and has been designed to achieve excellent electrical performances up to 30GHz. For cost improvement this PCB is made of Rogers Ro4003 material 0.203 mm [8 mils] with a double side copper cladding of 17µm [0.7 mils]. In this design, the package ground pad is electrically and thermally grounding with 25 via-holes made through the Ro4003 dielectric layer (see Figure 8). Quasi-coplanar ground/signal/ground 50Ω accesses are managed on the PCB at contact area of the package's millimetre-wave leads in order to improve the impedance matching at high frequency. Decoupling SMD capacitors have to be located as close as possible from the packaged device in order to prevent any un-stability or spurious issue. The exact location depends on the product, the application and of the selected PCB design.
The detailed PCB drawing is given at the Annex 2. A dxf file version can be provided upon request.

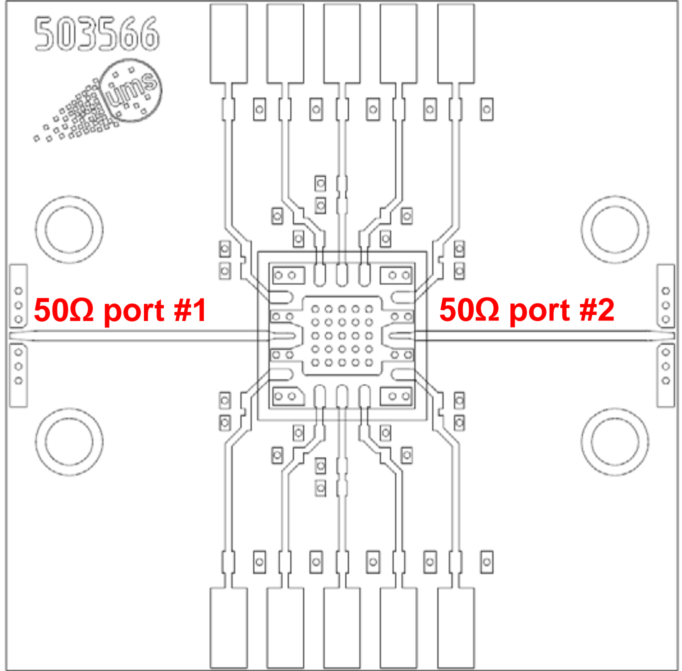


Figure 8 : Recommended PCB electrical design.

For enhanced thermal performances, a cut-out in the PCB can also be recommended in order to braze directly the package's ground pad on the metallic cold plate (ie. heat sink) of the system (see the example at Figure 9).

Bât. Charmille - Parc SILIC - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34

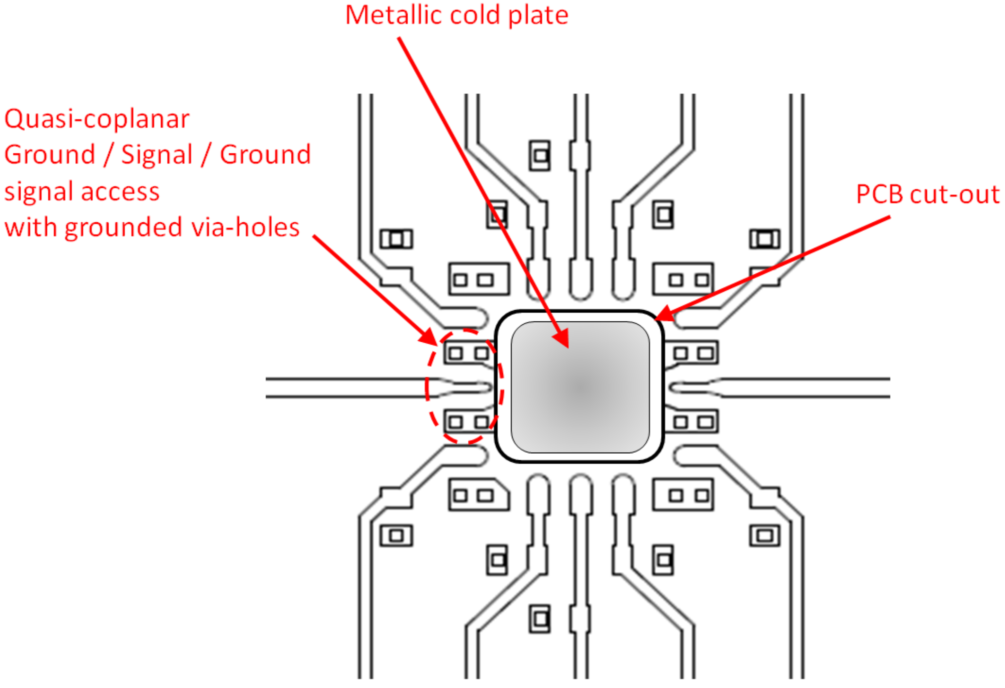


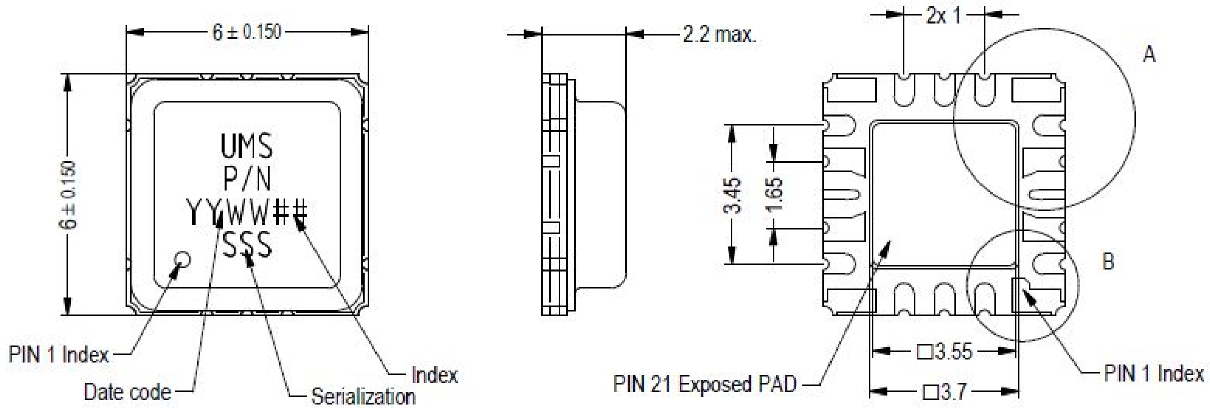
Figure 9: Alternative PCB configuration with metallic heat sink rising in the PCB cut-out.

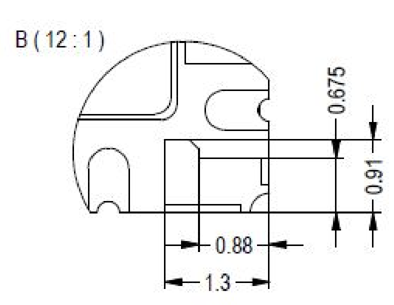
Thanks to its construction, the FAB package is perfectly mechanically matched with LTCC or others ceramic boards which should have very similar thermal expansion coefficient (CTE in ppm/°C). These boards family are perfectly adapted to space or military applications.

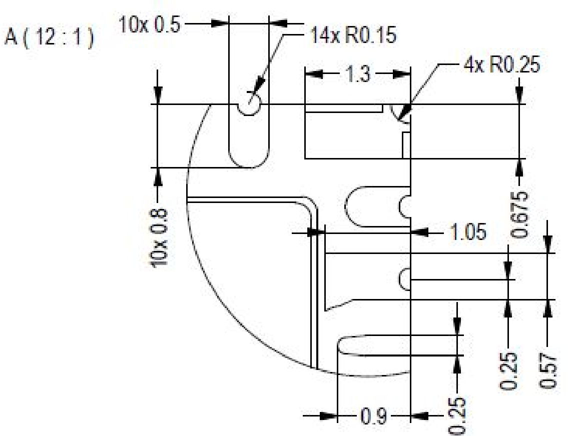
For organic PCBs made of FR4 or other multi-layers thick laminated substrates, and especially for hardened applications with large temperature range, thermal expansion of the mother-board has to be considered during the system design. In some cases, package under-filling could be recommended to improve the mechanical reliability of the assembly. Underfilling materials NAMICS Ohmcoat 1570, 1572 could be proposed.

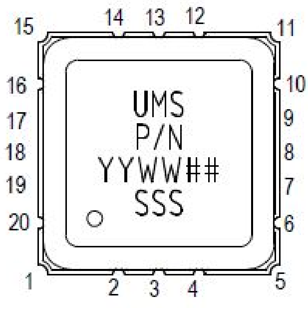
Bât. Charmille - Parc SILIC - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34

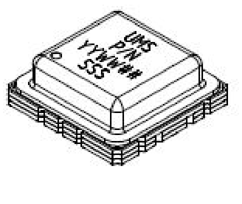
5. ANNEX 1: FAB package outline











1- GND	8- RF	15- GND
2- Signal	9- GND	16- Signal
3- Signal	10- Signal	17- GND
4- Signal	11- GND	18- RF
5- GND	12- Signal	19- GND
6- Signal	13- Signal	20- Signal
7- GND	14- Signal	21- GND

Unit : mm

Bât. Charmille - Parc SILIC - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34

6. ANNEX 2: Recommended PCB electrical design

30

30

503566

MATERIAL
Ro4003 ROGERS
Thickness : 0.008in (0,203mm)
2 Sides Cu 17.5µm

Vias Holes
○ 83 Ø 0.2 Finished
○ 4 Ø 2 Finished

Finish
Top layer : Ni 4à7µ-Pd0.15µm-Au 0.05µ (ENEPIG)
Bottom layer : Ni 4à7µ-Pd0.15µm-Au 0.05µ (ENEPIG)
Top layer : Solder Mask : XV501T

Rev.	Modification	Date

United Monolithic Semiconductors

A Company of :
AIRBUS
THALES S.A.

United Monolithic Semiconductors S.A.S.
10 avenue du Québec - SILIC 521
91946 COURTABOEUF Cedex
France

Property of ums SAS. Distribution to third parties prohibited without consent.
Propriété de ums SAS. Ne peut être communiqué à des tiers sans autorisation.

CIRCUIT 503566

Document Number : 61503566
Material Description : Circuit FAA-FAB_EDG RF7-17
Material Group : RCIRCUIT

Drawn: T Belloche – 03/08/17
App: –
Type : 011 Scale:
Format: A4 Sheet :01 of 01
Unit: mm Projection:

7. Glossary

SMD:	Surface Mount Device
SMT:	Surface Mount Techniques
QFN:	Quad Flat Non-leaded
PCB:	Printed Circuit Board
BOM:	Bill Of Materials
Sij:	Scattering Parameters
RoHS:	Restriction of the use of certain Hazardous Substances
Lead-free:	Part of the RoHS directive (Leadless)
DI:	Deionised water
MMIC:	Monolithic Microwave Integrated Circuit
THB:	Temperature and Humidity Biased
HOTL:	High Temperature Operating Life
Pb:	Lead
MSL:	Moisture Sensitivity Level
CTE:	Coefficient of thermal expansion
CPK:	Or CpK is a process capability index.

8. References

[1]: Mil-Std-883

Bât. Charmille - Parc SILIC - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34

Table of contents

1. FAB type package general presentation 1

2. Package outline 2

3. Assembly recommendations 2

3.1. Package bottom-side coplanarity 2

3.2. Solder past selection 3

3.3. Recommendations for solder past printing process selection 4

3.3.1. Solder mask design recommendations 5

3.3.2. Stencil printer recommendations 6

4. Recommended PCB design 8

5. ANNEX 1: FAB package outline 10

6. ANNEX 2: Recommended PCB electrical design 11

7. Glossary 12

8. References 12

Table of contents 13

Bât. Charmille - Parc SILIC - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34

Recommended package footprint

Refer to the application note AN0017 available at http://www.ums-gaas.com for package foot print recommendations.

SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at http://www.ums-gaas.com.

Recommended ESD management

Refer to the application note AN0020 available at http://www.ums-gaas.com for ESD sensitivity and handling recommendations for the UMS package products.

Contacts:

Web site: www.ums-gaas.com
email: mktsales@ums-gaas.com
Phone: 33 (1) 6933 0226 (France)
1 973 812 2139 (USA)
8 621 610 31665 (China)

Information furnished is believed to be accurate and reliable. However **United Monolithic Semiconductors S.A.S.** assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of **United Monolithic Semiconductors S.A.S.**. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. **United Monolithic Semiconductors S.A.S.** products are not authorised for use as critical components in life support devices or systems without express written approval from **United Monolithic Semiconductors S.A.S.**

Bât. Charmille - Parc SILIC - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34