

Application Note related to UMS products - Electrostatic Discharge Sensitivity Data -

GaAs Monolithic Microwave IC

1. General considerations on ESD sensitivity

GaAs Monolithic Microwave IC's are known to have a high sensitivity to the Electrostatic Discharge and fundamental ESD* control principles have to be followed from the fabrication of the products up to their integration in the system or the equipment.

Both in the front-end and in the back-end, UMS is taking care of this ESD concern using the basics of the IEC 61340-5-1 standard [1]. After shipping by the UMS supply chain the GaAs products should be also safely handled to assure the best ESD protection.

This document gives some information about how to proceed with the UMS products.

2. Components characteristics

2.1. Field Effect Transistors

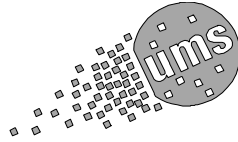
Most of the UMS products include biased FET's* in a typical common source configuration. So an external ESD could run more or less through the biasing circuits to the transistor from the DC pads (V_{gs} , V_{ds}) or through the matching circuits from the Input / Output pads.

Therefore, positive or negative discharges can be conducted through the Schottky gate junction or the FET channel; the greatest vulnerability being for negative discharges into the gate and for both type of pulses into the smallest devices; so the sensitivity is higher in stages with low gate width. In the same way, technologies with larger gate length are expected to be more robust.

2.2. Diodes

Often encountered in mixers or up/down converters, diodes have a similar ESD sensitivity to that of Field Effects Transistors. Nevertheless, differences are noticed in relation with the Anode area; we are expecting greater robustness for a BES* diode ($1\mu\text{m}$ gate length) than for a PH25* diode ($0,25\mu\text{m}$ gate length) with the same Anode width.

As the diode periphery used for design is small especially for high frequency products, care should be taken from the ESD protection integrated in the biasing circuits without degradation of the performances – see § 3.2.



Besides ESD characterisation showing that diodes are more sensitive to negative pulses on Anode contact than positive discharges, this should be taken into account in the ESD protection.

* see glossary

2.3. Bipolar transistors

Some UMS products includes biased HBT's* in a typical common emitter configuration. Thus through the biasing circuits from the DC pads (I_{be}, V_{ce}) or through the matching circuits from the Input/Output pads, an external ESD can reach the bipolar transistor.

ESD failure modes in bipolar devices are usually located at the emitter-base junction due to a lower avalanche breakdown voltage. The degradation is accompanied by a decrease of the current gain β and an increase of the base current I_{be}.

Even with a collector to base stress condition, the forward biasing of the emitter-base junction begins due to the current flowing in the base after the collector-base avalanching; the high vulnerability being for the smallest devices.

2.4. Passive components

Metallic or resistive transmission lines can handle for short time typical ESD discharges significantly higher in current than the DC maximum ratings. Although the resistance shows no noticeable drift during high transients, a slight increase is observed just before the failure. The result depends on the physical size of the line, with a larger vulnerability for the small geometries.

Furthermore, interdigitated or coupled structures and inductances have a great susceptibility to high ESD pulse voltages leading to a local burnout at the failure level.

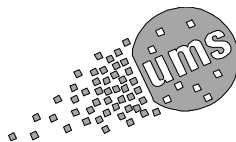
While in matching circuits the capacitors are often of small area (A), they are of bigger size in the decoupling circuits contributing with resistors ($\tau = RC$) during the transient phase to a better protection of the internal elements of the product. Also, larger dielectric conductivity is able to dissipate more ESD energy $E = \frac{1}{2} \epsilon_0 \epsilon_r U^2 A / d$ (thickness d) . And in relation with the dielectric breakdown ($\sim 1\text{Volt} / \text{nm Si}_x\text{N}_y$ thickness), the best results were evidenced with lower capacitance densities. [8]

3. Products Characterisation

3.1. Class of models

Three models are intended to represent the situations the products are facing up to Electrostatic Discharges:

- ✓ HBM* model simulating the field failures caused by human handling [5]
- ✓ MM* model the ability to reproduce the failures due to machine handling [4]
- ✓ CDM* model considering the situations where charge initially resides on a device via triboelectric rubbing or sliding in shipping tubes [3]



3.2. Design consideration

In order to reduce the sensitivity to Electrostatic Discharge of the UMS products – or increase the ESD class, one solution is to introduce clamping elements between the critical points such as the input/output accesses and the ground pad of the products. So that if the ESD induced voltage exceeds the clamping voltage, the element turns on and becomes a low impedance shunt to divert the high currents to the ground.

For this purpose, a set of several series diodes in two parallel and anti parallel paths can contribute to minimize the ESD damage; the size and the number of elements are determined during the design phase taking into account the technology and the targeted specifications of the product.

As a trade-off between the product characteristics, the frequency range and the chip area, alternative configurations can also be used to reduce ESD sensitivity:

- ✓ Input/output matching with short circuited stub
- ✓ Increase the size of the active elements
- ✓ Increase the area of the decoupling capacitors
- ✓ Several series capacitors to increase the voltage threshold
- ✓ Prefer cell filters with a topology using parallel inductors
- ✓ Isolate the gate access behind series resistors

So the ESD robustness can be improved, but as a consequence, in general, the RF accesses are grounded from the DC point of view – see specific information given in the datasheets.

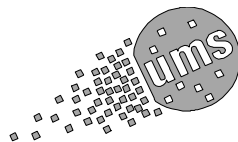
3.3. ESD class for UMS products

The destructive power of ESD has revealed essentially three basic failure mechanisms in the products that are junction burnout, Si_xN_y oxide punch-through and metallisation burnout. These mechanisms are thermal in nature with damage occurring when the temperature of the affected region dissipating the ESD pulse energy rises to the melting point.

While the Si_xN_y oxide punch-through is related to the dielectric breakdown (~1V/nm thickness), the two other mechanisms are linked to electro thermo migration with for example current densities in excess in metallisation of 10⁷ A/cm² within about 1μs. [6]

3.3.1. FET products

Most of the UMS products are based on Hemt technology so many results are available even if the ESD values are more related to the product design itself than to the production process. Some typical results on UMS products are presented hereafter:



Function	Technology	Failure level (Volts)			Comments
		HBM	MM	CDM	
LNA	Hemt – 0,25µm	300	>400		limited by low series capacitors in output access
Attenuator	Mesfet – 0,7µm	>1000	200		with cold FET's of large size
Down-conv	Hemt – 0,25µm	400			small size transistor degradation on FI port
MPA	Hemt – 0,15µm	>500	>500		thanks to specific filter circuits
Down-conv	Hemt – 0,25µm	>500	300	> 200	behind RC filters low size FET's degradation
SP4T	Hemt – 0,25µm	250			limited by the output series capacitors
HPA	pHemt – 0,25µm	250	100		parallel capacitors on DC pads short circuited
HPA	pHemt – 0,15µm	>500	400		with RF designed-in protections
Up-conv	pHemt – 0,25µm	250	30		G-S diode degradation with negative pulses
		>500	200	>200	with on board RC filter
HPA	pHemt – 0,25µm	> 500			through efficient RC filters and series capacitors
MPA	pHemt – 0,15µm	> 500	> 500		with built-in ESD protections
LNA	Hemt – 0,25µm	250	100		with small size capacitors in the RF accesses
LNA	Hemt – 0,25µm		70		without any specific RC filter at RF accesses

> in relation with limited characterization

3.3.2. HBT products

As for the FET products, the ESD values are more related to the product design itself than to the production process. Some typical results on UMS products are presented hereafter:

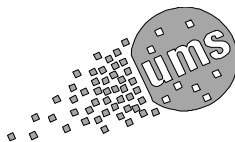
Function	Technology	Failure level (Volts)			Comments
		HBM	MM	CDM	
HPA	HBT 2µm - 250pF	1000			through series capacitor and parallel inductors
	HBT 2µm - 250pF	400			RF access limited by two series capacitors
Mixer	HBT 2µm - 250pF			250	sensitive accesses protected by diode cells
VCO	HBT 2µm - 250pF	>500	450		with high value resistors and parallel capacitors
VCO	HBT 2µm - 300pF	300			limited by the diode cell protection size
VCO	HBT 2µm - 450pF	>500			through a RC filter which fits with high τ values
VCO	HBT 2µm - 300pF		50		low RF impedance in the output access
VCO	HBT 2µm - 300pF		125		small diodes in the temperature control cell
VCO	HBT 2µm - 250pF	>1000			limited by the dielectric leakage in the output port

> in relation with limited characterization

3.3.3. Diode products

As diodes are the most ESD sensitive active component an HBM characterization was undertaken directly on mono finger diodes of 5µm width and 1µm length:

Technology	Failure level (Volts)		Comments
	Three Negative discharges	Three Positive discharges	
Diode 1µm	69	100	junction burnout with high reverse voltages



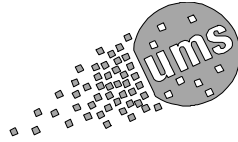
4. Handling precaution

The fundamental ESD control principles that form the basis of IEC 61340-5-1 implemented in UMS [1] are as follows:

- a) Avoid a discharge from any charged, conductive object (personnel, equipment) into the ESDS*. This can be accomplished by bonding or electrically connecting all conductors in the environment, including personnel, to a known EBP* ground or contrived ground. This attachment creates an equipotential balance between all items and personnel. Electrostatic protection can be maintained at a potential different from “zero” voltage ground potential, as long as all items in the system are at the same potential.
- b) Avoid a discharge from any charged ESD sensitive device (the charging can result from direct contact and separation or can be field induced. Necessary insulators in the environment cannot lose their electrostatic charge by attachment to ground. Ionization systems provide neutralization of charges on these necessary insulators (circuit board materials and some device packages are examples of necessary insulators). Assessment of the ESD hazard created by electrostatic charges on the necessary insulators in the work place is required to ensure that appropriate actions are implemented, according to the risk.
- c) Once outside of an electrostatic discharge protected area (referred to as an EPA*) it is often not possible to control the above items, therefore, ESD protective packaging may be required. ESD protection can be achieved by enclosing ESD sensitive products in static protective materials, although the type of material depends on the situation and destination. Inside an EPA, low charging and static dissipative materials may provide adequate protection. Outside an EPA, low charging and static discharge shielding materials are recommended.

The 100V HBM limit was selected in the IEC 61340-5-1 standard as a baseline susceptibility threshold but the product documentation would identify that some ESDS with sensitivities of less than 100V HBM were being handled.

The user guide IEC 61340-5-2 - [2] has been produced for individuals and organizations that are faced with controlling electrostatic discharge. It provides guidance that can be used for developing, implementing and monitoring an electrostatic discharge control program in accordance with IEC 61340-5-1.



5. ESD versus EOS*

One difference between Electrical Overstress (EOS) and Electrostatic Discharge (ESD) is the voltage magnitude which is typically in the range of tens to hundred of volts for EOS while in ESD voltage pulses are one to two orders of magnitude higher. The short duration of an ESD (1ns to 1 μ s) compared to an EOS (1 μ s to 1ms) is another characteristic.

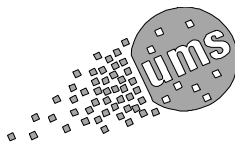
In EOS large currents flow through device junctions because of excessive applied fields that arise from weak protections due to a trade-off with performances in circuit design, mishandling or voltage pulses.

In ESD high voltages are generated by static charge, signal-switching transients, electromagnetic pulses, spacecraft charging, high-power electromagnetic and radio-frequency interference or lightning [6].

All these effects can occur during device processing, assembly into systems and/or use of the UMS product by the customers. In some cases it may result in latent defects which are not detected as changes in device characteristics, but which increase device susceptibility to failure in the future.

6. Glossary

BES	: 1 μ m UMS Diode Technology
CDM	: Field-Induced Charged-Device Model
EBP	: Earth Bonding Point
EOS	: Electrical Overstress
EPA	: ESD Protective Area
ESD	: ElectroStatic Discharge
ESDS	: ESD-Sensitive devices
FET	: Field Effect Transistor
HBM	: Human Body Model
HBT	: Heterojunction Bipolar Transistor
Hemt	: High Electron Mobility Transistor
MM	: Machine Model
MMIC	: Monolithic Microwave Integrated Circuit
pHemt	: Pseudomorphic Hemt
PH25	: 0,25 μ m UMS Hemt Technology
Si _x N _y	: dielectric for capacitor and glassivation



7. References

- [1] International Standard IEC 61340 - Part 5-1 Protection of electronic devices from electrostatic phenomena – General Requirements – Ed 1.0 2007-08
- [2] International Standard IEC 61340 – Part 5-2 Protection of electronic devices from electrostatic phenomena – User guide – Ed 1.0 2007-08
- [3] JESD22-C101 Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components - Field-Induced Charged-Device Model
- [4] JESD22-A115 Electrostatic Discharge (ESD) Sensitivity Testing - Machine Model (MM)
- [5] JESD22-A114 Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)
- [6] Reliability and Failure of Electronic Materials and Devices – Milton Ohring – Academic Press ©1998
- [7] ESD program management – A Realistic Approach to Continuous Measurable Improvement in Static Control - edited by G. Theodore Dangelmayr - Chapman & Hall - ©1999
- [8] SiN Capacitors and ESD – G.I. Drandova, J.M. Beall, K.D. Decker – CS MANTECH Conference, April 24-27, 2006, Vancouver, British Columbia, Canada

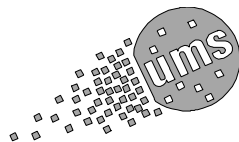


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