United Monolithic Semiconductors

CHA8154-99F

7.25-7.75GHz High Power Amplifier

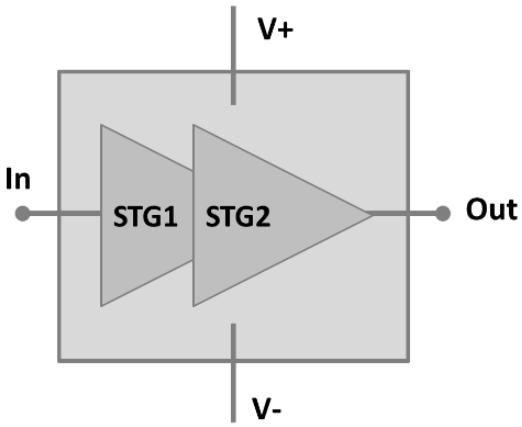
GaN Monolithic Microwave IC

Description

The CHA8154-99F is a two-stage monolithic GaN Power Amplifier operating between 7.25 and 7.75GHz and typically providing 18W Output Power at 49% of Power Added Efficiency. This amplifier exhibits more than 6W linear Output Power associated to 17dBc NPR and 42% Power Added Efficiency. It also provides a typical small signal gain of 28.5dB.

This amplifier is well suited for radar and space communications as well as telecommunications.

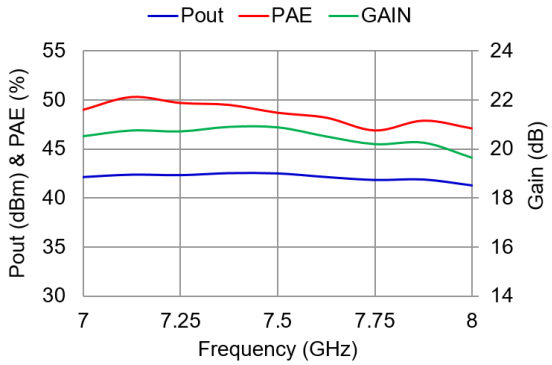
The circuit is manufactured using a space evaluated, robust GaN-on-SiC HEMT process and is provided as a bare die for direct integration into hybrid circuits.



Main Features

- Frequency range: 7.25 – 7.75 GHz
- High output power: 18W
- High PAE: 49%
- Linear Gain: 28.5dB
- DC bias: VD = 28V & Idq = 330mA
- Chip size: 5.14 x 4.22mm²
- Available as bare die

V_D = 28V, I_{Dq} = 330mA, $T_{backside}$ = 25°C,
Psat (8dBcompression)



Main Electrical Characteristics

$T_{backside}$ = +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	7.25		7.75	GHz
Gain	Linear Gain		28.5		dB
Pout	Output Power @ Psat (8dB compression)		42.6		dBm
PAE	Power Added Efficiency @ 8dB compression		49		%

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Specifications

$T_{backside}$ = +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	7.25		7.75	GHz
Gain	Linear Gain		28.5		dB
IRL	Input Return Loss		14		dB
ORL	Output Return Loss		16		dB
Psat	Saturated Output Power (@8dBcomp)		42.6		dBm
PAE	Associated Power Added Efficiency		49		%
Pdiss	Dissipated Power @ Psat (8dBcomp)		18.9		W
AMAM	AM/AM @ Psat (8dBcomp)		8		dB
AMPM	AM/PM @ Psat (8dBcomp)		14		°
Idq	Quiescent Drain Current		330		mA
Vd	Drain Voltage		28		V
Vg	Gate Voltage		-3.5		V
Id	Associated Drain Current @ Psat (8dBcomp)		1310		mA

Absolute Maximum Ratings (1)

$T_{backside}$ = +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	45	V
Vg	Gate bias voltage	-25	V
Pin	Maximum peak input power overdrive	28	dBm
Pdiss	Maximum dissipated power at $T_{backside}$ =115°C for Tj=230°C	60	W
Tj	Junction temperature(2)	230	°C
Tstg	Storage temperature range	-55 to +150	°C

(1) Absolute Maximum Ratings (AMR): Absolute maximum ratings are limiting values of operating and environmental conditions that are applicable to any electronic device of a specified type as defined by its published data. Absolute maximum ratings should not be exceeded under any operating condition. Operating this device above anyone of these parameters may cause permanent damage.

(2) See Device Thermal Performances section.

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Recommended Operating Range (1), (2), (3)

Symbol	Parameter	Values	Unit
Vd	Drain Bias Voltage	15 to 30	V
Idq	Quiescent Drain Current (without RF signal)	170 to 560	mA
Vg	Gate Bias Voltage	-5 to -2.5	V
Tj	Maximum Junction Temperature(3)	200	°C
Pin	Maximum Input Power	26	dBm

(1) Electrical performances are defined for specified test conditions
(2) Electrical performances are not guaranteed over all recommended operating conditions
(3) See Device Thermal Performances section.

Temperature Range

$T_{backside}$	Operating Temperature Range	-20 to +115	°C
Tstg	Storage Temperature Range	-55 to +150	°C

Typical Bias Conditions

$T_{backside}$ =+25°C

Symbol	Pad Name(N°)	Parameter	Values	Unit
Vg	G1H(3), G2H(6), G1B(14), G2B(11)	Gate Voltage	-3.5	V
Vd	D1H(5), D2H(8), D1B(12), D2B(9)	Drain Voltage	28	V

“Power ON” sequence

1. Bias HPA gate voltage at Vg close to Vpinch-off (Typically: Vg ≈ -5V)
2. Apply Vd bias voltage (Typically: Vd = 28V)
3. Increase gate voltage Vg up to quiescent bias drain current Idq (Around -3.5V)
4. Apply RF signal

“Power OFF” sequence

1. Turn off RF signal
2. Bias HPA gate voltage at Vg close to Vpinch-off (Typically: Vg ≈ -5V)
3. Check that quiescent bias drain current Idq is close to 0mA
4. Turn Vd bias voltage to 0V
5. Check that quiescent bias drain current Idq is close to 0mA
6. Turn Vg bias voltage to 0V

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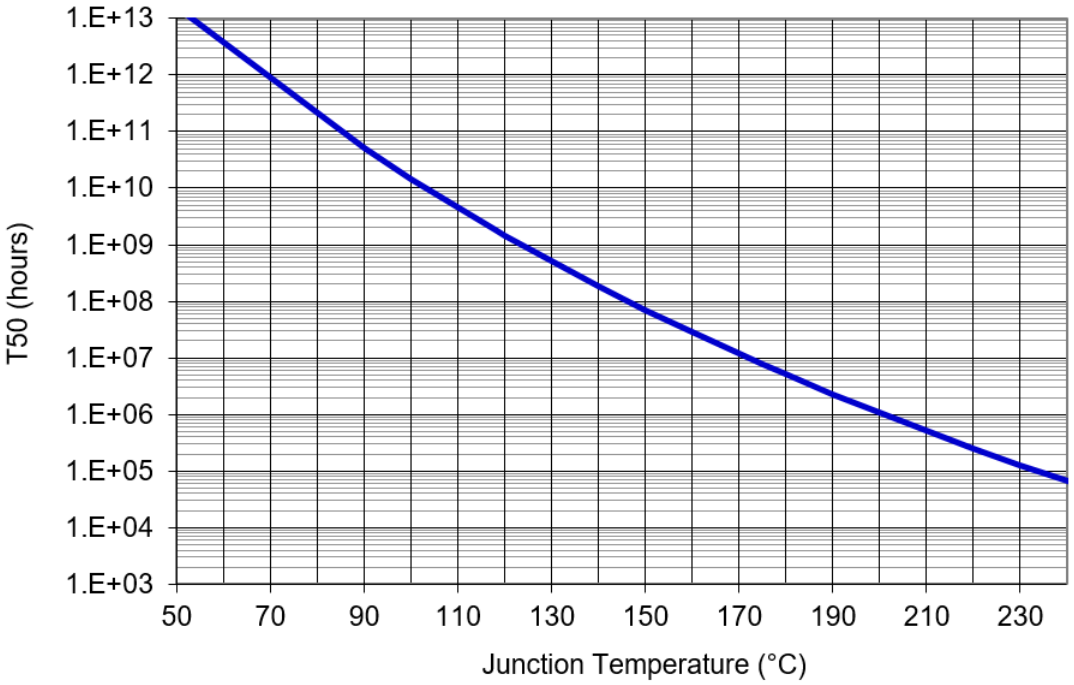
Device thermal performances

All figures given in this section are obtained assuming the chip backside is only cooled down by the conduction through the test board (no convection mode is considered).
The temperature is monitored at the chip backside ($T_{backside}$).
The system maximum temperature must be adjusted in order to guarantee that T_J remains below the maximum value specified in the Recommended Operating Range table.
The system PCB must be designed to comply with this requirement.

Parameter	Biasing conditions	$T_{junction}$ (°C)	R_{TH} (°C/W)	T50 (hours)
R_{TH} (1) Thermal Resistance	Vd=28V, Idq=330mA, $T_{backside}$=85°C, Pdiss=22W(Sat) Pin=24.6dBm Pout=42.3dBm	122	1.70	1.8E+09

(1) A Thermal resistance measured to back of the chip



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Typical Board Sij parameters

$T_{backside}$ = +25°C, Vd = 28V, Idq = 330mA

FREQ	dBS11	PhS11	dBS12	PhS12	dBS21	PhS21	dBS22	PhS22
GHz	dB	°	dB	°	dB	°	dB	°
0.50	-0.03	-37.42	-78.68	43.52	-34.49	-2.95	-0.01	-38.61
1.00	-0.81	-75.44	-95.82	-72.08	-22.35	138.93	-0.11	-76.83
1.50	-0.53	-105.91	-106.57	178.38	-6.45	-25.70	-0.29	-114.81
2.00	-0.55	-143.80	-88.49	138.21	-15.08	-136.24	-0.34	-153.35
2.50	-0.75	179.08	-75.39	100.08	-16.79	164.78	-0.47	168.20
3.00	-1.04	142.20	-70.71	38.42	-20.13	89.46	-0.55	129.92
3.50	-1.31	105.86	-68.09	13.76	-30.64	135.49	-0.58	91.23
4.00	-1.56	69.14	-65.18	-17.37	-16.50	108.31	-0.61	51.95
4.50	-1.84	31.66	-62.69	-56.13	-9.40	55.40	-0.61	11.74
5.00	-2.18	-6.66	-61.63	-96.66	-2.87	-1.36	-0.67	-30.85
5.50	-2.63	-46.38	-62.04	-135.96	3.78	-63.99	-0.96	-76.83
6.00	-3.40	-89.40	-61.32	175.63	12.05	-128.86	-1.62	-132.58
6.50	-5.30	-139.16	-64.81	-6.40	22.72	132.17	-6.47	141.59
7.00	-10.40	178.39	-50.09	-164.53	28.34	-8.18	-15.21	-153.69
7.50	-13.82	131.72	-47.09	86.23	28.66	-137.50	-15.91	87.12
8.00	-13.84	-29.44	-46.49	-26.90	28.23	90.74	-9.05	-36.29
8.50	-9.32	-160.30	-51.95	-152.14	21.65	-45.60	-3.20	-130.54
9.00	-11.95	124.31	-57.96	120.95	12.85	-145.62	-2.40	170.58
9.50	-16.72	47.55	-64.40	77.13	4.95	129.20	-1.94	126.18
10.00	-16.74	-72.71	-67.94	76.29	-2.83	49.83	-1.54	86.44
10.50	-10.30	-154.80	-62.47	83.38	-11.16	-24.89	-1.23	49.17
11.00	-6.22	146.56	-60.51	57.30	-21.03	-92.74	-1.02	13.50
11.50	-3.92	94.50	-55.55	10.37	-35.84	-136.39	-0.88	-20.64
12.00	-2.60	48.92	-54.88	-40.29	-36.22	-78.17	-0.80	-52.94
12.50	-1.86	6.44	-57.51	-81.96	-31.46	-137.79	-0.73	-84.52
13.00	-1.38	-32.07	-59.70	-123.31	-31.78	130.38	-0.68	-114.11
13.50	-1.14	-67.99	-68.40	-157.21	-38.49	45.74	-0.64	-143.38
14.00	-0.96	-101.89	-76.99	-74.70	-45.22	-12.82	-0.60	-171.87
14.50	-0.85	-133.61	-63.89	-87.46	-49.74	-63.57	-0.56	160.33
15.00	-0.80	-164.52	-59.38	-125.85	-51.90	-111.92	-0.55	132.68
15.50	-0.78	165.71	-58.88	-163.44	-54.08	-149.73	-0.56	105.25
16.00	-0.78	135.41	-60.06	163.41	-56.72	173.96	-0.60	77.56
16.50	-0.75	105.33	-63.86	152.62	-59.79	152.93	-0.61	49.41
17.00	-0.78	75.85	-63.30	171.20	-60.17	167.23	-0.62	22.03
17.50	-1.10	47.03	-56.39	160.22	-55.42	147.54	-0.62	-5.09
18.00	-0.74	22.97	-57.25	130.17	-59.65	125.11	-0.62	-32.41
18.50	-0.54	-4.48	-53.43	126.12	-54.15	126.94	-0.66	-60.18
19.00	-0.44	-30.82	-48.88	98.30	-49.02	101.23	-0.80	-90.15

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Typical Board Sij parameters

$T_{backside}$ = +25°C, Vd = 28V, Idq = 470mA

FREQ	dBS11	PhS11	dBS12	PhS12	dBS21	PhS21	dBS22	PhS22
GHz	dB	(°)	dB	(°)	dB	(°)	dB	(°)
0.50	-0.02	-37.38	-89.84	-31.87	-33.36	-3.73	-0.01	-38.57
1.00	-0.80	-75.19	-93.34	-116.96	-21.11	136.59	-0.10	-76.79
1.50	-0.52	-106.00	-85.08	164.77	-5.25	-26.64	-0.29	-114.80
2.00	-0.53	-143.91	-74.61	103.87	-13.83	-137.24	-0.34	-153.33
2.50	-0.75	178.96	-79.60	50.39	-15.56	163.57	-0.46	168.23
3.00	-1.04	142.06	-70.32	43.62	-18.92	88.42	-0.55	129.96
3.50	-1.32	105.69	-68.72	22.02	-29.32	134.54	-0.57	91.28
4.00	-1.57	68.99	-66.94	-17.74	-15.17	106.62	-0.60	52.00
4.50	-1.85	31.45	-64.11	-57.75	-8.08	53.01	-0.60	11.79
5.00	-2.21	-6.93	-61.78	-91.39	-1.58	-4.48	-0.66	-30.78
5.50	-2.69	-46.77	-61.70	-132.38	5.01	-67.86	-0.96	-76.67
6.00	-3.51	-90.02	-62.01	179.07	13.17	-133.84	-1.65	-132.14
6.50	-5.59	-139.59	-67.99	-2.04	23.51	126.25	-6.54	145.34
7.00	-10.67	179.25	-51.07	-168.96	28.89	-12.22	-16.05	-166.62
7.50	-14.38	129.03	-47.99	85.80	29.30	-141.36	-15.28	78.64
8.00	-13.41	-40.67	-47.57	-27.72	28.50	85.76	-8.29	-42.09
8.50	-8.86	-162.52	-52.84	-148.91	21.71	-47.12	-3.18	-131.86
9.00	-11.22	122.17	-58.69	130.03	13.04	-145.96	-2.34	170.32
9.50	-15.56	44.31	-65.58	86.94	5.18	129.53	-1.88	125.92
10.00	-15.73	-71.07	-67.69	81.98	-2.58	50.96	-1.50	86.14
10.50	-9.96	-154.20	-61.59	86.70	-10.85	-22.89	-1.22	48.96
11.00	-6.08	146.51	-59.56	58.86	-20.61	-90.00	-1.01	13.47
11.50	-3.87	94.51	-55.52	10.42	-35.23	-133.35	-0.88	-20.75
12.00	-2.57	48.92	-54.81	-38.07	-35.47	-75.71	-0.80	-52.91
12.50	-1.86	6.48	-57.02	-83.33	-30.67	-135.84	-0.72	-84.47
13.00	-1.37	-31.96	-59.36	-119.89	-31.10	132.22	-0.67	-114.07
13.50	-1.13	-67.89	-68.06	-149.55	-37.72	49.50	-0.63	-143.27
14.00	-0.95	-101.78	-72.96	-89.11	-44.46	-9.31	-0.58	-171.77
14.50	-0.84	-133.44	-62.94	-84.19	-48.96	-59.65	-0.56	160.46
15.00	-0.78	-164.36	-58.97	-129.67	-51.64	-107.84	-0.54	132.81
15.50	-0.77	165.95	-58.32	-158.21	-53.58	-149.32	-0.55	105.39
16.00	-0.76	135.61	-60.17	162.84	-56.02	170.04	-0.59	77.70
16.50	-0.73	105.52	-63.66	161.42	-60.03	154.27	-0.60	49.50
17.00	-0.76	75.99	-62.47	177.08	-60.35	158.27	-0.60	22.11
17.50	-1.08	46.94	-56.92	162.91	-55.17	145.36	-0.61	-4.99
18.00	-0.76	22.97	-57.10	127.46	-59.06	126.03	-0.61	-32.35
18.50	-0.54	-4.32	-53.37	125.72	-54.19	129.41	-0.65	-60.09
19.00	-0.44	-30.60	-48.83	97.64	-48.82	101.01	-0.79	-90.04

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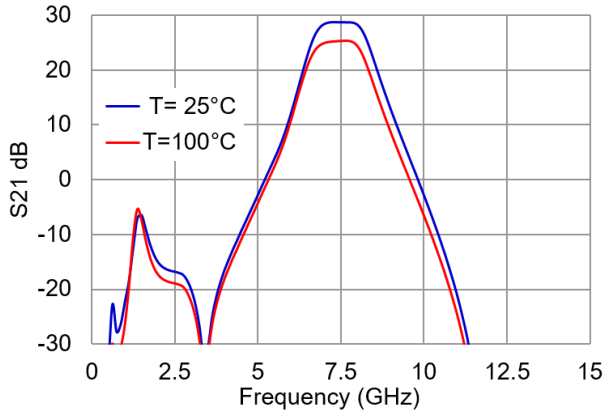
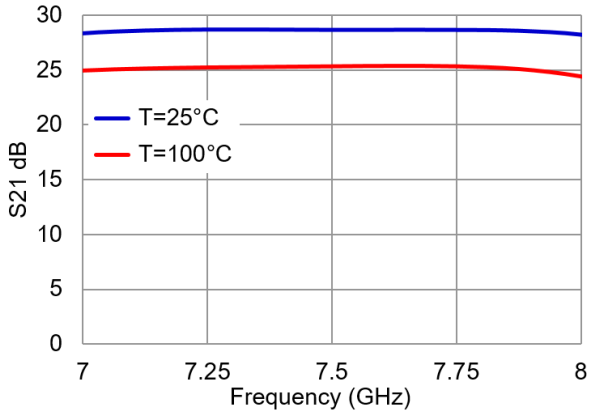
Typical Board Measurements: Small Signal Performance

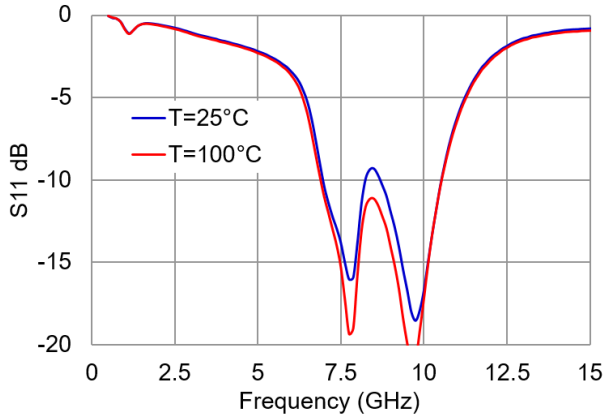
Test conditions: CW, Vd = 28V, Idq = 330mA@25°C, $T_{backside}$ = 25°C / 100°C

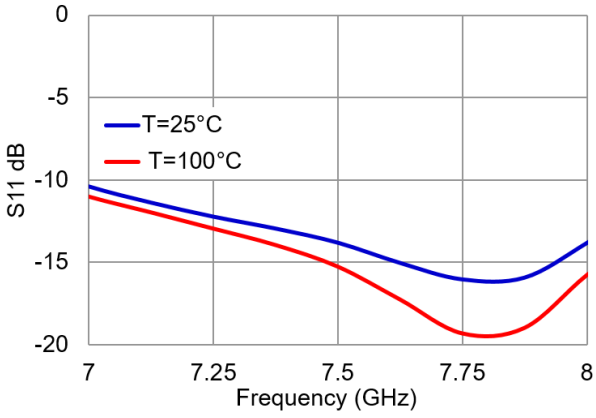
Linear Gain vs. Frequency vs. Temperature



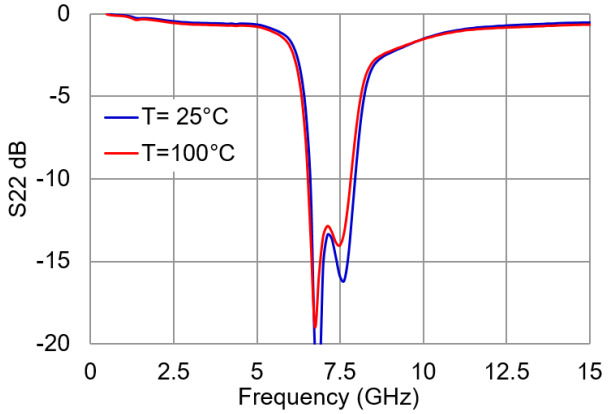


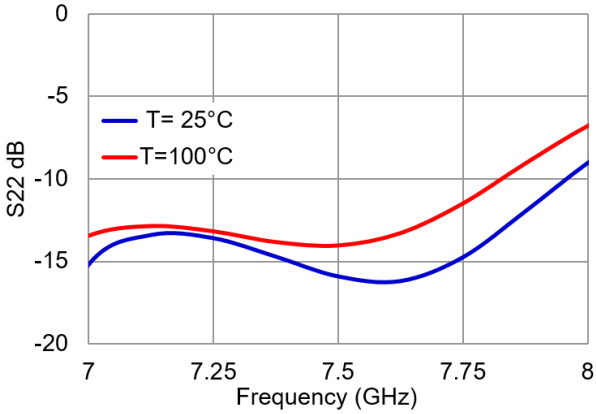
Input Return Loss vs. Frequency vs. Temperature





Output Return Loss vs. Frequency vs. Temperature





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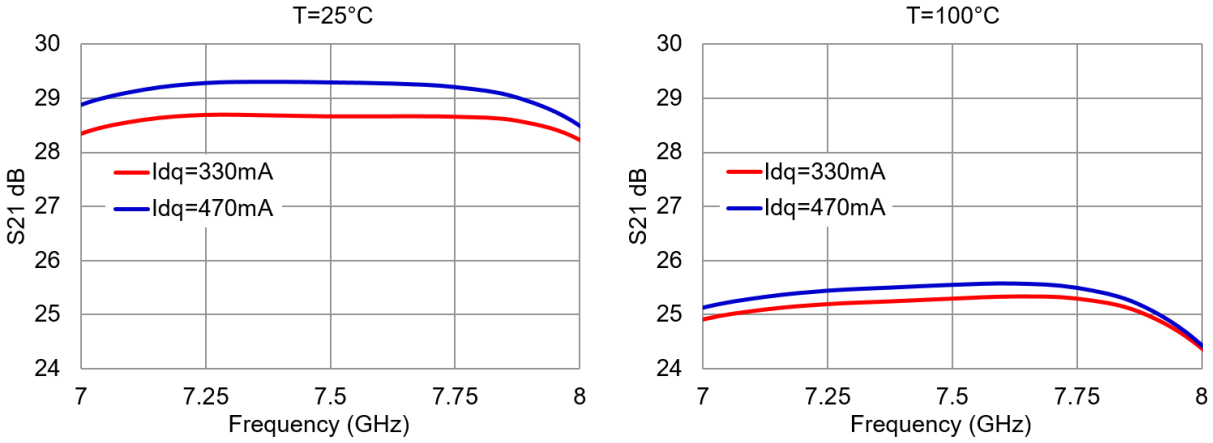
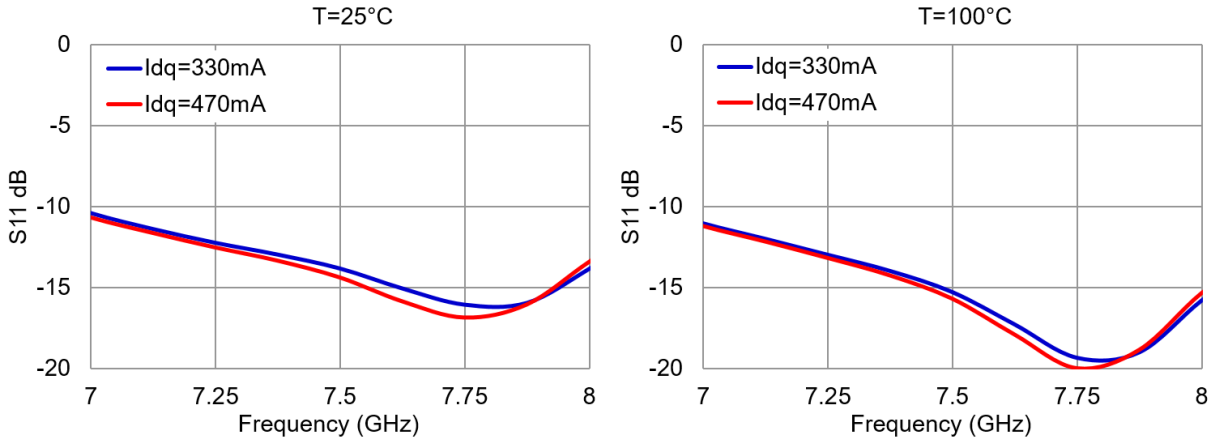
Typical Board Measurements: Small Signal Performance

Test conditions: CW, Vd = 28V, Idq = 330mA / 470mA @25°C, $T_{backside}$ = 25°C / 100°C

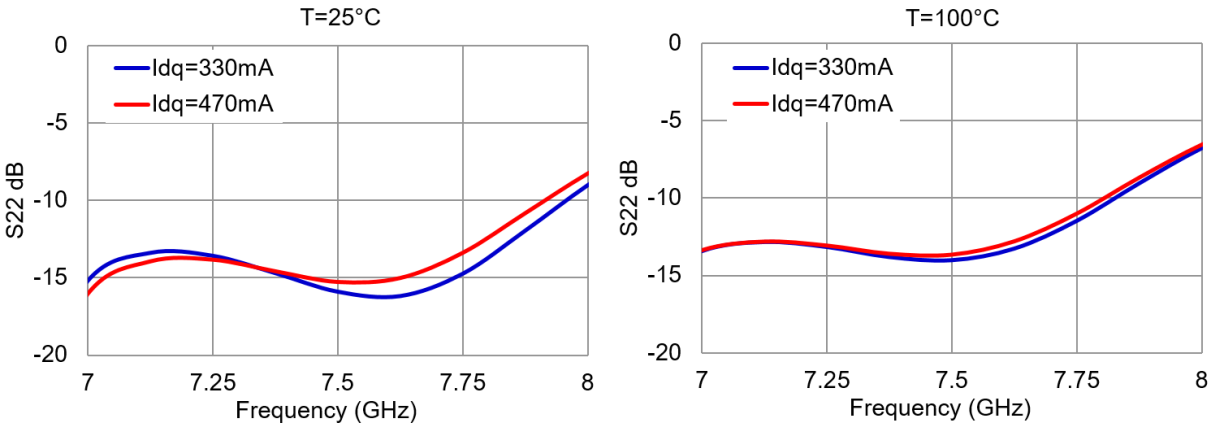
Linear Gain vs. Frequency vs. biasing current Idq



Input Return Loss vs. Frequency vs. biasing current Idq



Output Return Loss vs. Frequency vs. biasing current Idq



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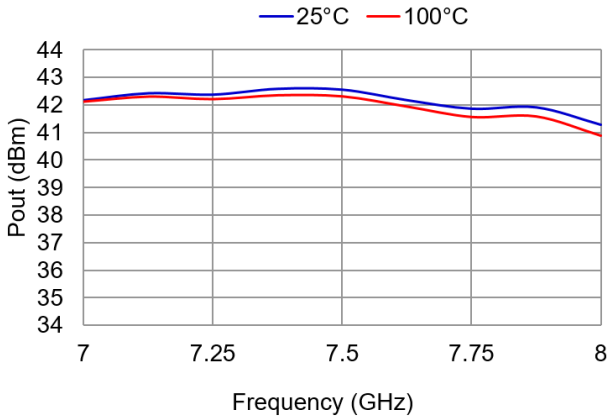
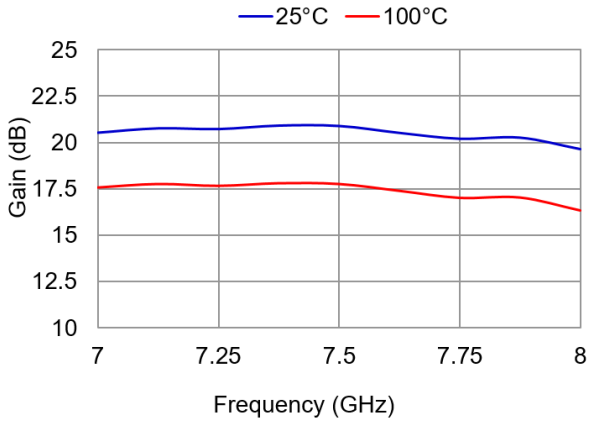
Typical Board Measurements: Large Signal Performance

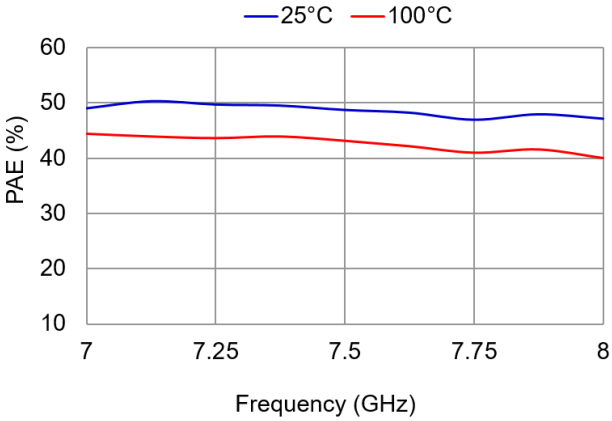
Test conditions: CW, Vd = 28V, Idq = 330mA, $T_{backside}$ = 25°C / 100°C at 8dBcomp

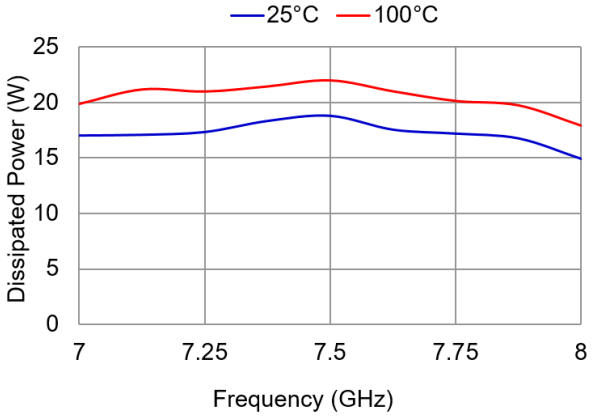
Output Power and Gain vs. Frequency



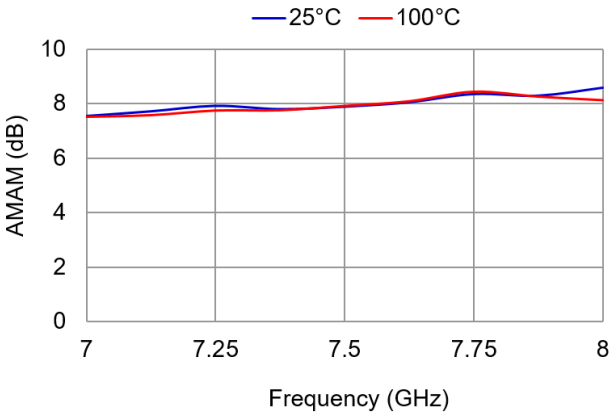


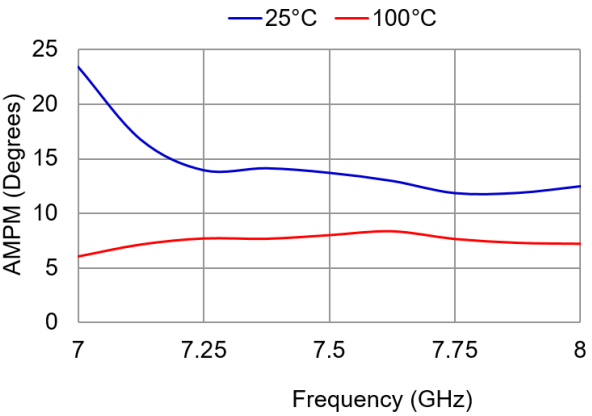
Power Added Efficiency (PAE) and Dissipated Power vs. Frequency





AMAM & AMPM vs. Frequency





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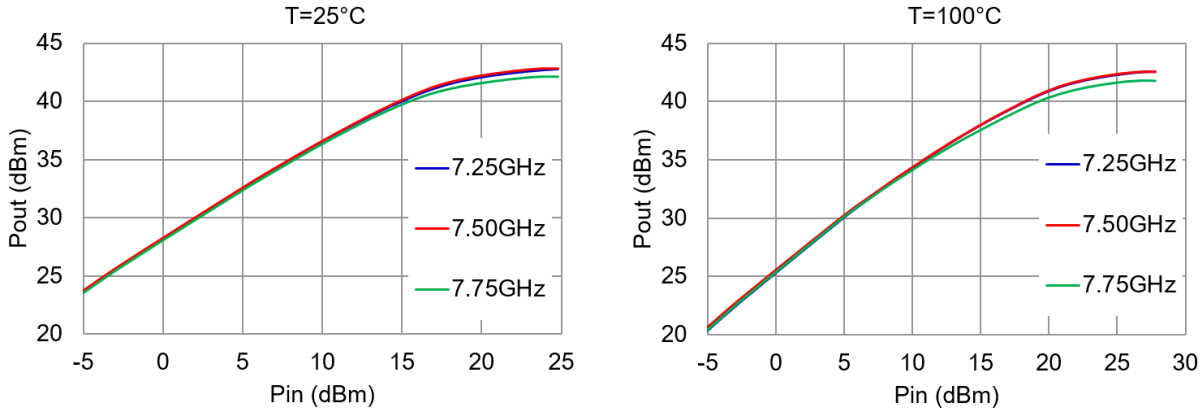
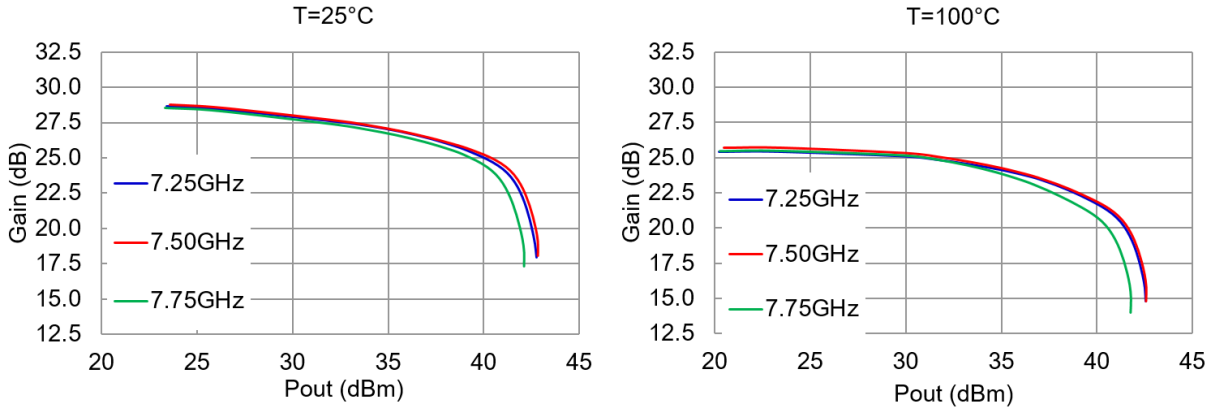
Typical Board Measurements: Large Signal Performance

Test conditions: CW, Vd = 28V, Idq = 330mA, $T_{backside}$ = +25°C / 100°C

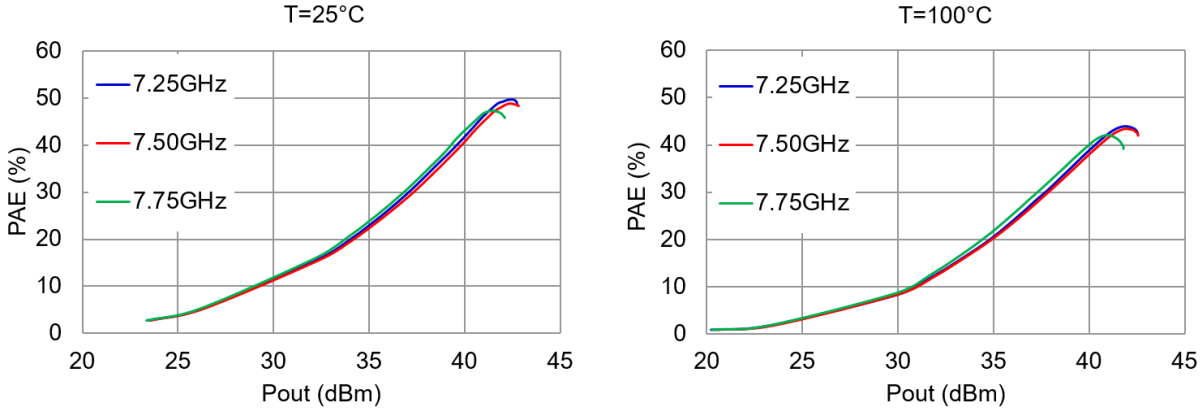
Output Power vs. Input Power (Pin) vs. Frequency



Gain vs. Output Power (Pout) vs. Frequency



Power Added Efficiency vs. Output Power vs. Frequency



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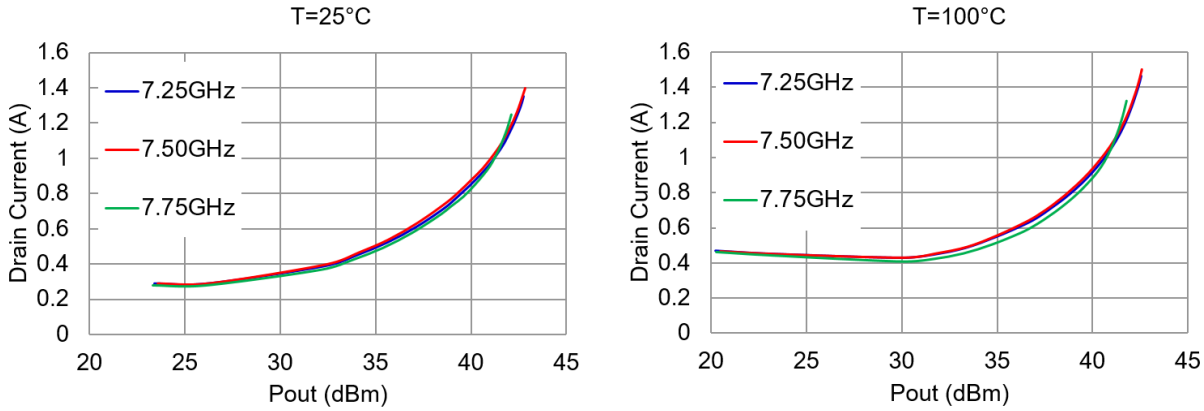
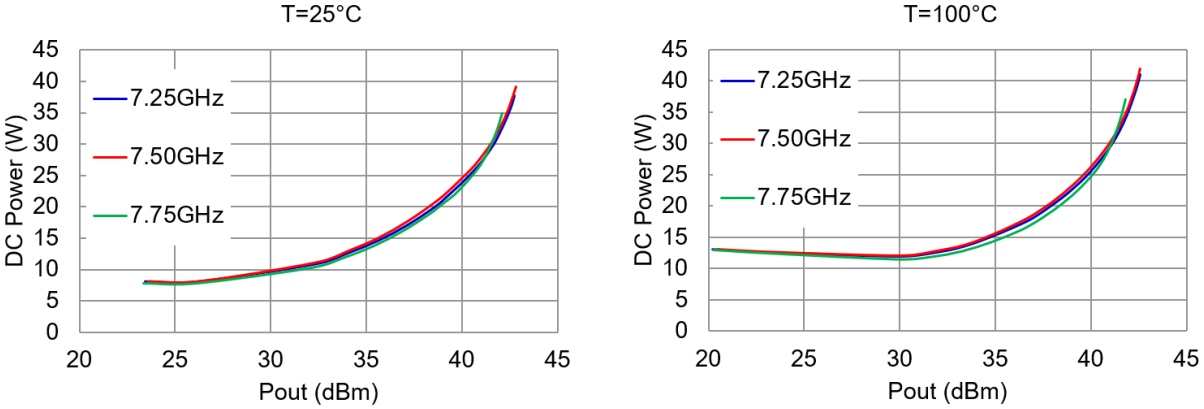
Typical Board Measurements: Large Signal Performance

Test conditions: CW, Idq = 330mA, $T_{backside}$ = +25°C / 100°C

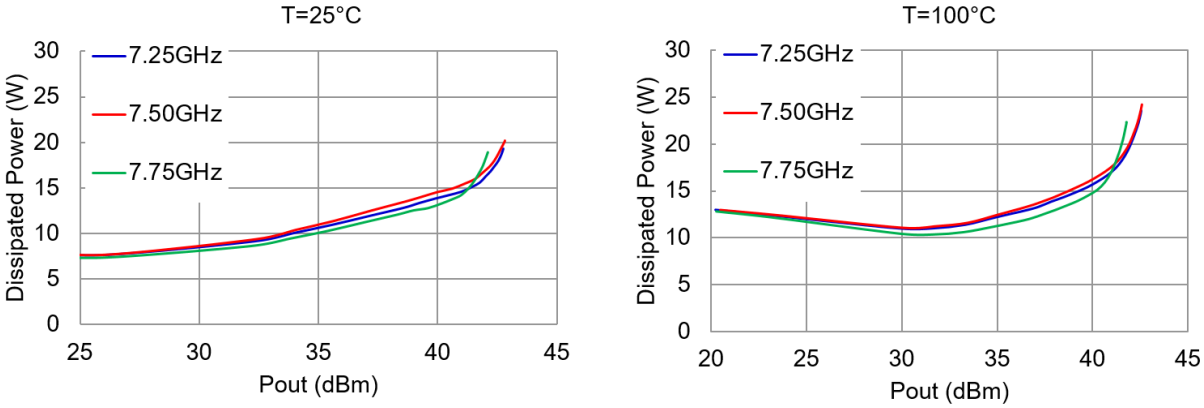
Drain Current vs. Output Power (Pout) vs. Frequency



DC Power vs. Output Power (Pout) vs. Frequency



Dissipated Power vs. Output Power (Pout) vs. Frequence



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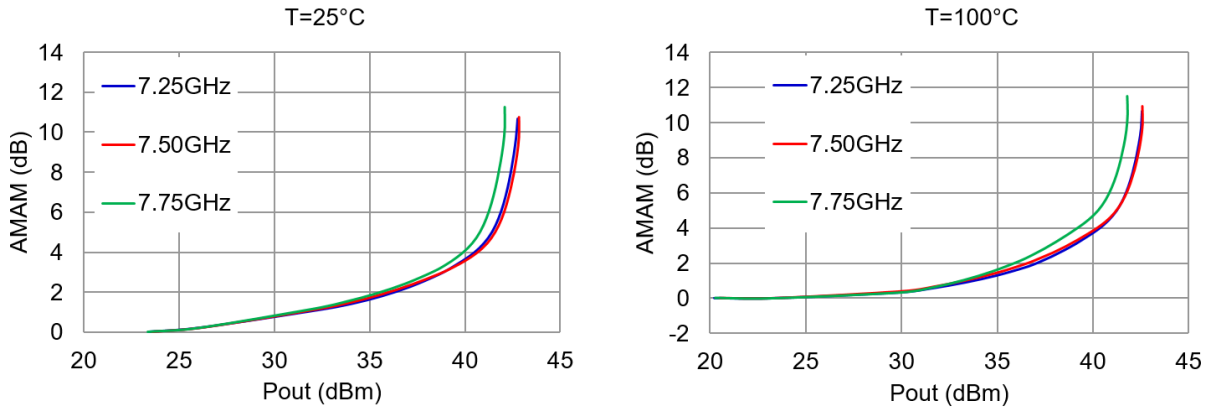
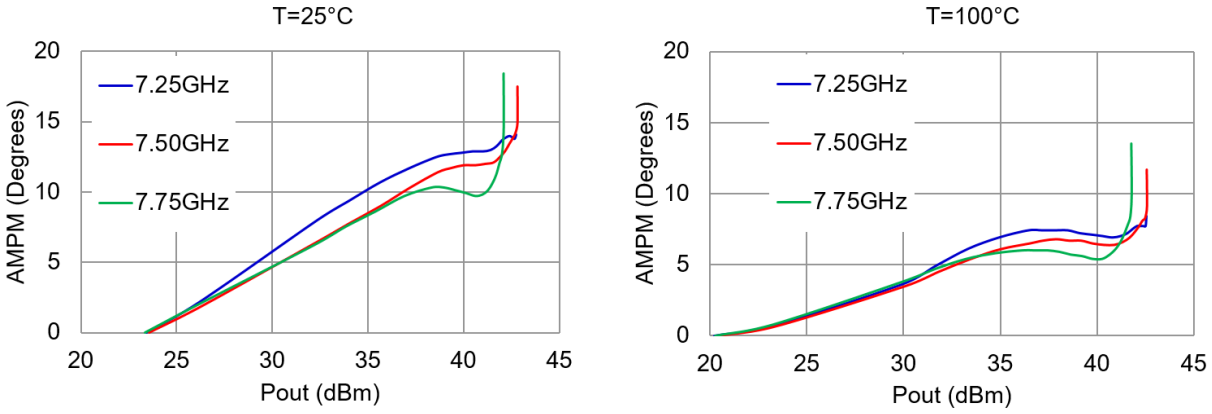
Typical Board Measurements: Large Signal Performance

Test conditions: CW, Idq = 330mA, $T_{backside}$ = +25°C / 100°C

AMAM vs. Output Power (Pout) vs. Frequency



AMPM vs. Output Power (Pout) vs. Frequency



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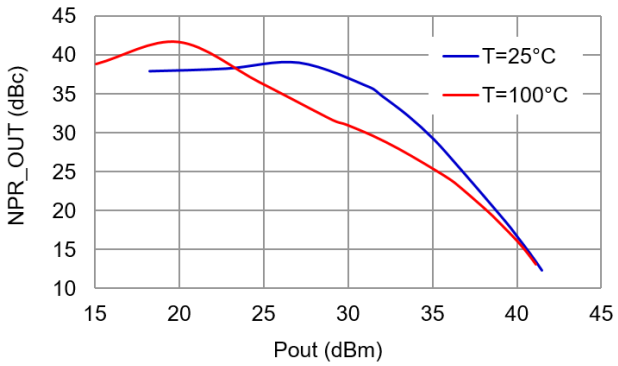
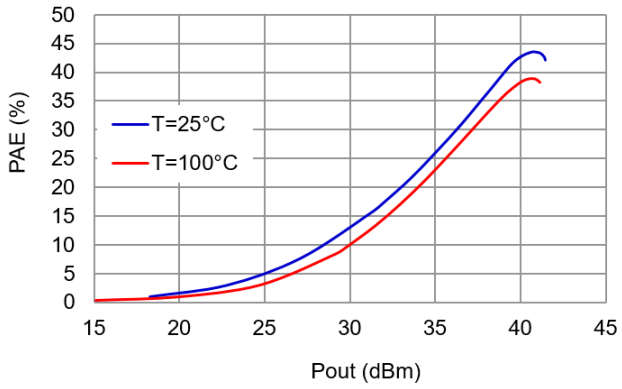
Typical Board Measurements: Linearity - Noise Power Ratio

Test conditions: Vd = 28V, Idq = 330mA, BW= 500MHz, Notch=10%, Number of tones: 4000, Frequency = 7.5GHz, $T_{backside}$ = +25°C / 100°C

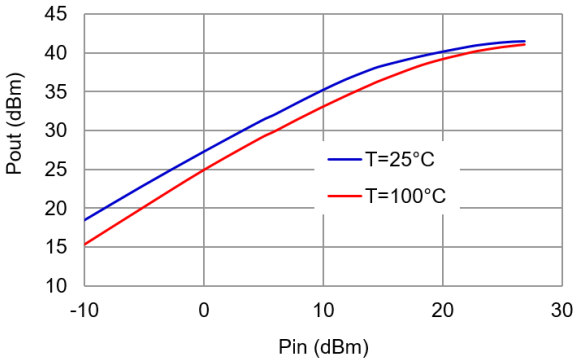
NPR vs. Output Power (Pout)

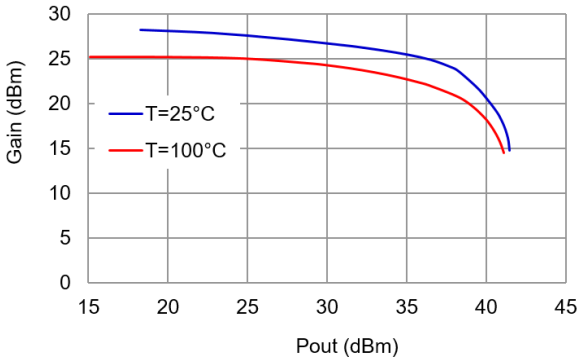


PAE vs. Output Power



Output power vs. Input power and Gain vs. Output Power (Pout)





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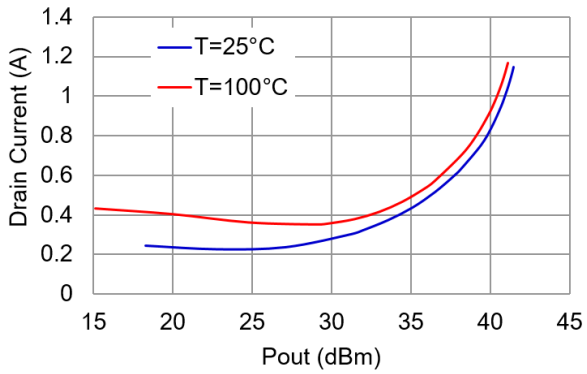
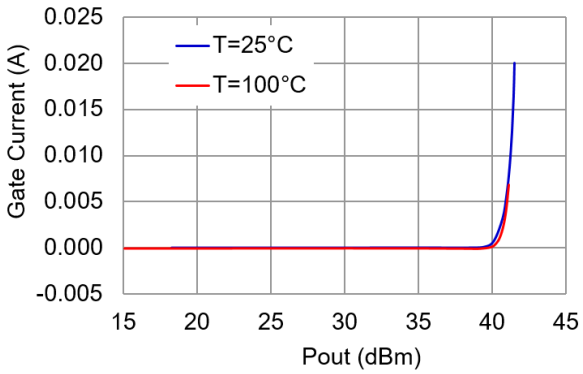
Typical Board Measurements: Linearity - Noise Power Ratio

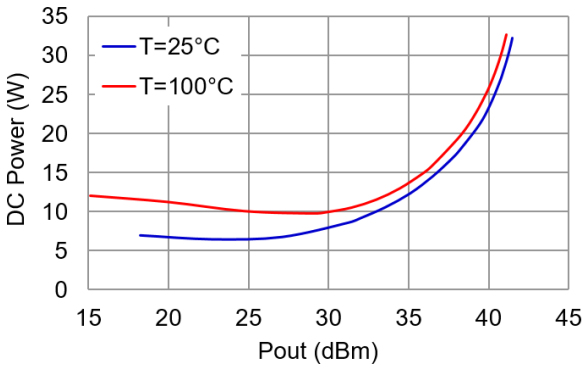
Test conditions: Vd = 28V, Idq = 330mA, BW= 500MHz, Notch=10%, Number of tones: 4000, Frequency = 7.5GHz, $T_{backside}$ = +25°C / 100°C

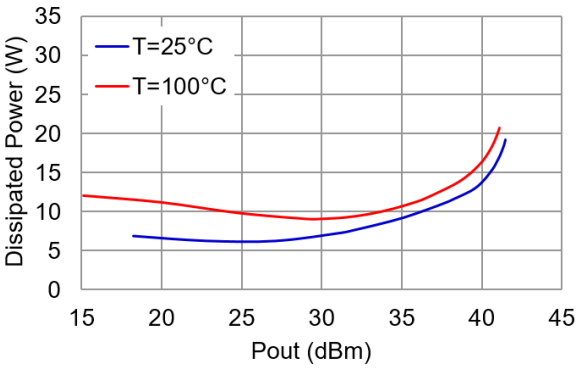
Drain and Gate currents vs. Output Power (Pout)





DC and Dissipated Power vs. Output Power





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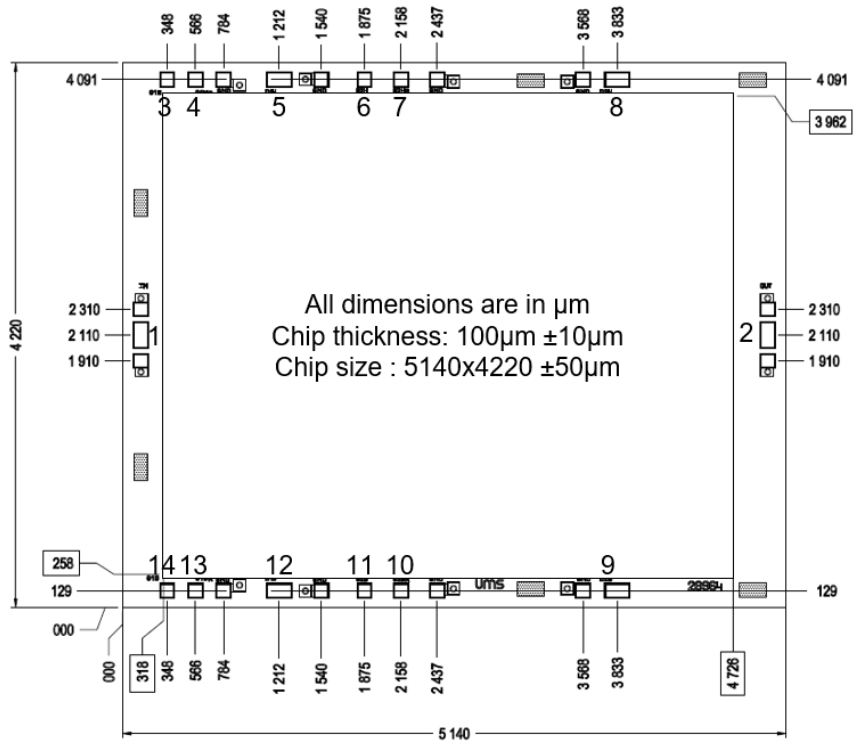
Mechanical Drawing



Pad	Name	Description	PAD Size
1	IN	RF input	116x206
2	OUT	RF output	116x206
3	G1H	DC Gate voltage, 1st Stage, North	108x108
4	G1HR	DC Gate voltage, 1st Stage, North with Rg 40Ω	108x108
5	D1H	DC Drain voltage, 1st Stage bias north	190x108
6	G2H	DC Gate voltage, 2nd Stage, North	108x108
7	G2HR	DC Gate voltage, 2nd Stage, North with Rg 10Ω	108x108
8	D2H	DC Drain voltage, 2nd Stage bias north	190x108
9	D2B	DC Drain voltage, 2nd Stage bias South	108x108
10	G2BR	DC Gate voltage, 2nd Stage, South with Rg 10Ω	108x108
11	G2B	DC Gate voltage, 2nd Stage, South	108x108
12	D1B	DC Drain voltage, 1st Stage bias South	190x108
13	G1BR	DC Gate voltage, 1st Stage, South with Rg 40Ω	108x108
14	G1B	DC Gate voltage, 1st Stage, South	108x108

Notes:
(1) VD1H, VD1B, VD2H, VD2B Pins must be connected to the DC drain supply voltage.
(2) Please only use one Pin of G1H and G1B to bias the first stage. Please only use one Pin of G2H and G2B to bias the second stage.
(3) G1HR, G2HR, G1BR, G2BR are not used.

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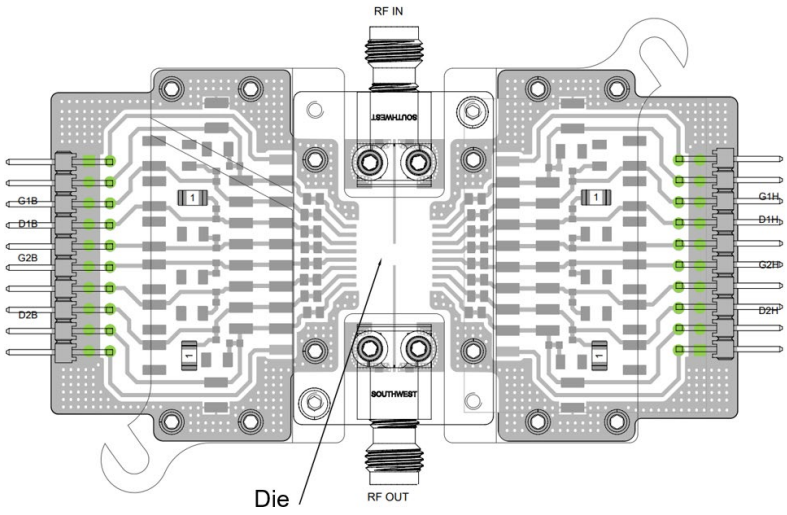
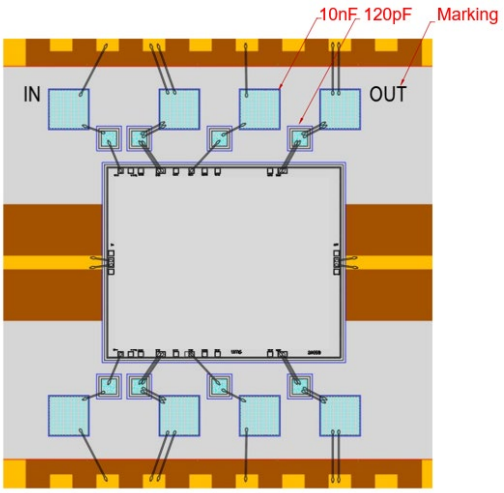
Recommended assembly plan





Three levels of decoupling capacitors have been used: Two on the tab and one on the board. The first level is composed of 120 pF chip capacitors. The second level is composed of 10nF chip capacitors. The third level is made with 68nF SMD 1206 capacitors (and 10 ohms added in series). The first two levels should be as close as possible to the die.

Recommended circuit bonding and decoupling table

Label	Bonding (25µm diameter)	External Capacitor
RFin//RFout	Two parallel bond wires on input and output RF accesses. That corresponds to a measured length of 489µm/bond and an equivalent inductor 0.34nH.	Not required
G1H,G1B,G2B,G2H	Inductance ≤ 1nH (mainly for first decoupling level)⇒1.2mm length	C1 ~ 120pF C2 ~ 10nF C3 ~ 68nF
D1H,D1B,D2B,D2H	Inductance ≤ 1nH (mainly for first decoupling level)⇒1.2mm length	C1 ~ 120pF C2 ~ 10nF C3 ~ 68nF

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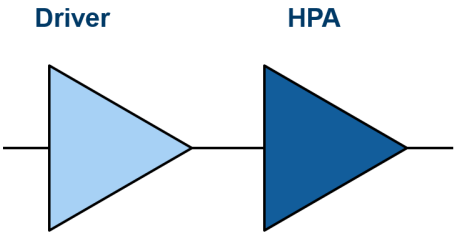
Recommended UMS Power chain

The CHA8154-99F is recommended with the CHA6154-99F as driver.
Total Gain: > 65 dB
For more information about the CHA6154, see our web site www.ums-rf.com



CHA6154-99F	CHA8154-99F
7.25GHz – 7.75GHz	7.25GHz – 7.75GHz
28 V	28 V
70 mA	330 mA

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Recommended reflow process assembly

Refer to the application note AN0001 available at https://www.ums-rf.com for die attach.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at https://www.ums-rf.com.

Recommended ESD management

Refer to the application note AN0020 available at https://www.ums-rf.com for ESD sensitivity and handling recommendations for the UMS package products.

Recommended Evaluation board assembly

Refer to the application note AN0030 available at https://www.ums-rf.com Evaluation board.

Ordering Information

Chip form	CHA8154-99F/00

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