11 – 18GHz Low Noise Amplifier

GaAs Monolithic Microwave IC in SMD leadless package

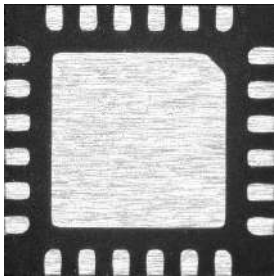
Description

The CHA1252-QDG is a three-stage Low Noise Amplifier operating in the 11 – 18GHz frequency band. This LNA typically presents low Noise Figure of 1.3dB associated to a small signal gain of 26dB.

It can provide up to 7dBm output power at 1dB gain compression and needs DC power supply of 2V/30mA. It is available in 4x4 plastic package.

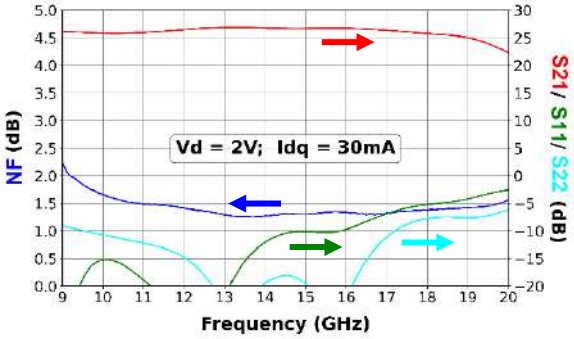
Designed for space applications, it is also ideal for a wide range of microwave systems.

This product is developed using a GaAs pHEMT process and is provided on low cost SMD RoHS compliant QFN plastic package.



Main Features

- Frequency range : 11 – 18 GHz
- Linear Gain : 26dB
- NF : 1.3dB
- OP1dB : 7dBm
- OIP3 : 18dBm
- DC bias: Vd = 2V @Idq = 30mA
- 24 Leads – QFN 4x4mm^2
- MSL1



Main Electrical Characteristics

Test conditions : T_{case} = 25°C, Vd = 2V, Idq = 30mA

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	11		18	GHz
Gain	Small signal Gain		26		dB
NF	Noise Figure		1.3		dB
P1dB	Output Power @1dB compression		7		dBm

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Specifications

Test conditions : T_{case} = 25°C, Vd = 2V, Idq = 30mA

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	11		18	GHz
Gain	Small signal Gain		26		dB
NF	Noise Figure		1.3		dB
S11	Input Return loss		10		dB
S22	Output return loss		10		dB
OP1dB	Output Power at 1dB gain compression		7		dBm
OIP3	Output Third order Intercept Point		18		dBm
Idq	Quiescent Drain Current		30		mA

These values are representative of on board measurements as defined on the drawing in paragraph "Evaluation mother board".

Absolute Maximum Ratings (1)

T_{case} = 25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	4	V
Idq	Quiescent Drain current	85	mA
Vg	Gate bias voltage	-1.5 to 0.3	V
Pin	Maximum peak input power overdrive	-8	dBm

(1) Operation of this device above anyone of these parameters may cause permanent damage.

Recommended Operating Range (2), (3)

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	1.5 – 3	V
Idq	Quiescent Drain current	30 – 60	mA
Pin	Maximum peak input power overdrive (2)	-10	dBm
$T_{junction\_max}$	Maximum Junction temperature	175	°C
T_{case}	Operating temperature range	-40 to 85	°C
T_{stg}	Storage temperature range	-55 to 150	°C

(2) Electrical performances are defined for specified test conditions

(3) Electrical performances are not guaranteed over all recommended operating conditions

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Typical Bias Conditions

Symbol	Pad Nº	Parameter	Values	Unit
Vd	10	Drain bias voltage	2	V
Vg	21	Gate bias voltage	Set Vg for recommended Idq	V

“Power ON” sequence

1. Ground the device
2. Set the Gate voltage to -1.5V
3. Apply the Drain voltage Vd (Typically 2V)
4. Increase Vg up to quiescent bias drain current Idq
5. Apply RF signal

“Power OFF” sequence

1. Turn off RF signal
2. Decrease the Gate voltage to -1.5V
3. Decrease the Drain voltage to 0V
4. Turn off Vd supply
5. Turn off Vg supply

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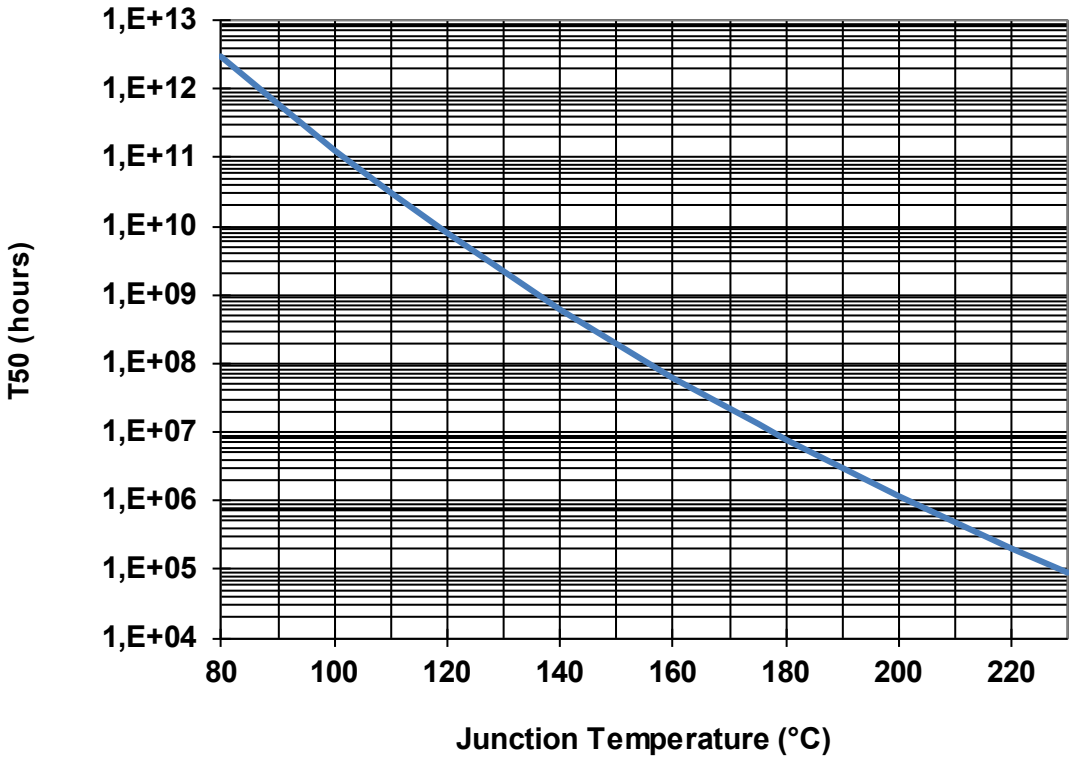
Device Thermal Performances

All the figures given in this section are obtained assuming that the die is only cooled down by conduction through the package case.
The temperature is monitored at the QFN backside interface (T_{case}).
For nominal operation, the system's maximum temperature must be adjusted to ensure that the junction temperature ($T_{junction}$) remains below the maximum value specified in the Recommended Operating Ratings table.
The system PCB must be designed to comply with this requirement.

Parameter	Biasing conditions	$T_{junction}$ (°C)	R_{TH} (°C/W)	T_{50} (2) (hours)
R_{TH} (1) Thermal Resistance (Junction to Case)	Vd= 2V Id= 30mA Pdiss= 60mW	107	363	1.6E+10
	Vd= 2V Id= 60mA Pdiss= 120mW	129	363	1.2E+09

(1) Assuming 85°C T_{case}.
(2) The time at which 50% of the products are expected to have failed or reached the end of their useful life.



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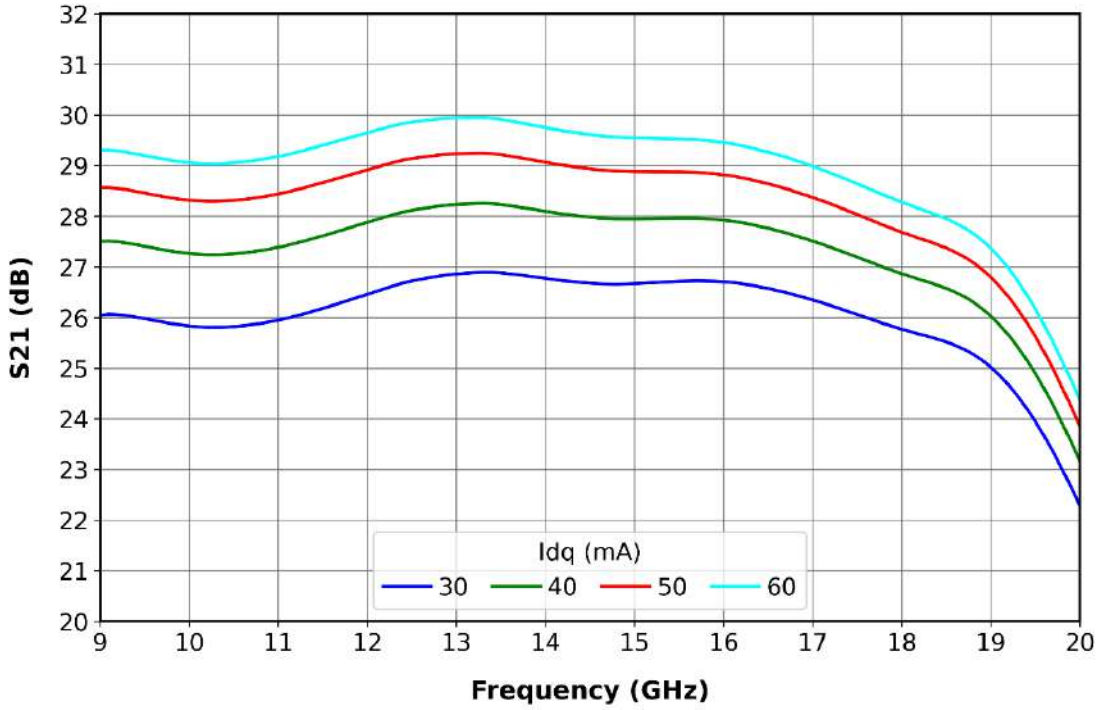
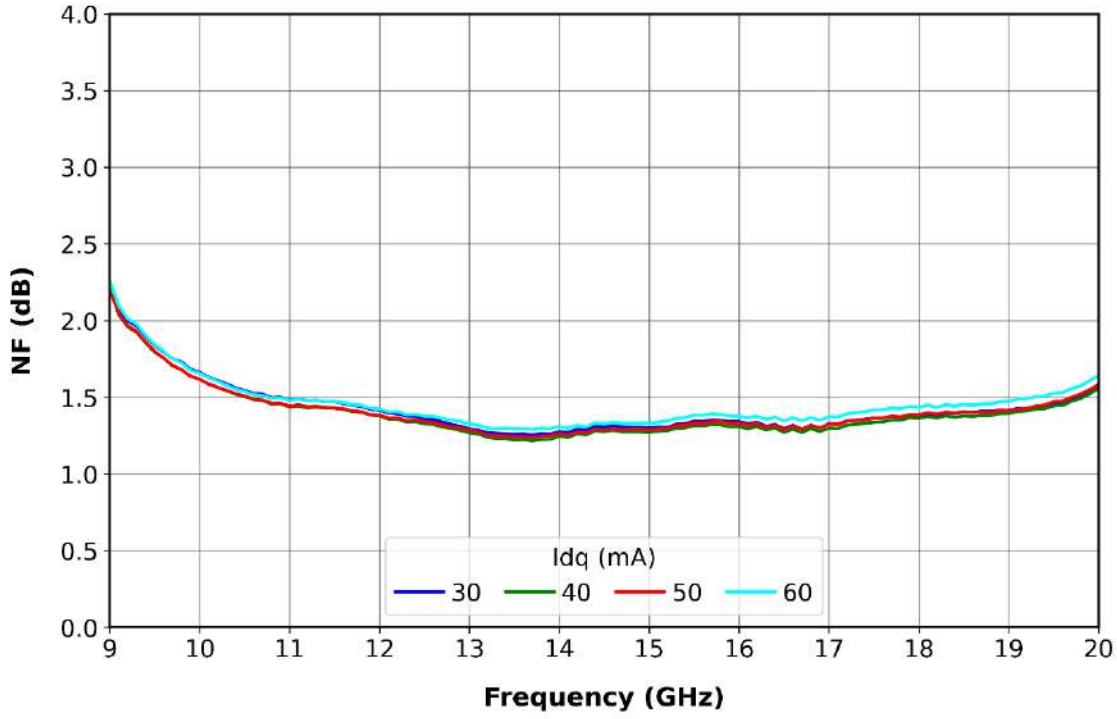
Typical Board Measurements

Board losses are de-embedded. Measurements are given in the package reference planes.
Test conditions : CW, T_{case} = 25°C, Vd = 2V

Small signal Gain vs. Freq and Idq



Noise Figure vs. Freq and Idq



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Typical Board Measurements

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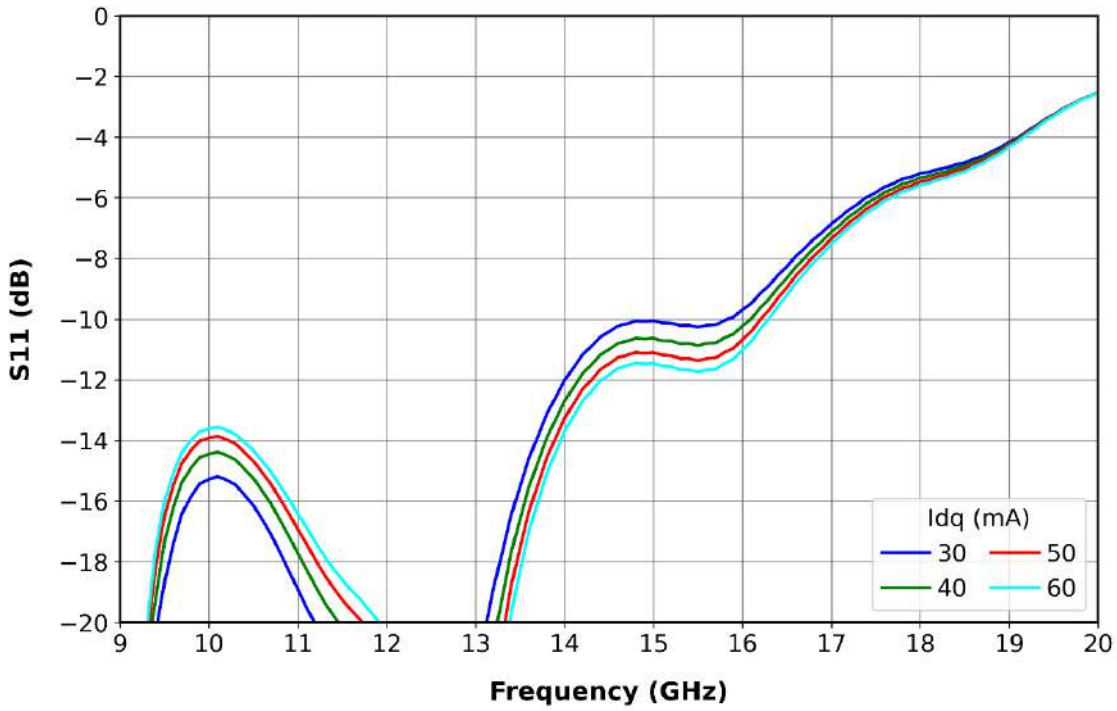
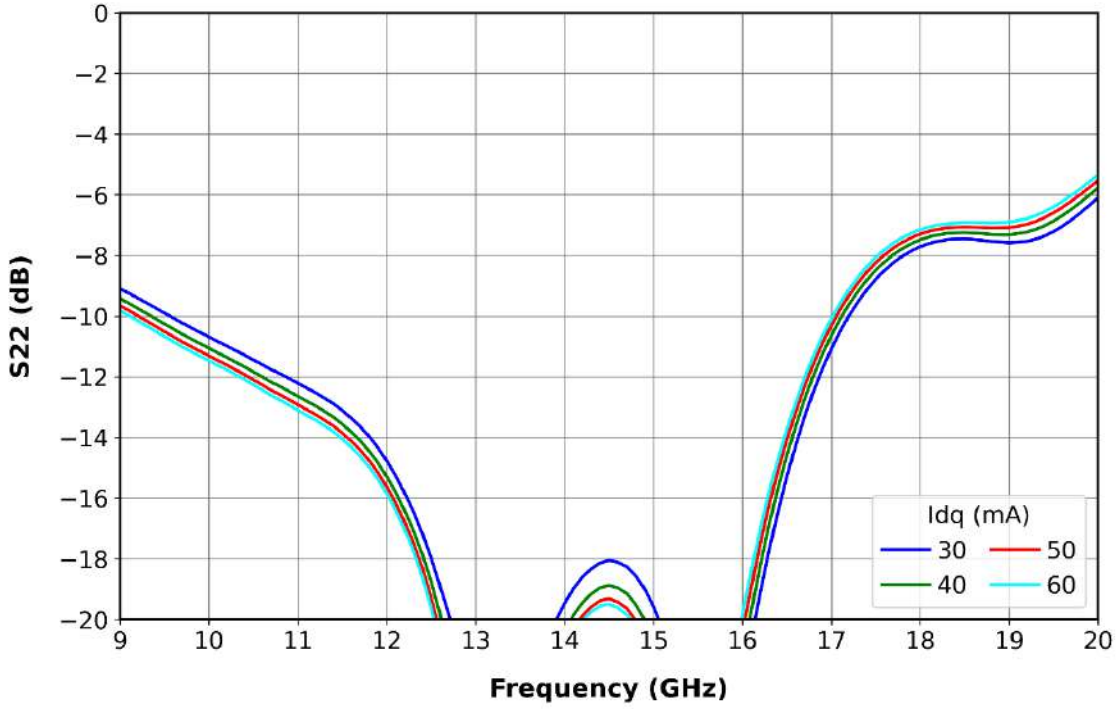
Test conditions : CW, T_{case} = 25°C, Vd = 2V

Input Return loss vs. Freq and Idq



Output Return loss vs. Freq and Idq



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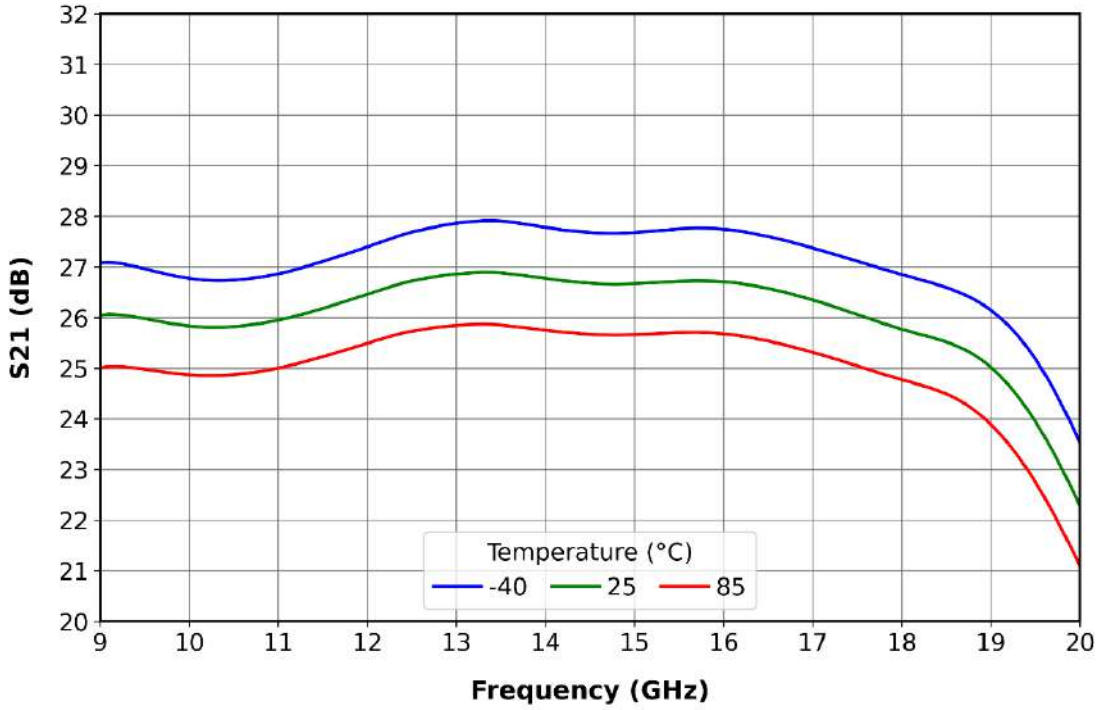
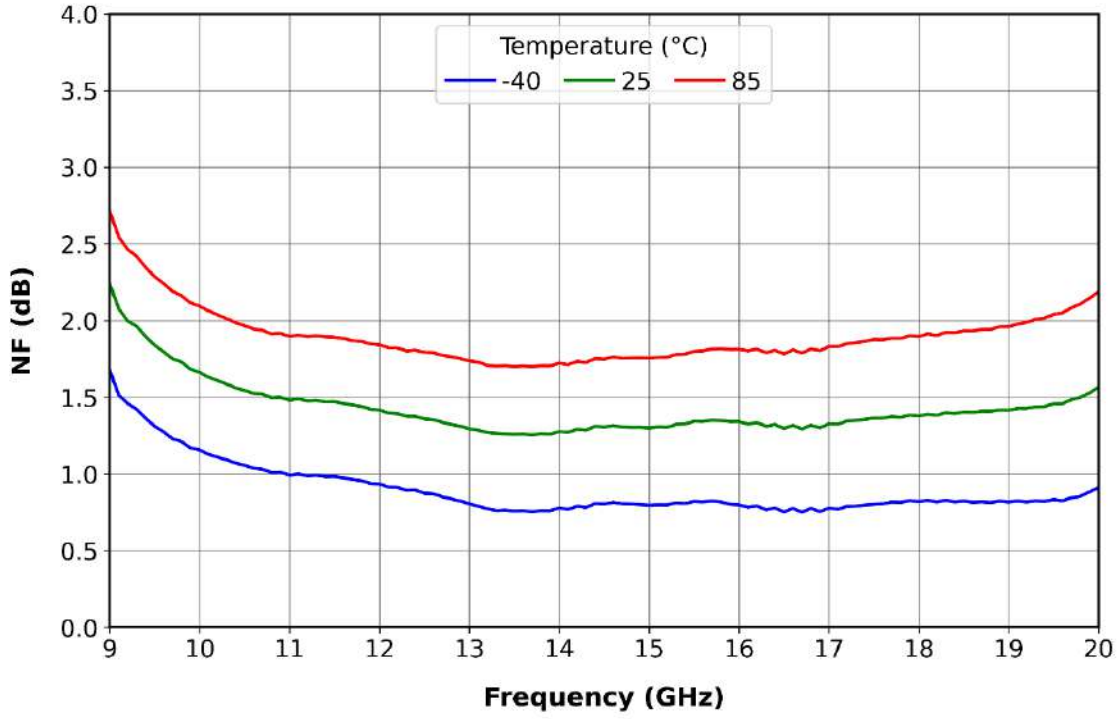
Typical Board Measurements

Board losses are de-embedded. Measurements are given in the package reference planes.
Test conditions : CW, Vd = 2V, Idq = 30mA

Small signal Gain vs. Freq and Temperature



Noise Figure vs. Freq and Temperature



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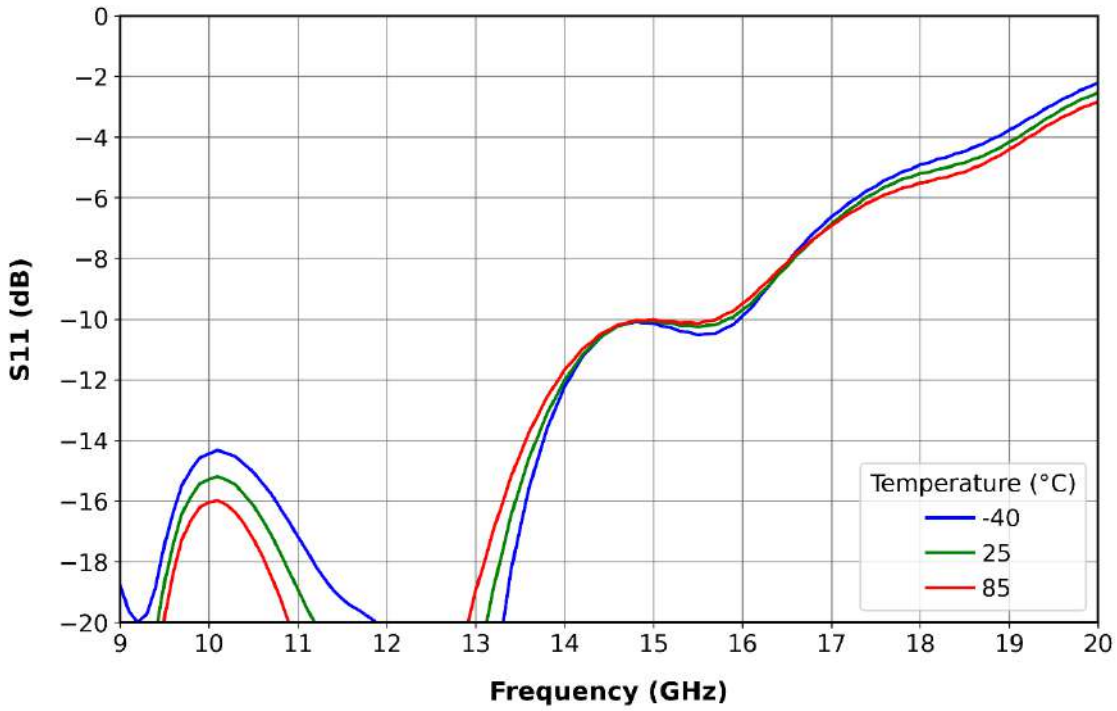
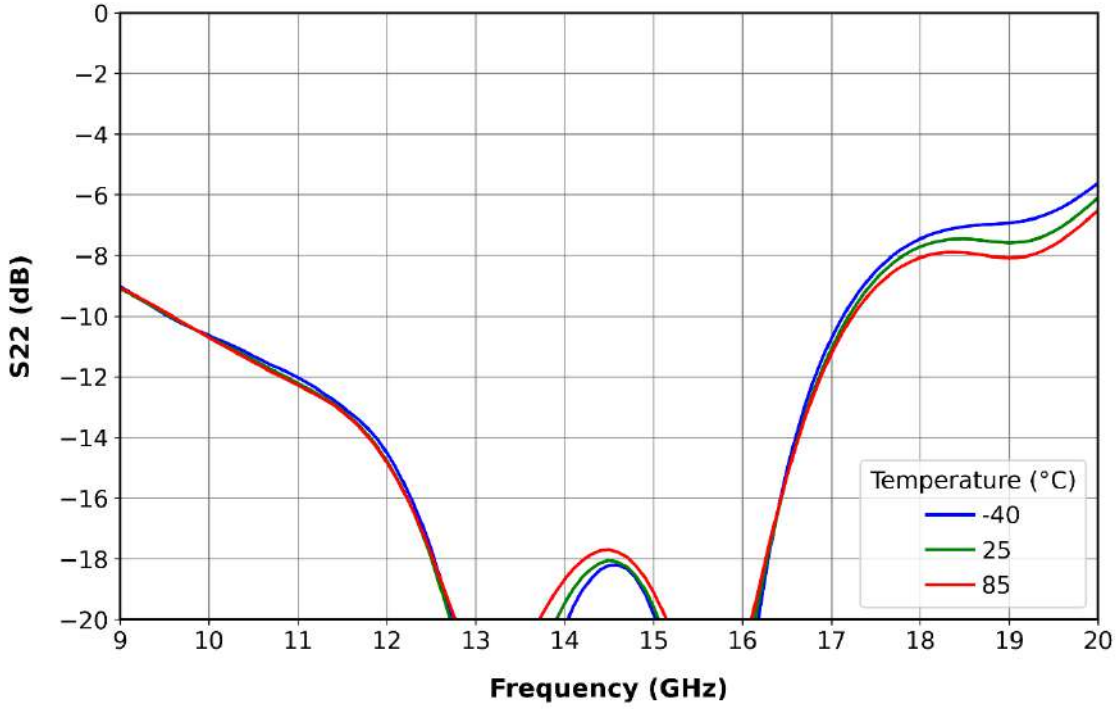
Typical Board Measurements

Board losses are de-embedded. Measurements are given in the package reference planes.
Test conditions : CW, Vd = 2V, Idq = 30mA

Input Return loss vs. Freq and Temperature



Output Return loss vs. Freq and Temperature



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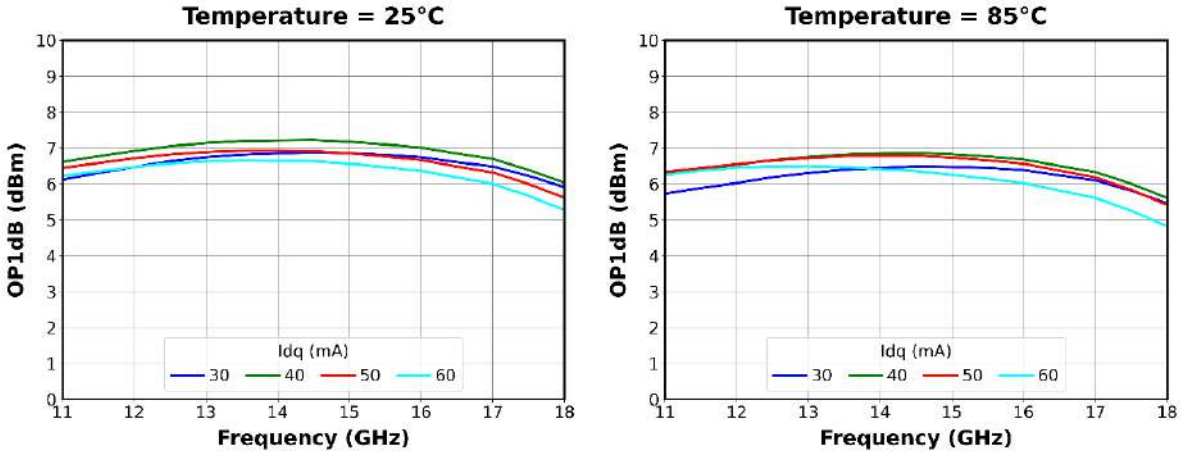
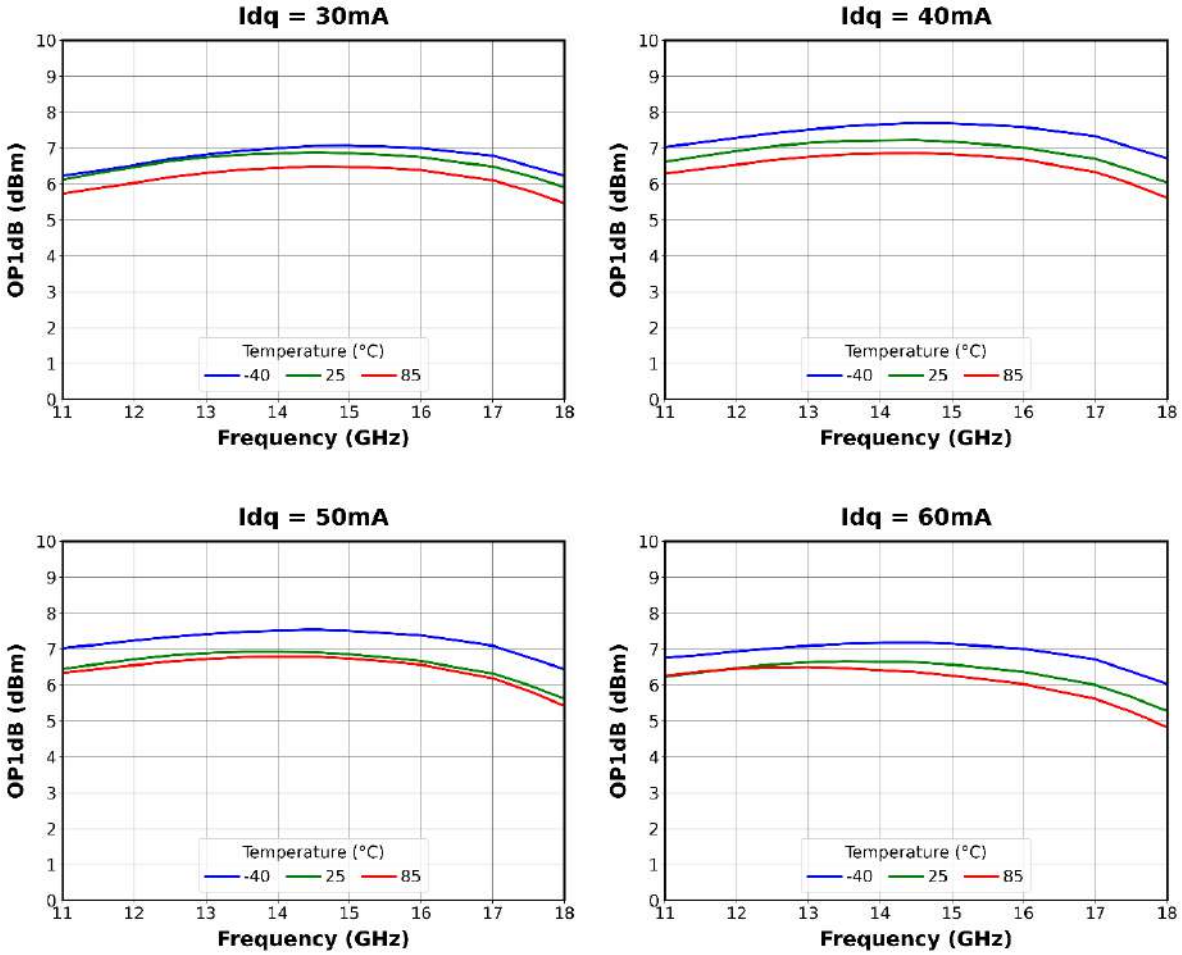
Typical Board Measurements

Board losses are de-embedded. Measurements are given in the package reference planes.
Test conditions : CW, Vd = 2V

OP1dB vs Freq and Idq for different Temperature



OP1dB vs Freq and Temperature for different Idq



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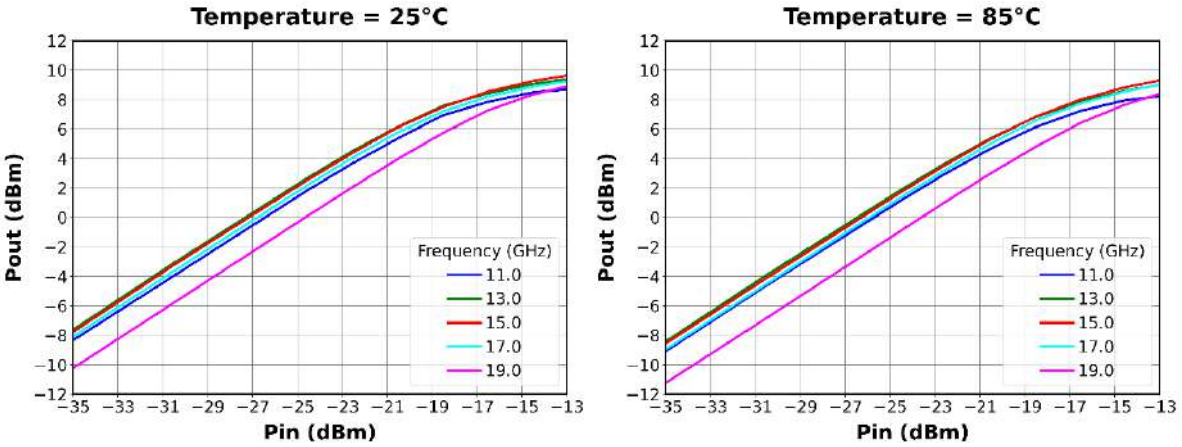
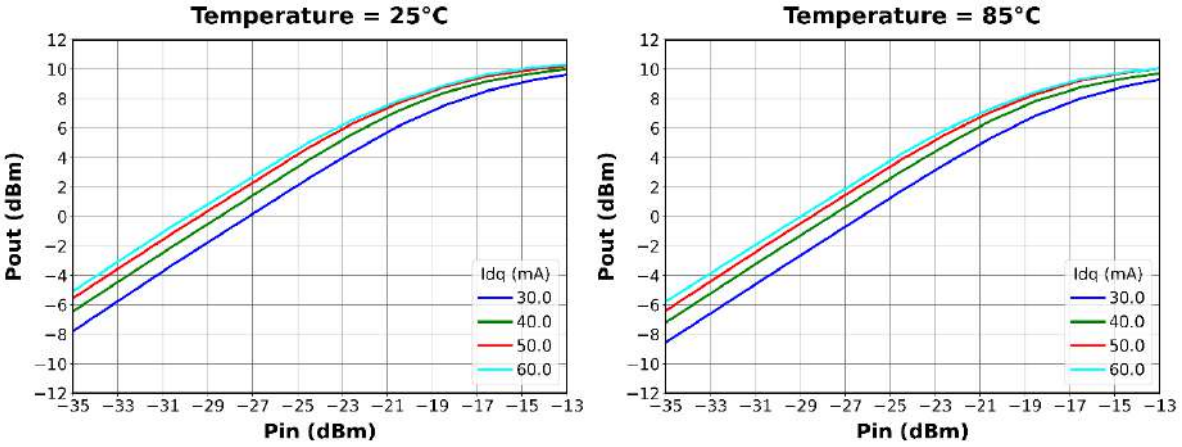
Typical Board Measurements

Board losses are de-embedded. Measurements are given in the package reference planes.
Test conditions : CW, Vd = 2V

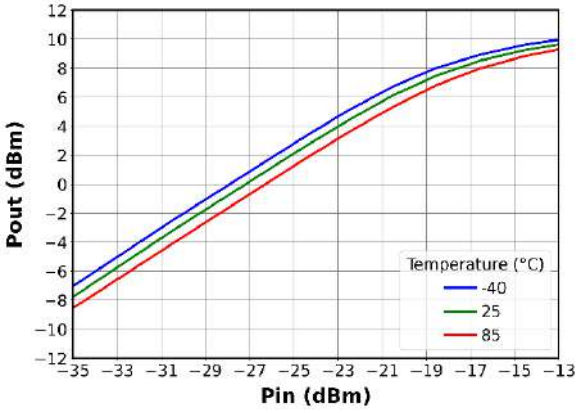
Pout vs Pin and Freq for different Temperature @Idq = 30mA



Pout vs Pin and Idq for different Temperature @ Freq = 15GHz



Pout vs Pin and Temperature @Idq = 30mA & @ Freq = 15GHz



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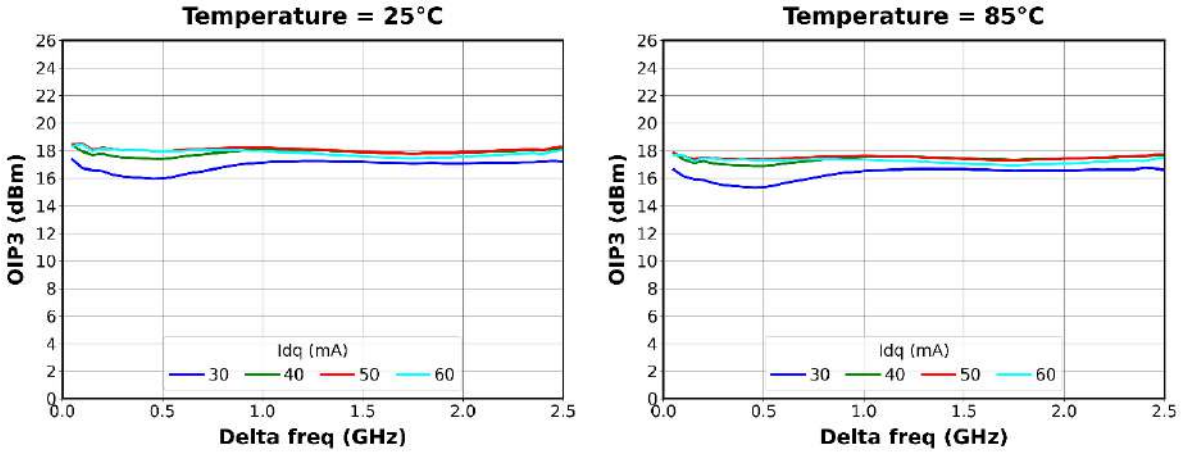
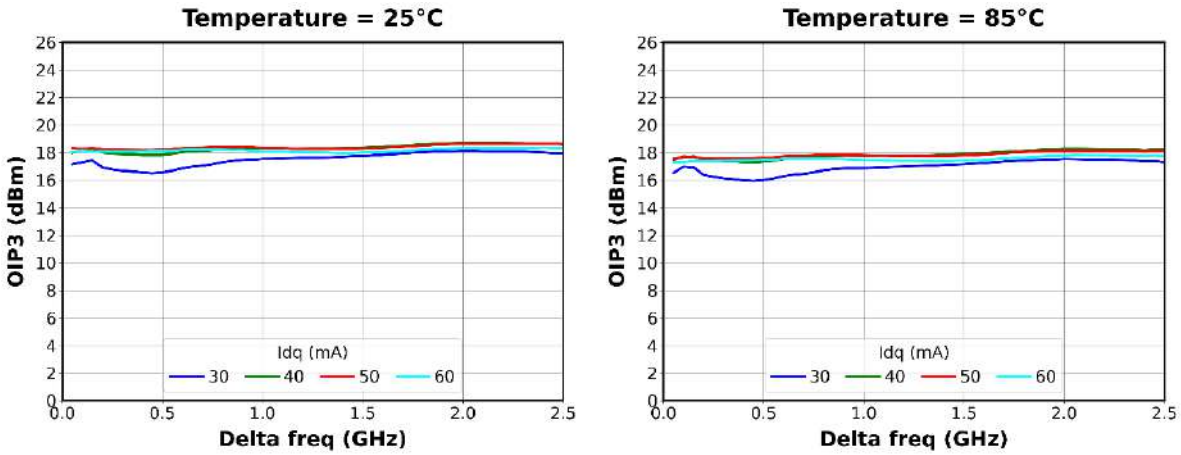
Typical Board Measurements

Board losses are de-embedded. Measurements are given in the package reference planes.
Test conditions : CW, Vd = 2V, Pin (per tone) = -35dBm

OIP3 vs Delta Freq and Idq @Freq = 13.25GHz



OIP3 vs Delta Freq and Idq @Freq = 15.75GHz



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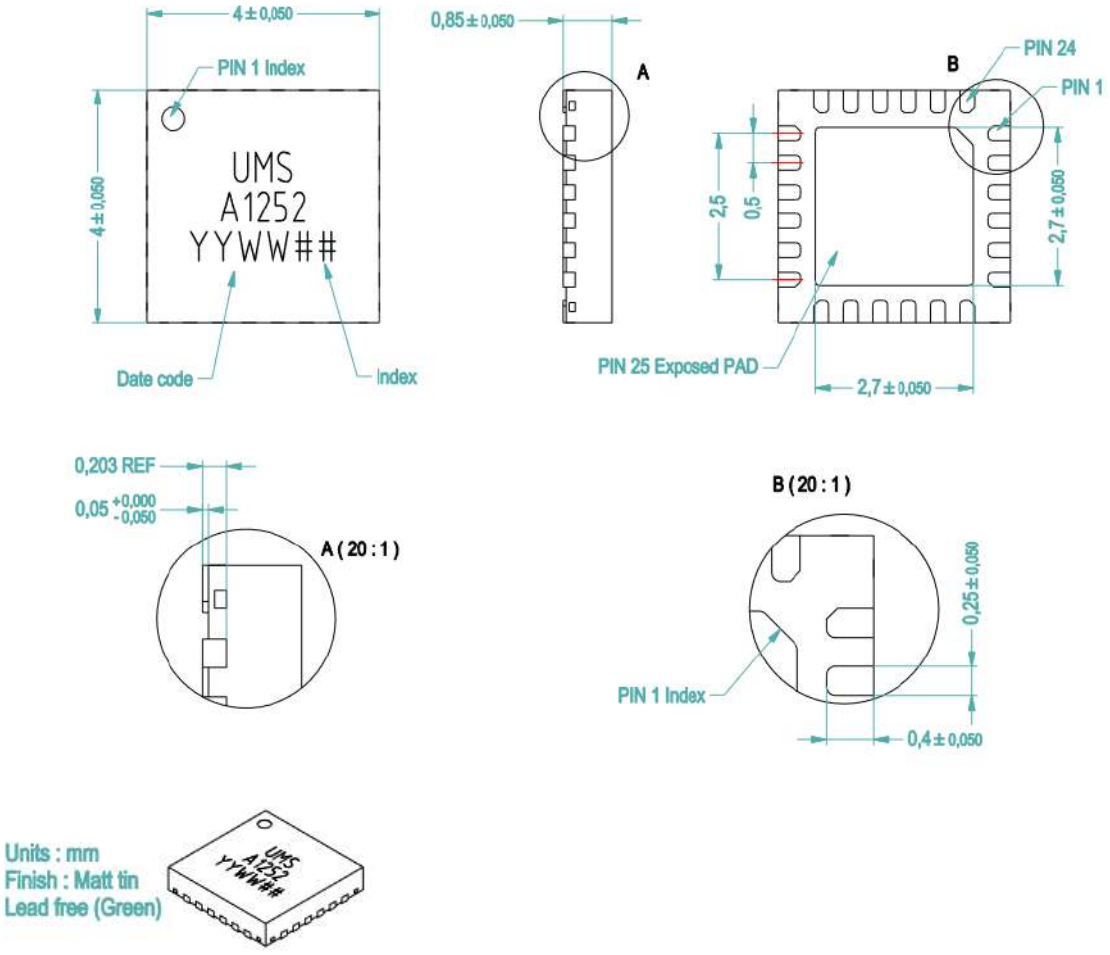
Package outline (1)



Units :	mm	1- NC	11- NC	21- VG
Finish :	Matt tin	2- NC	12- NC	22- GND(2)
MSL Rating :	MSL1	3- GND(2)	13- NC	23- NC
Lead Free (Green)		4- RFin	14- GND(2)	24- NC
From the standard :	JEDEC MO-220	5- GND(2)	15- RFout	25- GND(2)
NC :	VGGD Not Connected	6- NC	16- GND(2)	
		7- NC	17- NC	
		8- NC	18- NC	
		9- GND(2)	19- NC	
		10- VD	20- NC	

(1) Refer to the application note AN0017 (https://www.ums-rf.com) for general consideration and recommendations for Molded Plastic QFN/DFN packages.

(2) It is strongly recommended to ground all pins marked “GND” through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

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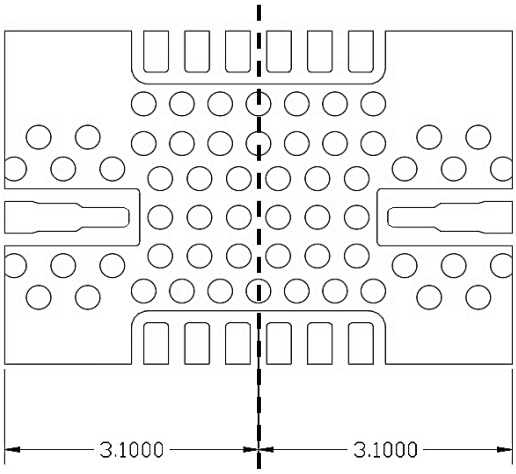
Definition of measurements reference planes

The reference planes used measurements given above are symmetrical from the symmetrical axis of the package (see drawing beside). The input and output reference planes are located at 3.1mm offset (input wise and output wise respectively) from this axis.



Package Information

Parameter	Value
Package body material	RoHS-compliant
	Low stress Injection Molded Plastic
Lead finish	Matt tin
MSL Rating	MSL1

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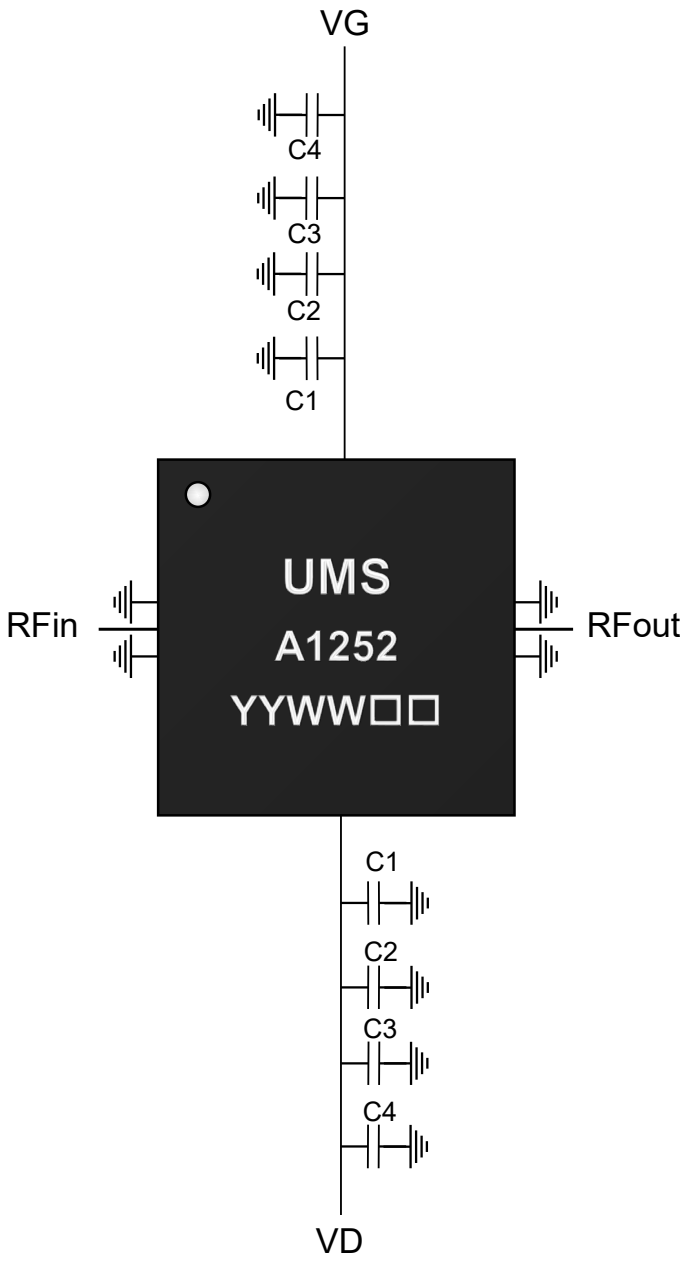
Recommended Assembly Plan



Bill of Materials

Label	Value	Description
C1	RF	Capacitor 120pF ±15% 20V
C2	RF	Capacitor 10nF ±10% 20V
C3	RF	Capacitor 1µF ±10% 20V
C4	RF	Capacitor 10µF ±10% 20V

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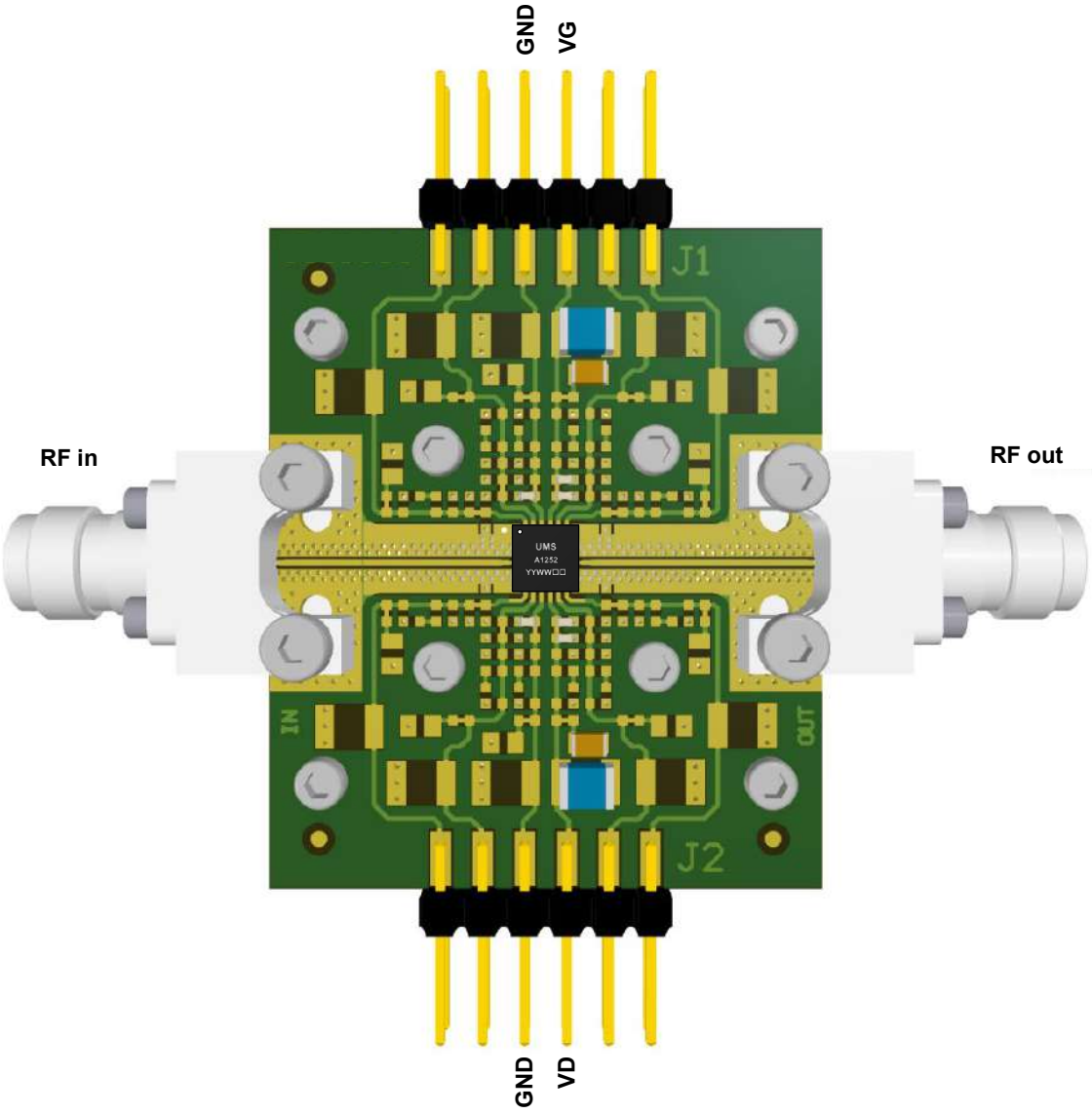
Evaluation Board

- Compatible with the proposed footprint.
- Based on typically Ro4350 / 8mils or equivalent.
- Using a micro-strip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 120pF, 10nF, 1µF, 10µF ±10% are recommended for all DC accesses.



Notes:
All board measurements are performed using shielded cables, even for DC bias, to ensure safe operation.

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Recommended package footprint

Refer to the application note AN0017 available at https://www.ums-rf.com for package foot print recommendations.

SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017 available at https://www.ums-rf.com.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at https://www.ums-rf.com.

Recommended ESD management

Refer to the application note AN0020 available at https://www.ums-rf.com for ESD sensitivity and handling recommendations for the UMS package products.

Description of Evaluation Board

Refer to the application note AN0031 available at https://www.ums-rf.com for the description of Evaluation Board for Packaged Die and recommendations for this UMS package product.

Ordering Information

Evaluation Board:	EDG-CHA1252-QDG	
QFN 4x4 package:	CHA1252-QDG/XY	
	Stick: XY = 20	Tape & reel: XY = 21

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