Shared Foundry Offer 2024

United Monolithic Semiconductors

Take advantage of very high frequency and Cost effective UMS BES Schottky diode process

United Monolithic Semiconductors is opening **a shared foundry run on BES Schottky diode process**.
The launch date for the Multi-Project Wafer is **April 19, 2024.**

BES diode process extremely high cut off frequency allows very diverse circuit design from high frequency RF power detector to passive balanced mixers for radar signal analysis, for power level control loop to astronomy signal detection beyond 300GHz.

Optimized for low conversion loss, high frequency and high volume high yield MMIC production, **BES** is widely recommended for the design of mixers, passive receivers and power detector for applications such as Telecommunication Radio or Automotive Collision Avoidance radars and Space Communication systems.

BES is successfully evaluated for Space use and referenced in the European Preferred Part List by the European Space Agency – see:https://escies.org/epplmanufacturer/show?id=124%20

Designers are invited to share a **BES** run at an affordable entry price of 2 000€/mm².

What are the main characteristics of BES?

Element	Parameter	Typical value	Conditions
Diode (1 x 5µm)	Ideality Factor n	1.2	Vdiode = 0.55V
	Jo (A/cm2)	3e-6	
	Rs (Ω)	5	Idiode = 15 mA
	Vbd (V)	-6.5	Idiode = -20 µA
	Von (V)	0.65	Idiode = -20 µA
	Ft (cut off freq.) (GHz)	3000	
MIM Cap.	Density (pF/mm²)	330	@ 1 MHz
MIM Cap. - High Density	Density (pF/mm²)	625	@ 1 MHz
TaN Resistor	Sheet Resistance (Ω/□)	30	
TiWSi Resistor	Sheet Resistance (Ω/□)	1000	
GaAs Resistor	Sheet Resistance (Ω/□)	9	
Wafer thickness	µm	100	

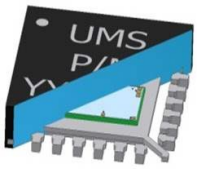
Examples of microwave performance achieved by UMS catalogue MMICs designed on BES process:

Part Number	Freq (GHz)	Gain (dB)	Dynamic (dB)	Case
Detector				
CHE1270-QAG	5-44	-	30	QFN
CHE1260-QAG	12-27	-1	30	QFN

Part Number	Freq (GHz)	Gain (dB)	P-1dB (dBm)	Case
Mixer				
CHM2378a99F	76-77	-7.5	0	Die
CHM1270a98F	76-77	-7.5	3.5/0	Die

mktsales@ums-rf.com
+33 (0) 1 69 86 3200

By choosing standard MMIC dimensions which are compatible with QFN high volume packaging capability, your project is on track for future industrial success.



How to participate to this shared foundry run?

So to start designing, please apply on-line for process Design Kit. Before the deadline, please send your layout to: foundry@ums-rf.com

INFORMATION	**Lowest cost guaranteed** Simply provide your layout **before April 19, 2024**

DELIVERY	20 chips
CONDITIONING	Gel-Pak®

AVAILABLE DIE SIZE (mm)	1	1,4	2,4	3,4	4
MAX RATIO	1:3				

Die size include 70µm dicing street - Launching date flexibility is +/- 2 weeks
Dieframes for layout can be provided on request
Minimum order is 4mm² - Price is valid until April 19, 2024
Order to be placed before April 5, 2024
Important Notes:

- UMS may cancel the run in case of insufficient number of participants.
- For some countries a specific dedicated export license may be required before delivery.

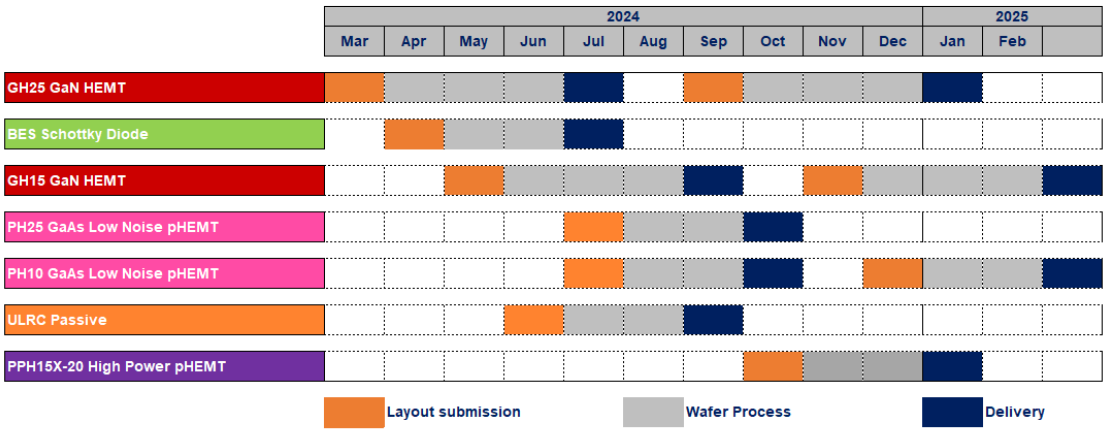
	1	1.4	2.4	3.4	4
1	1	1.4	2.4		
1.4	1.4	2	3.4	4.8	5.6
2.4	2.4	3.4	5.8	8.2	9.6
3.4		4.8	8.2	11.6	13.6
4		5.6	9.6	13.6	16

BES available die size (mm) including 70µm dicing street

How many dies will I receive and how much does it cost?

You will receive 20 dies of your circuit in Gel-Pak® box from a **BES** PCM good wafer. The price is based on your circuit dimensions on the mask tile multiplied by the mm² unit price. For example, if your circuit is 1.4 x 3.4 mm², the price is 1.4 x 3.4 x 2 000€ = 9 520€.

Which processes are regularly offered in shared foundry?



mktsales@ums-rf.com
+33 (0) 1 69 86 3200