United Monolithic Semiconductors

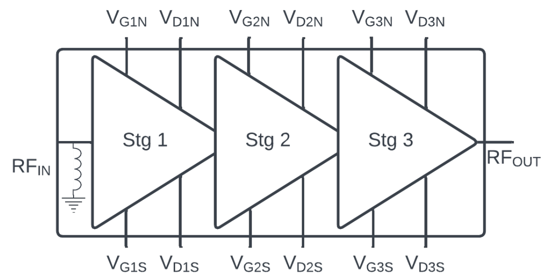
CHA8362-99F

27.5-31GHz 25W High Power Amplifier

GaN Monolithic Microwave IC in Bare Die Form

Description

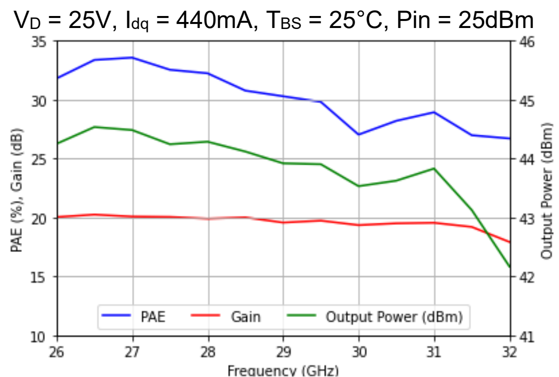
The CHA8362-99F is a three stages High Power Amplifier operating between 26.5 and 31GHz and providing typically 25W of saturated output power associated to 30% of power added efficiency. The typical power supply is 25V/440mA (quiescent current). The amplifier exhibits more than 25dB small signal gain. It is firstly dedicated to satcom applications and well suited for a wide range of microwave applications and systems. The circuit is manufactured on a robust GaN-on-SiC HEMT process and is available in bare die form. The input and output are matched to 50Ω and the input integrates an ESD RF protection.



Main Features

- Frequency range: 26.5 – 31 GHz
- High output power: 25 W
- High PAE: 30 %
- Linear Gain: 25dB
- DC bias: VD = 25V & Idq = 440 mA
- Chip size: 3.6x3.6 mm²
- Available in bare die form

V_D = 25V, I_{dq} = 440mA, T_{BS} = 25°C, Pin = 25dBm



Main Electrical Characteristics

T_{BS} = 25°C

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	26.5		31	GHz
Gain	Linear Gain		25		dB
Psat	Saturated Output Power		44		dBm
PAE	Power Added Efficiency		30	36	dB

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Specifications

Tcase = +25°C, Vd = +25V, CW excitation

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	26.5		31	GHz
Gain	Linear Gain		25		dB
Pout	Saturated Output Power		44		dBm
PAE	Power Added Efficiency		30		%
Id	Drain current at saturation		3.5		A
S11	Input Return Loss		-9		dB
S22	Output return loss		-12		dB
Idq	Quiescent current		440		mA
Vd	Drain Voltage		25		V

These values are representative of on-board measurements as defined on the drawing in paragraph "Evaluation mother board".

Absolute Maximum Ratings (1)

Tcase = +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	27	V
Id	Quiescent Drain bias current	1000	mA
Vg	Gate bias voltage	-7 to -1	V
Pin	Maximum Input Power	30	dBm

(1) Operation of this device above anyone of these parameters may cause permanent damage

Recommended Operating Range (2), (3)

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	18 to 25	V
Id	Drain bias current	300 to 700	mA
Vg	Gate bias voltage	-3.5 to -2.5	V
Pin	Maximum Input Power	25	dBm
Tj	Maximum Junction temperature(4)	200	°C

(2) Electrical performances are defined for specified test conditions

(3) Electrical performances are not guaranteed over all recommended operating conditions

(4) See Device thermal performances section.

Temperature Range

Tcase	Operating temperature range	-40 to +95	°C
Tstg	Storage temperature range	-55 to +150	°C

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Typical Bias Conditions

T_{case} = 25°C

Symbol	Pad N°	Parameter	Values	Unit
V_G	4,8 11, 23, 28, 30	Gate voltage tuned for I_{dq} = 440mA	-3	V
V_D	6,10,14, 20, 24,28	Drain voltage	25	V

"Power ON" sequence

1. Bias HPA gate voltage at Vg close to Vpinch-off (Typically: $V_G \approx$ -5)
2. Apply V_D bias voltage (Typically: V_D = 25V)
3. Increase gate voltage V_g up to quiescent bias drain current I_{dq}
4. Apply RF signal

"Power OFF" sequence

1. Turn off RF signal
2. Bias HPA gate voltage at Vg close to Vpinch-off (Typically: $V_G \approx$ -5V)
3. Check that quiescent bias drain current I_{dq} is close to 0mA
4. Turn V_D bias voltage to 0V
5. Check that quiescent bias drain current I_{dq} is close to 0mA
6. Turn V_G bias voltage to 0V

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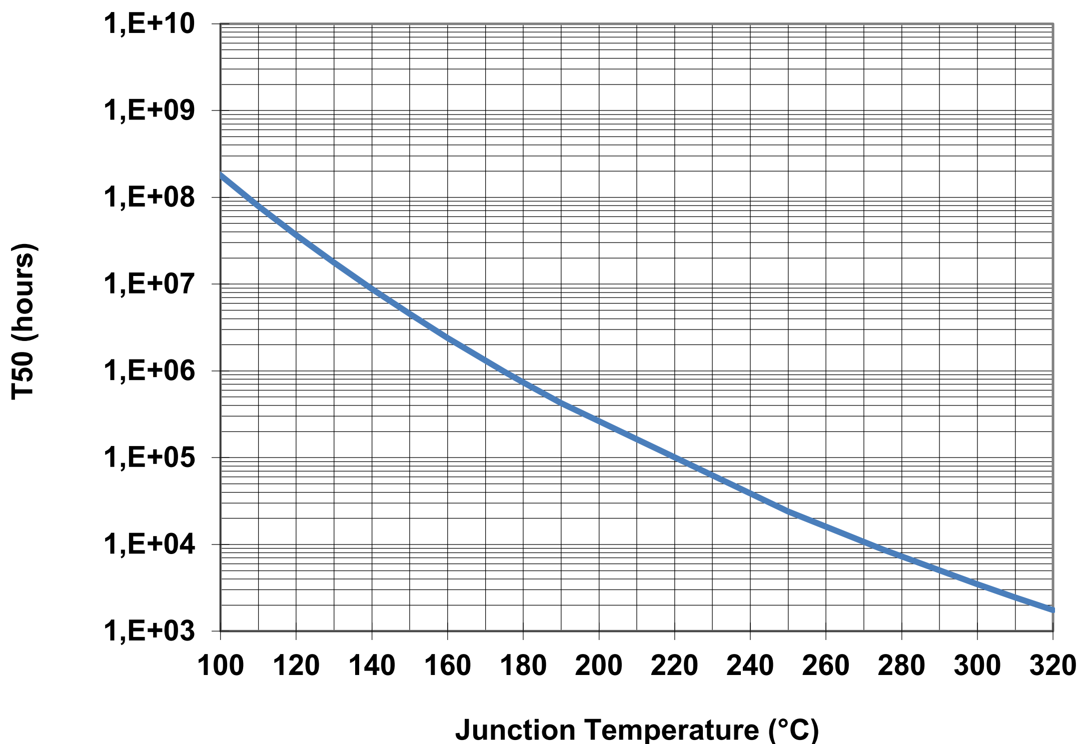
Device thermal performances

The device thermal performances below are based on UMS rules to evaluate the junction temperature.
This same procedure is the basis for junction temperature evaluation of the samples used to derive the Median lifetime and activation energy for the particular technology on which the CHA8362-99F is manufactured (GaN HEMT 0.15µm).
The temperature T_{case} is defined as the chip backside temperature. The thermal resistance (Rth_eq), given in the following table, is for the full circuit in CW mode.

Thermal Resistance [1]	R_{th_eq}	T_{case} = 25°C, Vd = 25V, Idq = 440 mA, Pin = 26 dBm, Freq = 29GHz, Pdiss = 56 W	1.27	°C/W
Junction Temperature	T_j		95	°C
Median Life	T50		>2E8	Hrs
Thermal Resistance [1]	R_{th_eq}	T_{case} = 85°C, Vd = 25V, Idq = 440 mA, Pin = 26 dBm, Freq = 29GHz, Pdiss = 54 W	1.71	°C/W
Junction Temperature	T_j		184	°C
Median Life	T50		5.9E5	Hrs

[1] Thermal resistance measured at the backside of the chip



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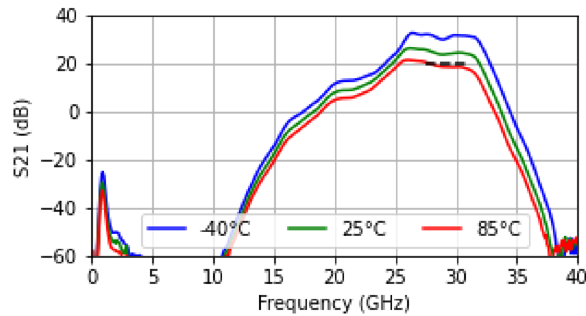
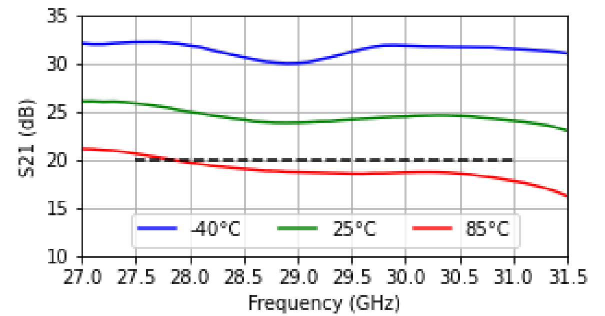
Typical Board Measurements : Small Signal Performances

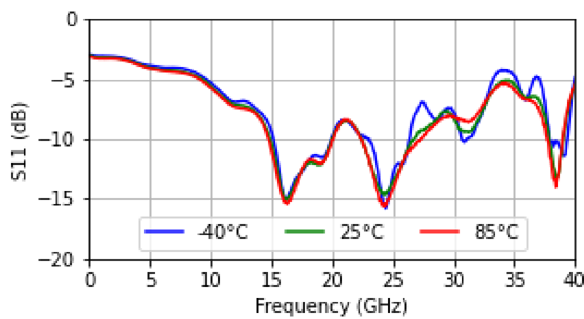
Performance versus temperature

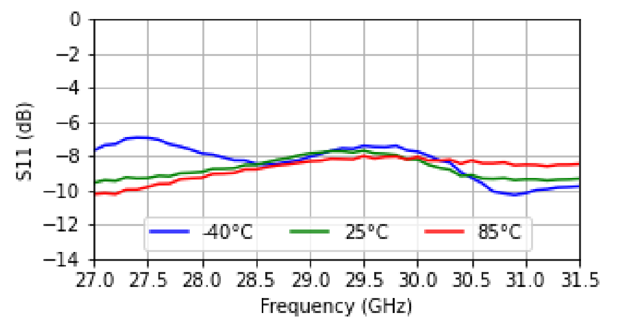
Test conditions : CW, V_D = 25V, I_{DQ} = 440mA, T_{case} = -40°C / 25°C / 85 °C

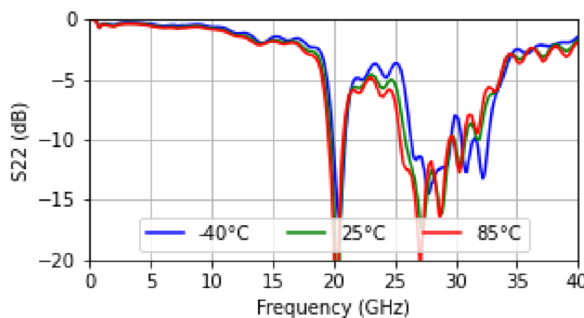
Measurements reference plane is de-embedded at the wire bondings plane on the RF feed line.

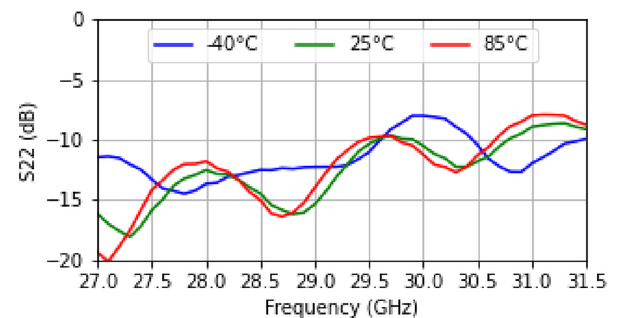












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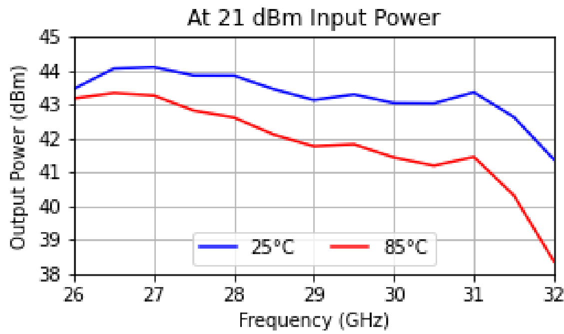
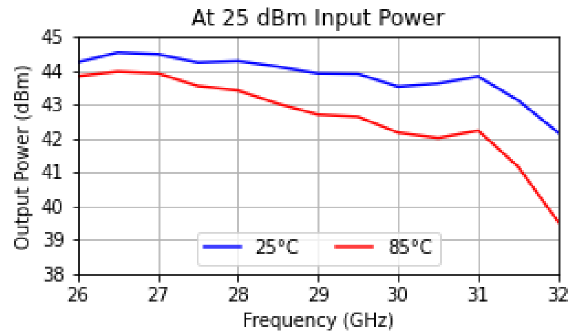
Typical Board Measurements : Large Signal Performances

Performance versus frequency versus temperature

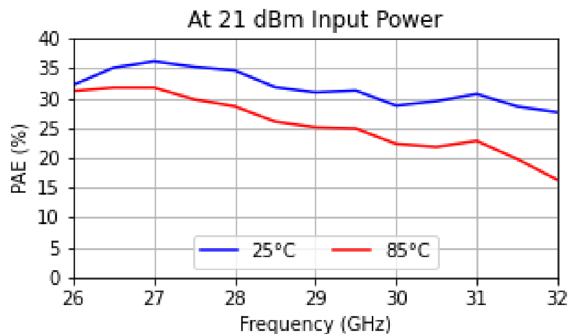
Test conditions : CW, V_D = 25V, I_{DQ} = 440mA, T_{case} = 25°C / 85 °C

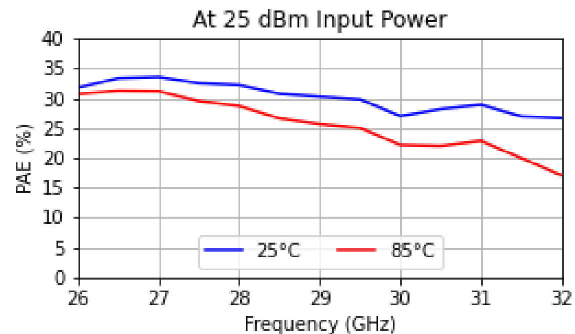
Output Power versus Frequency versus Chip Backside Temperature



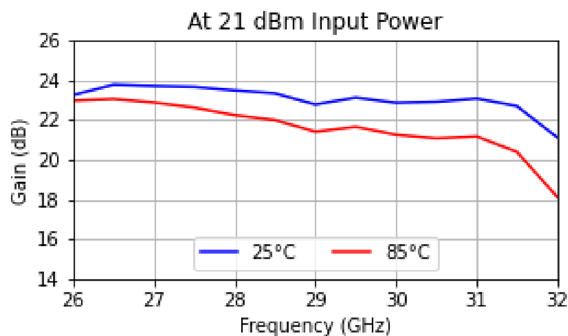


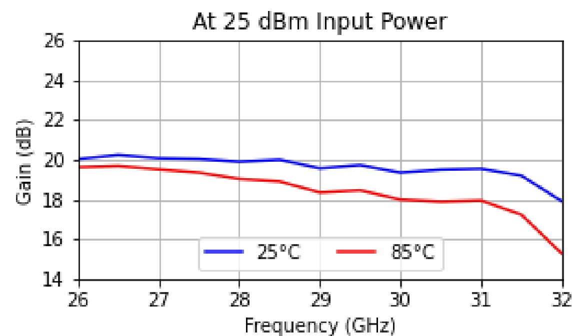
Power Added Efficiency versus Frequency versus Chip Backside Temperature



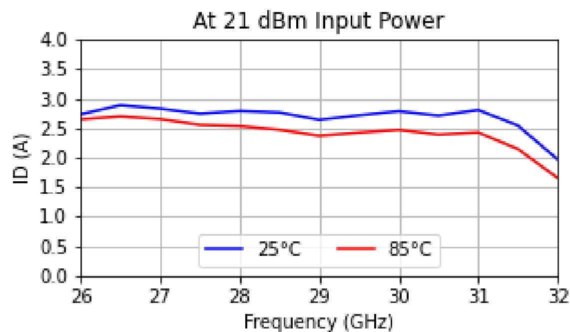


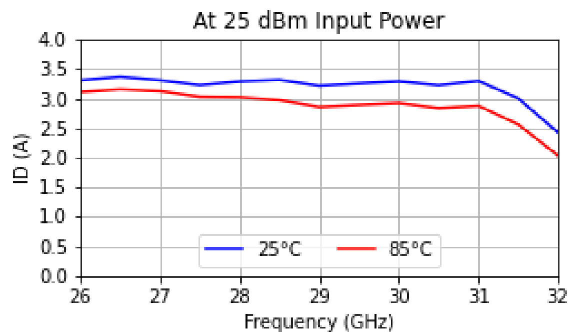
Gain versus Frequency versus Chip Backside Temperature





DC Drain current versus Frequency versus Chip Backside Temperature





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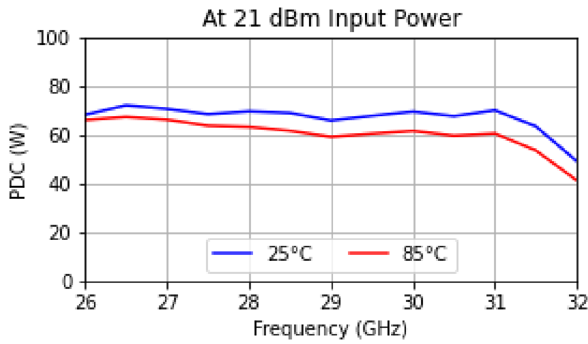
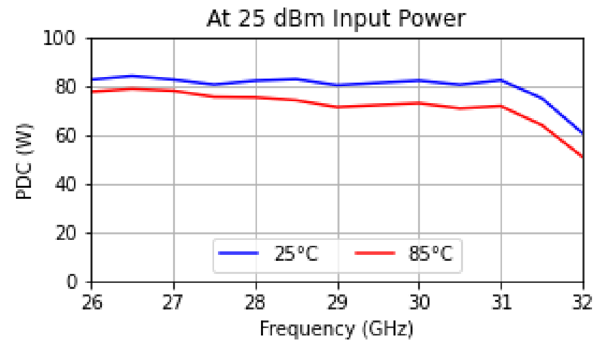
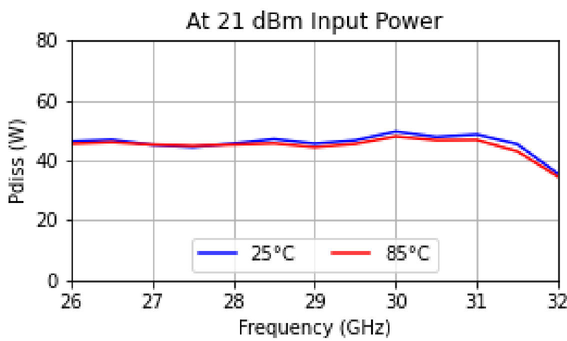
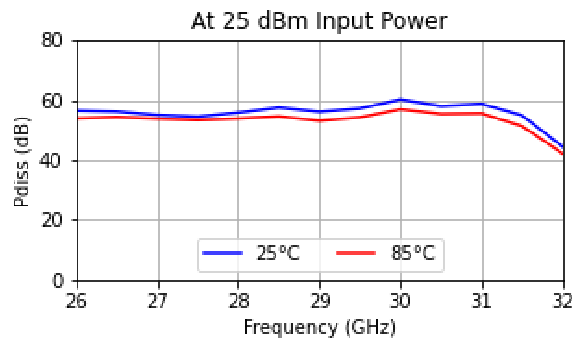
DC Power Consumption versus Frequency versus Chip Backside Temperature





Dissipated Power versus Frequency versus Chip Backside Temperature





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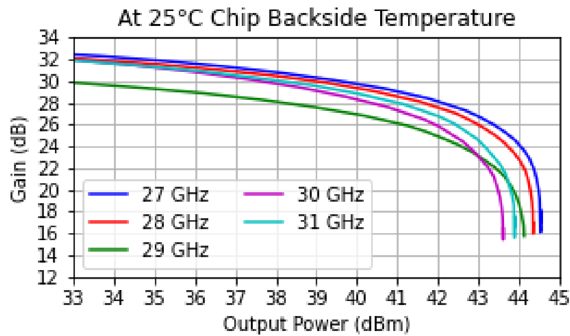
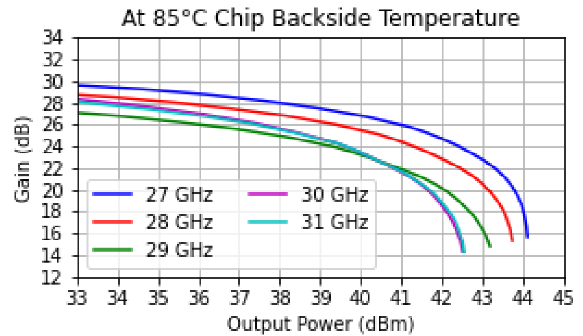
Typical Board Measurements : Large Signal Performances

Performance versus output power versus frequency

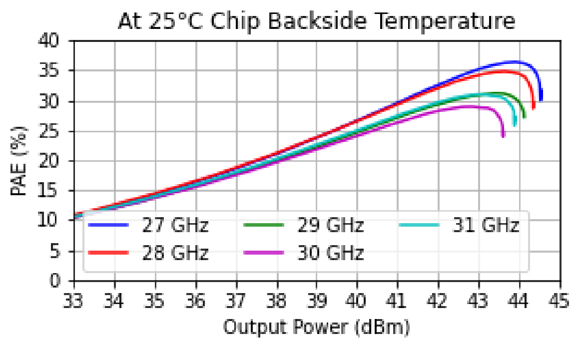
Test conditions : CW, V_D = 25V, I_{DQ} = 440mA, T_{case} = 25°C / 85 °C

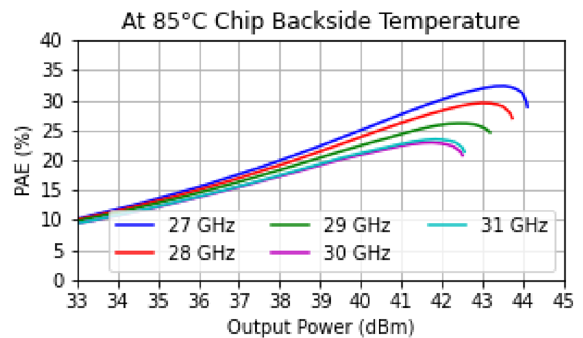
Gain versus Output Power versus Chip Frequency



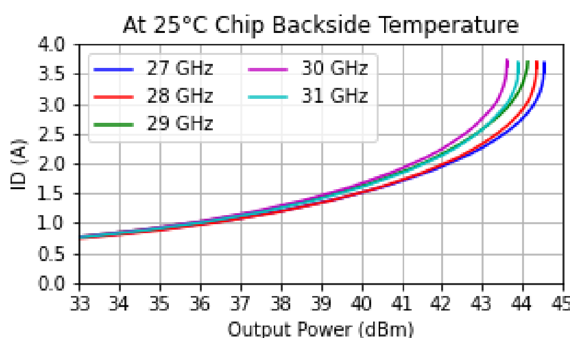


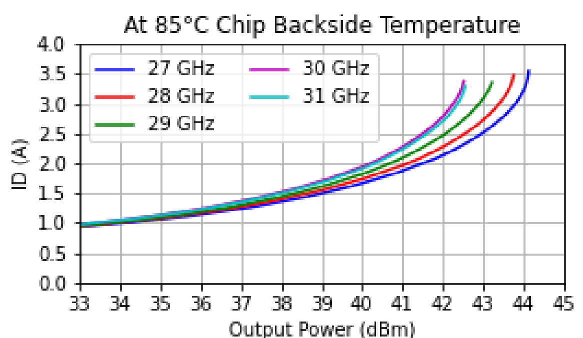
Power Added Efficiency versus Output Power versus Chip Frequency





DC Drain Current versus Output Power versus Chip Frequency





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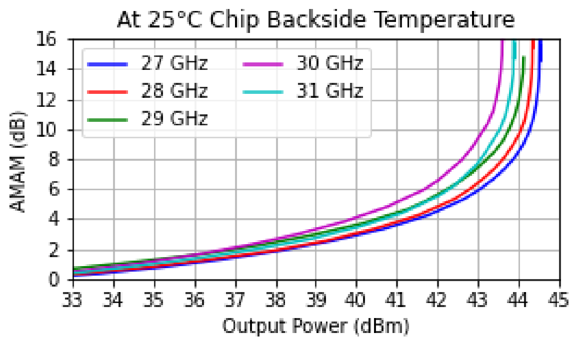
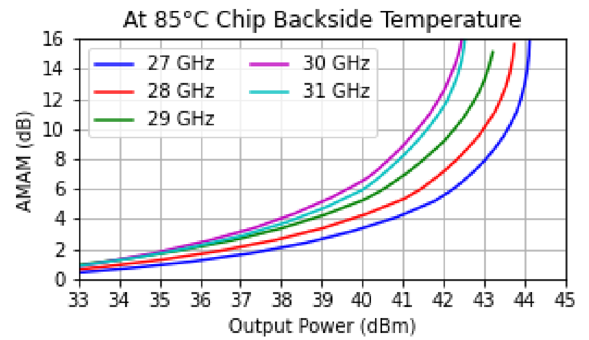
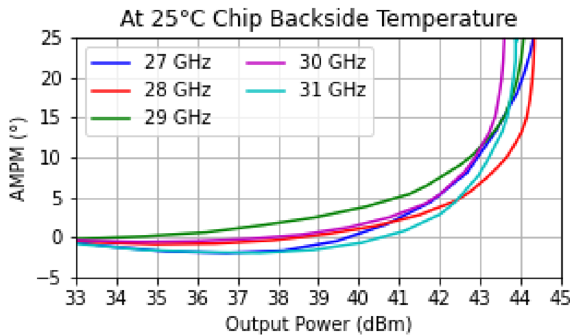
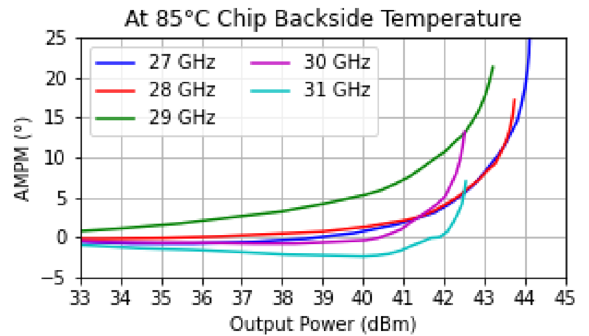
AMAM versus Output Power versus Chip Frequency





AMPM versus Output Power versus Chip Frequency





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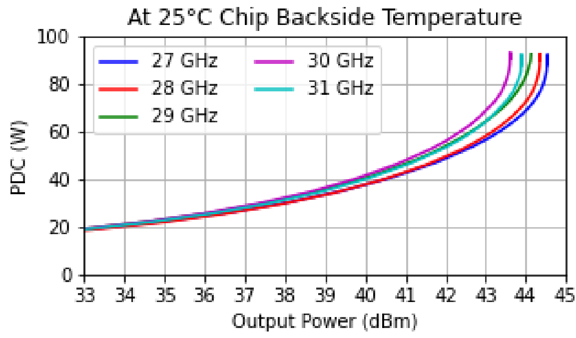
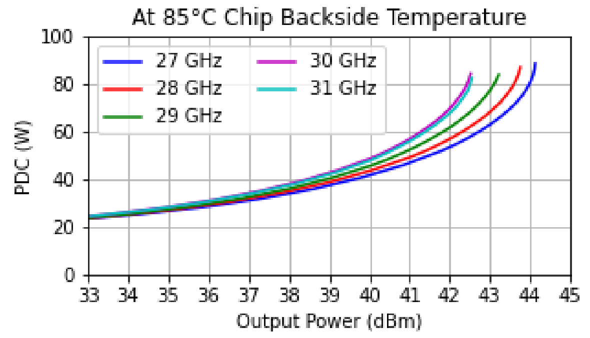
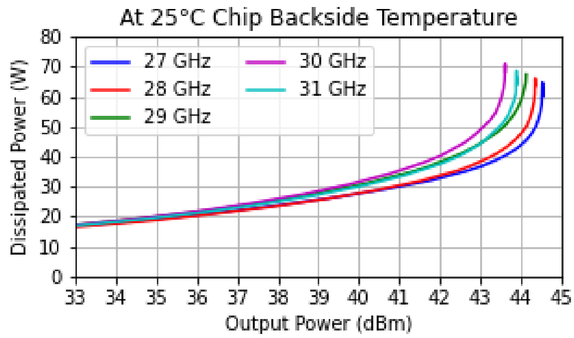
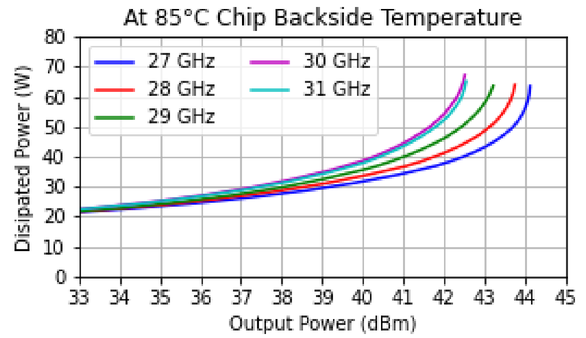
DC Power Consumption versus Output Power versus Chip Frequency





Dissipated Power versus Output Power versus Chip Frequency





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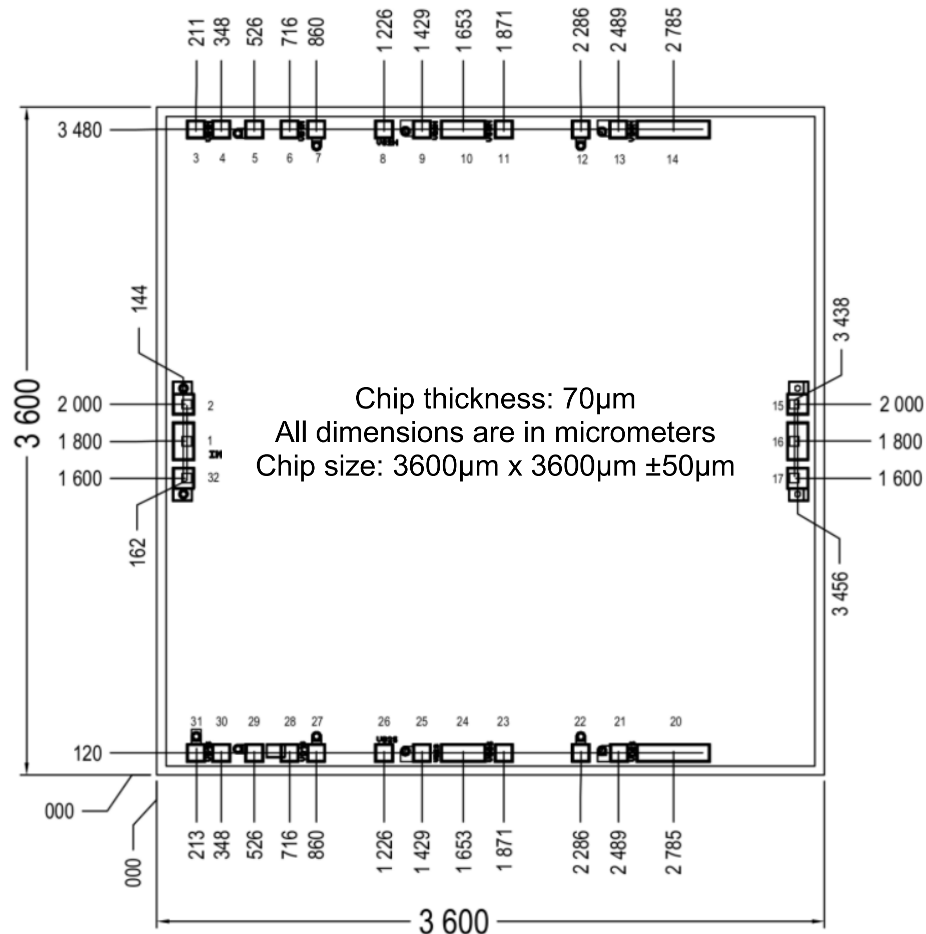
Mechanical Drawing



PAD Number	Name	Description	Pad size (BCB Opening)
1	RF IN	Input RF port	185µm x 200µm
4	G1	DC Gate voltage, 1st Stage, North	100µm x 100µm
6	D1	DC Drain voltage, 1st Stage, North	100µm x 100µm
8	G2	DC Gate voltage, 2d stage, North	100µm x 100µm
10	D2	DC Drain voltage, 2d stage, North	245µm x 100µm
11	G3	DC Gate voltage 3d stage, North	100µm x 100µm
14	D3	DC Drain voltage, 3d stage, North	400µm x 96µm
16	RF OUT	Output RF port	185µm x 200µm
20	D3	DC Drain voltage, 3d stage, South	400µm x 96µm
23	G3	DC Gate voltage 3d stage, South	100µm x 100µm
24	D2	DC Drain voltage, 2d stage, South	245µm x 100µm
26	G2	DC Gate voltage, 2d stage, South	100µm x 100µm
28	D1	DC Drain voltage, 1st Stage, South	100µm x 100µm
30	G1	DC Gate voltage, 1st Stage, South	100µm x 100µm
2,3,5,7,9,12, 13,15,17,21,22, 25,27,29,31,32	GND	Ground	100µm x 100µm

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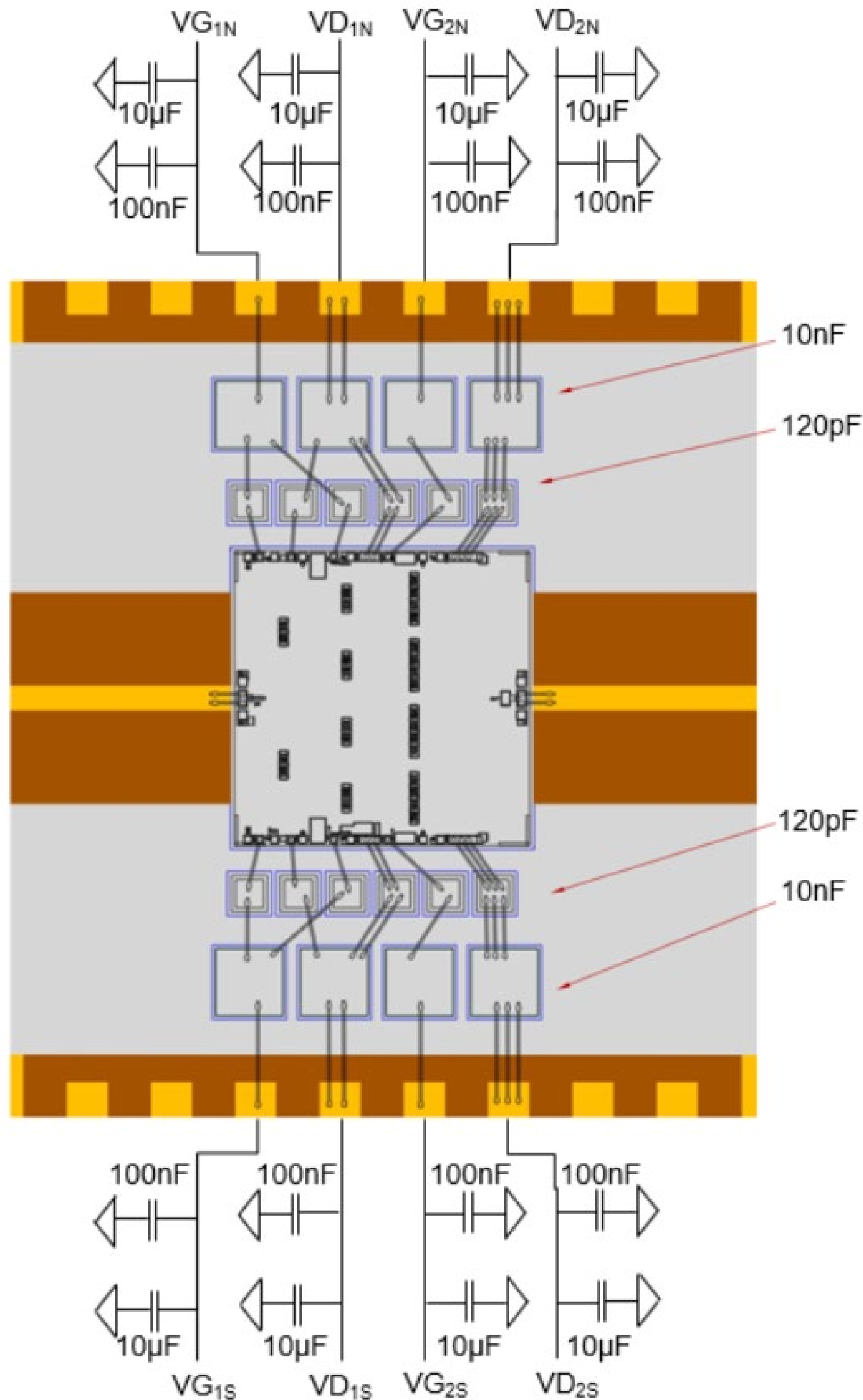
Recommended Assembly Plan



4 levels of decoupling capacitor have been used, 2 on the tab and 2 on the board. The first level is composed of 120 pF chip capacitors, the second level is composed of 10nF chip capacitors, the third level is composed of 100nF SMD 1210 capacitors and the fourth stage is composed of 1µF SMD 1206 capacitors. The first two levels should be as close as possible to the die.

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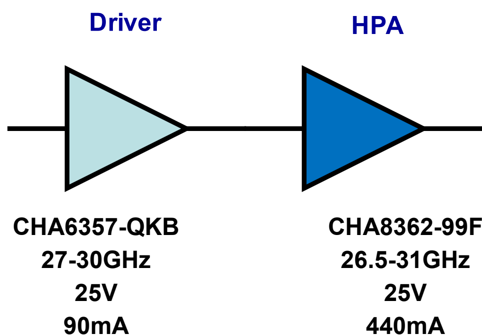
Recommended UMS Power chain

The CHA8362-99F is recommended with the CHA6357-QKB as driver.
Total Gain: > 50dB
For more information about the CHA6357-QKB, see our web site www.ums-rf.com



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Recommended reflow process assembly

Refer to the application note AN0001 available at https://www.ums-rf.com for die attach.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at https://www.ums-rf.com.

Recommended ESD management

Refer to the application note AN0020 available at https://www.ums-rf.com for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

Chip form : CHA8362-99F/00

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