United Monolithic Semiconductors

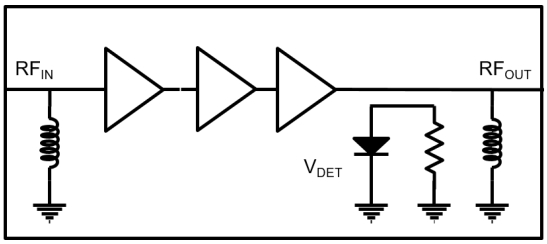
CHA6682-98F

24-27.5GHz 5W Power Amplifier

GaN Monolithic Microwave IC Bare Die

Description

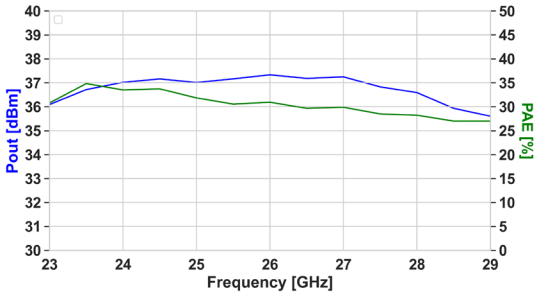
The CHA6682-98F is a three stage High Power Amplifier operating between 24 and 27.5GHz providing 5W of saturated output power with 32% of Power Added Efficiency. It includes a power detector. The amplifier exhibits more than 25dB small signal gain with a typical power supply of 20V/115mA quiescent current. This High Power Amplifier is dedicated to telecommunication applications and well suited for a wide range of microwave applications and systems.
The circuit is manufactured on a robust GaN on SiC HEMT process and is available as a bare die with BCB protection layer. The input and output are matched to 50Ω and integrate ESD RF protection.



Main Features

- Frequency range: 24 – 27.5GHz
- High output power: 5W
- High PAE: 32%
- Linear Gain: 25dB
- Output Power Detector
- DC bias: Vd = 20V & Idq = 115mA
- Chip size: 2.5x1.6mm²
- Available in bare die form

V_D = 20V, I_{dq} = 115mA, T_{case} = 25°C, Pin = 18dBm



Main Electrical Characteristics

T_{case} = 25°C (T_{case} : Chip Backside Temperature)

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	24		27.5	GHz
Gain	Linear Gain		25		dB
Psat	Saturated Output Power		37		dBm
PAE	Power Added Efficiency		32		%

United Monolithic Semiconductors S.A.S.
Bât. Charmille - Parc Mosaic - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34 - www.ums-rf.com

Specifications

T_{case} = +25°C, Vd = +25V, CW mode

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	24		27.5	GHz
Gain	Linear Gain		25		dB
Pout	Saturated Output Power		37		dBm
PAE	Power Added Efficiency		32		%
Id	Drain current at saturation		1000		mA
S11	Input Return Loss		-7		dB
S22	Output return loss		-10		dB
Idq	Quiescent current		115		mA
Vd	Drain Voltage		20		V

These values are representative of on-board measurements as defined on the drawing in paragraph "Evaluation board".

Absolute Maximum Ratings (1)

T_{case} = +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	27	V
Idq	Quiescent Drain bias current	1.5	A
Vg	Gate bias voltage	-7 to -1	V
Pin	Maximum Input Power	21	dBm

(1) Operation of this device above anyone of these parameters may cause permanent damage

Recommended Operating Range (2), (3)

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	18 to 25	V
Id	Drain bias current	90 to 150	mA
Vg	Gate bias voltage	-5 to -2.5	V
Pin	Maximum Input Power	18	dBm
Tj	Maximum Junction temperature(4)	200	°C

(2) Electrical performances are defined for specified test conditions

(3) Electrical performances are not guaranteed over all recommended operating conditions

(4) See Device thermal performances section

Temperature Range

T_{case}	Operating temperature range	-40 to +85	°C
T_{stg}	Storage temperature range	-55 to +150	°C

Bât. Charmille - Parc Mosaic - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34 - www.ums-rf.com

Typical Bias Conditions

T_{case} = 25°C

Symbol	Pad N°	Parameter	Values	Unit
Vg	6, 13, 17, 19	Gate voltage tuned for Idq = 115mA	~ -3	V
Vd	2, 4, 11, 15	Drain voltage	20	V
Vc	8	Control voltage	5	V

“Power ON” sequence

1. Bias HPA gate voltage at Vg close to Vpinch-off (Vg~-5V)
2. Set Vd bias voltage to 0V: Id=0mA
3. Apply Vd bias voltage, Vd = 20V: Id=0mA
4. Set Vc bias voltage to 5V for Detector biasing
5. Increase Vg up to quiescent bias drain current Idq=216mA
6. Apply RF input Power

“Power OFF” sequence

1. Turn off RF input power
2. Bias HPA Gate voltage at Vg~-5V: Id=0mA
3. Decrease Vd bias voltage down to 0V
4. Set Vc bias voltage to 0V
5. Turn Vg bias voltage to 0V

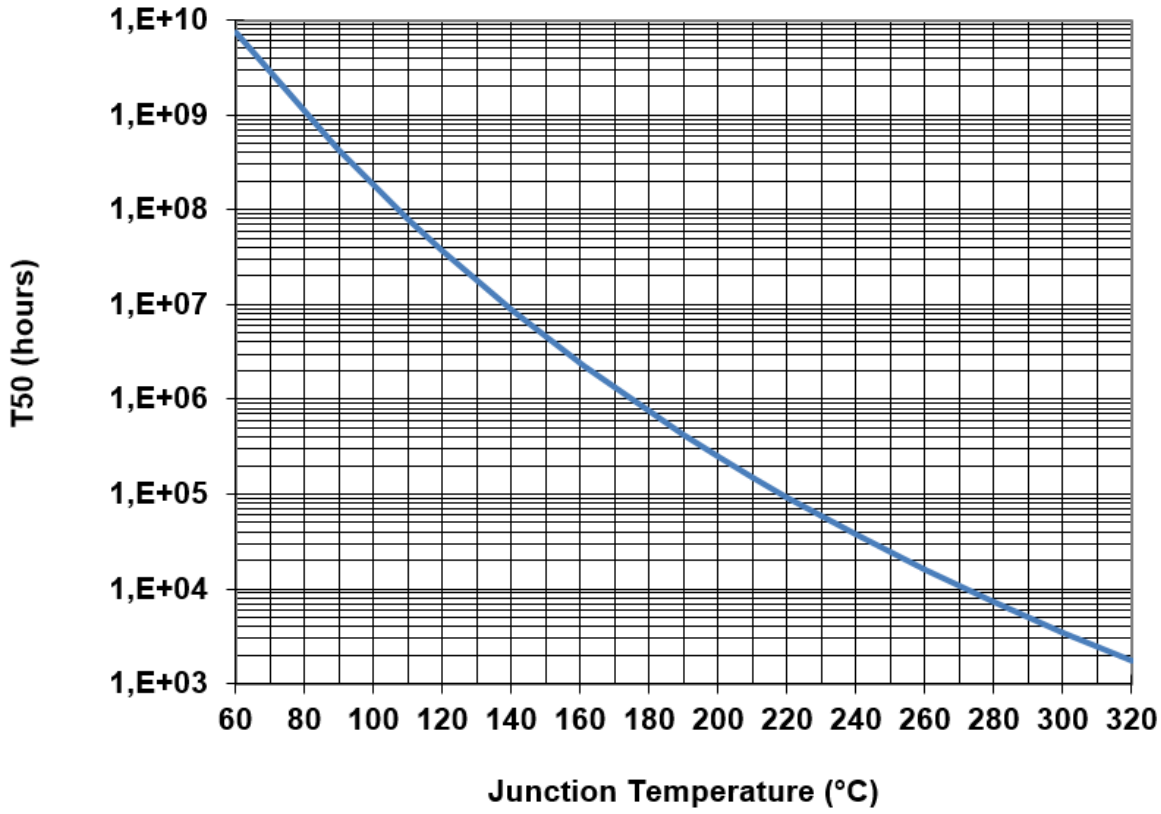
Bât. Charmille - Parc Mosaic - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34 - www.ums-rf.com

Device thermal performances

The device thermal performances below are based on UMS rules to evaluate the junction temperature.
This same procedure is the basis for junction temperature evaluation of the samples used to derive the Median lifetime and activation energy for the particular technology on which the CHA6682-98F is manufactured (GaN HEMT 0.15µm).
The temperature T_{case} is defined as the chip backside temperature. The thermal resistance ($R_{th\_eq,}$) given in the following table, is for the full circuit in CW mode.

Thermal Resistance (1)	R_{th_eq}	T_{case} = 25°C, Vd = 20V, Idq = 115 mA, Pin = 18 dBm, Freq = 26GHz, Pdiss = 12 W	4.61	°C/W
Junction Temperature	T_j		76	°C
Median Life	T50		1.52E+09	Hrs
Thermal Resistance (1)	R_{th_eq}	T_{case} = 85°C, Vd = 20V, Idq = 115 mA, Pin = 21 dBm, Freq = 26GHz, Pdiss = 13 W	6.22	°C/W
Junction Temperature	T_j		161	°C
Median Life	T50		2.26E+06	Hrs

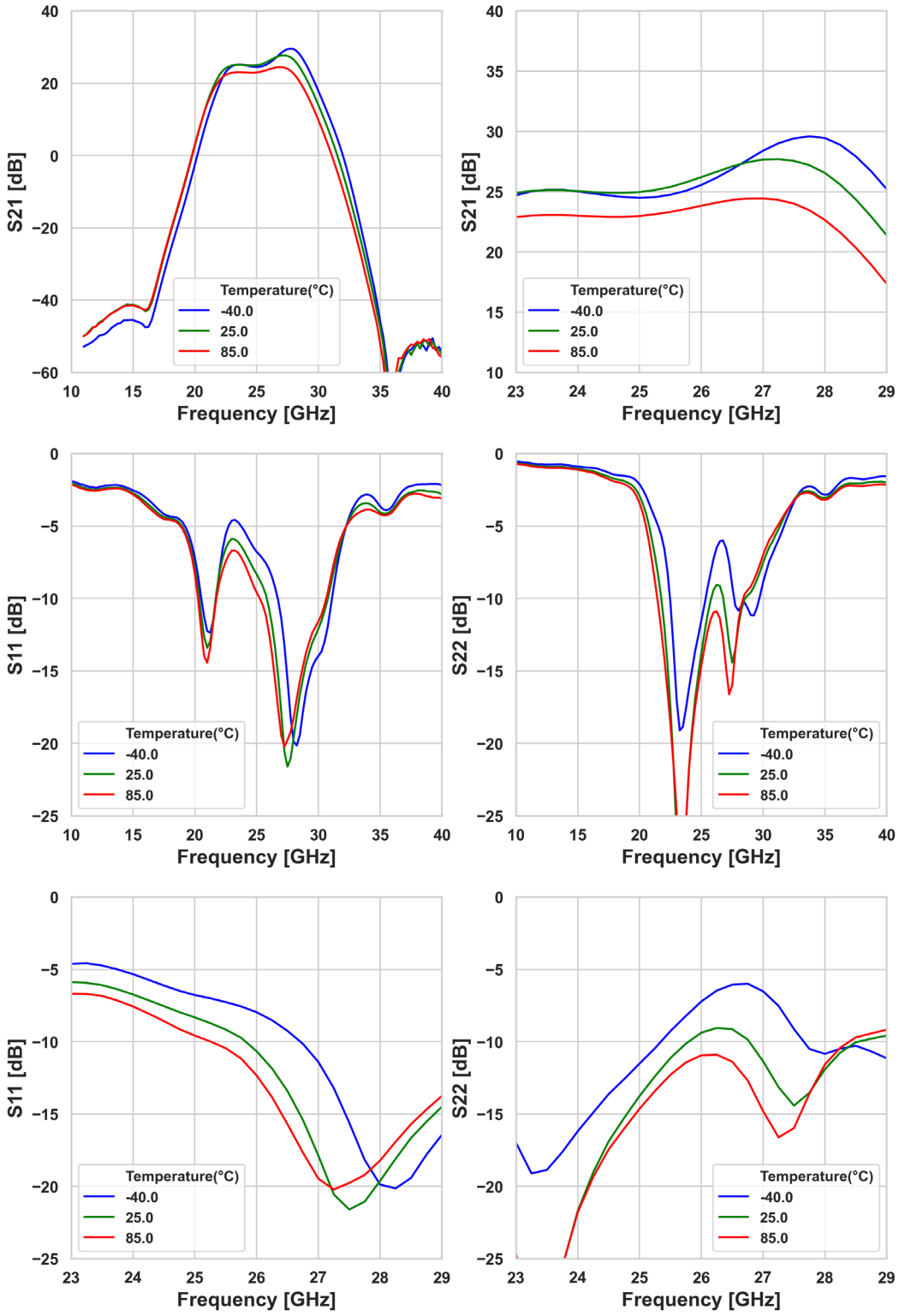
(1) Thermal resistance measured at the backside of the chip



Bât. Charmille - Parc Mosaic - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34 - www.ums-rf.com

Typical Board Measurements : Small Signal Performances

CW measurements: Vd = 20V, Idq = 115mA, T_{case} = -40°C / 25°C / 85°C
Board losses are de-embedded. Measurements are given in die reference planes.

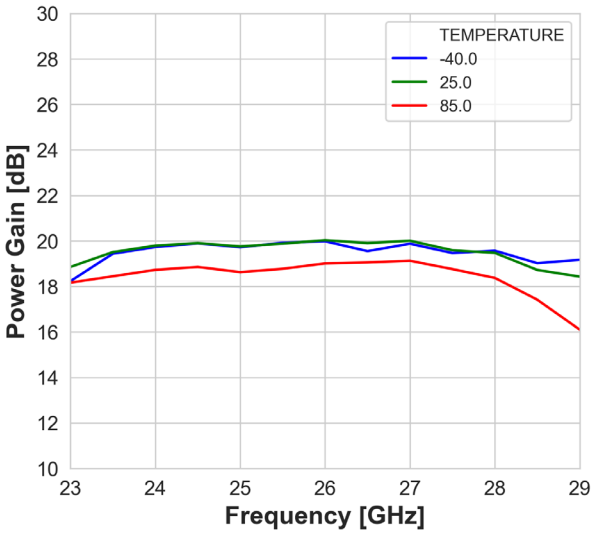


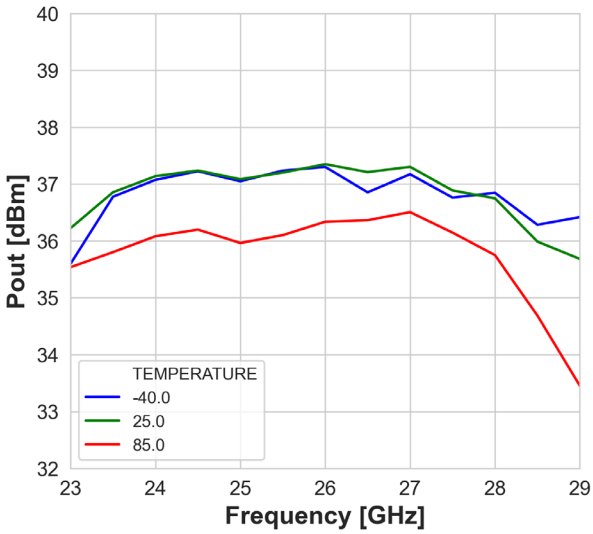
Bât. Charmille - Parc Mosaic - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34 - www.ums-rf.com

Typical Board Measurements : Large Signal Performances

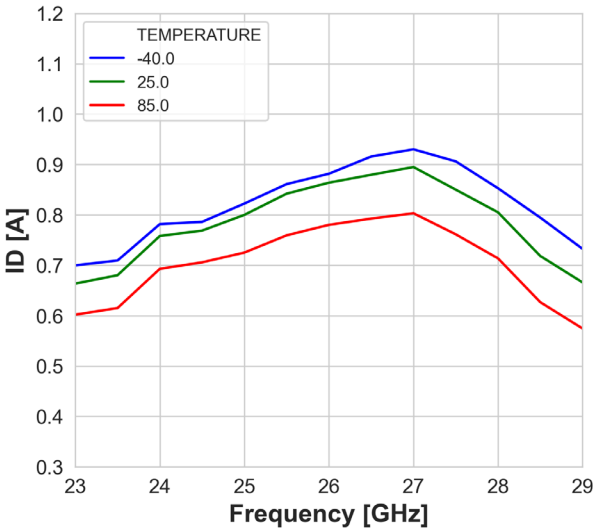
CW measurements : Pin = 18dBm, Vd = 20V, Idq = 115mA (adjusted at 25°C)
Board losses are de-embedded. Measurements are given in die reference planes.

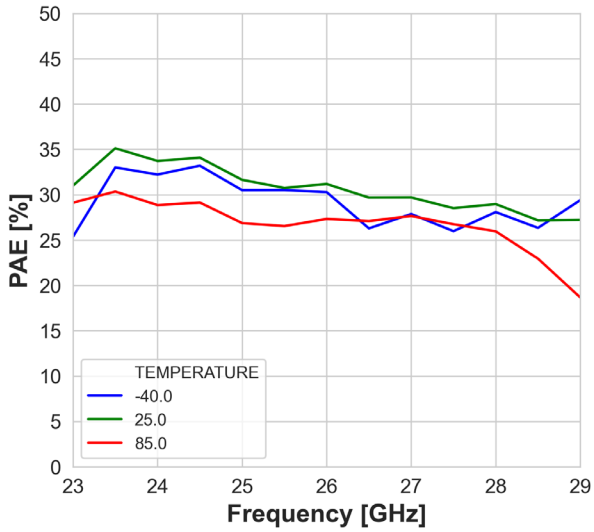
Power Gain & Output Power vs Frequency & Chip Backside Temperature





Drain current & Power Added Efficiency vs Frequency & Chip Backside Temperature

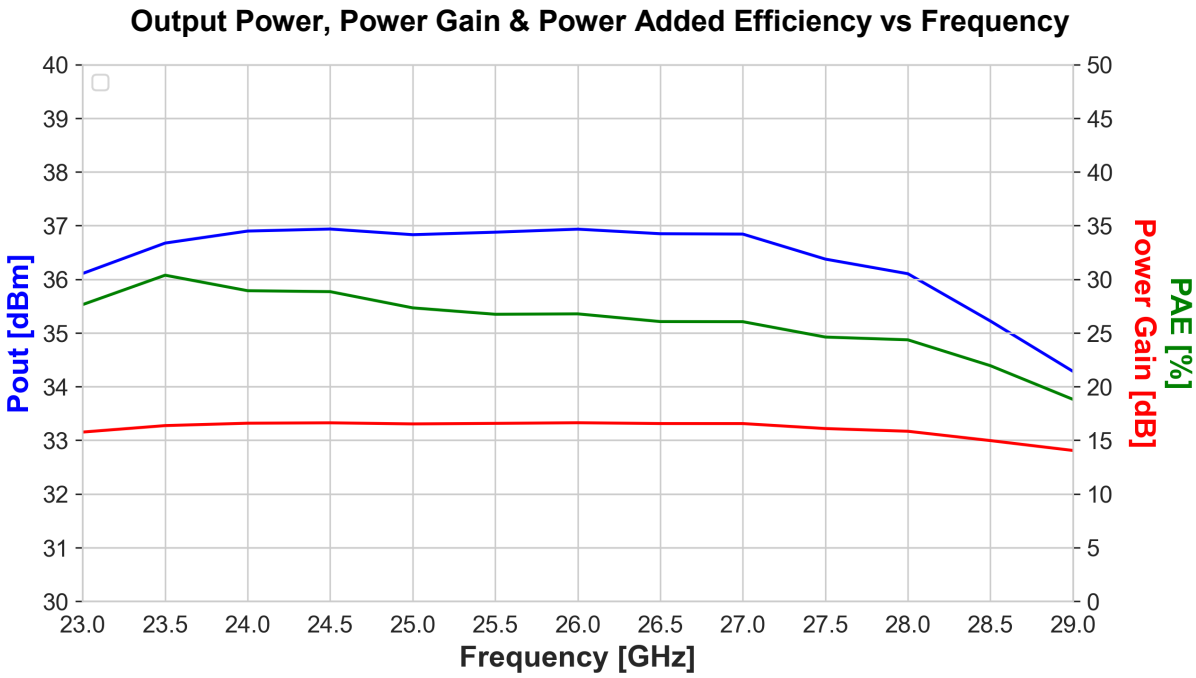




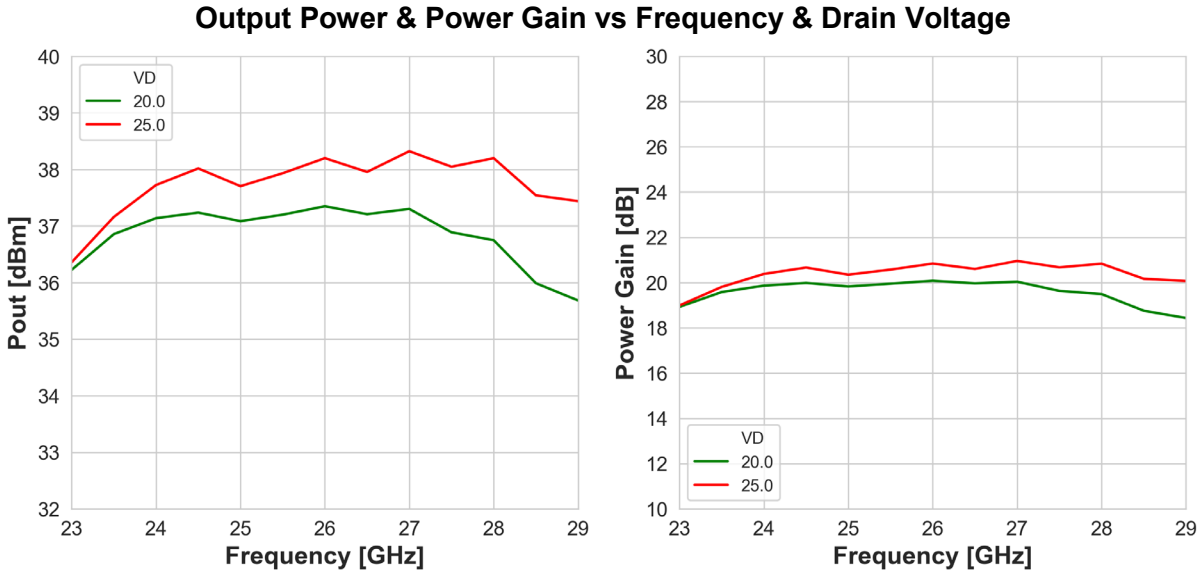
Bât. Charmille - Parc Mosaic - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34 - www.ums-rf.com

Typical Board Measurements : Non-linear performances

CW measurements : Pin = 21dBm, T_{case}=85°C, Vd = 20V, Idq = 115mA (adjusted at 25°C)
Board losses are de-embedded. Measurements are given in die reference planes.



CW measurements : Pin = 18dBm, T_{case} = 25°C, Idq = 115mA (adjusted at 25°C)
Board losses are de-embedded. Measurements are given in die reference plans.

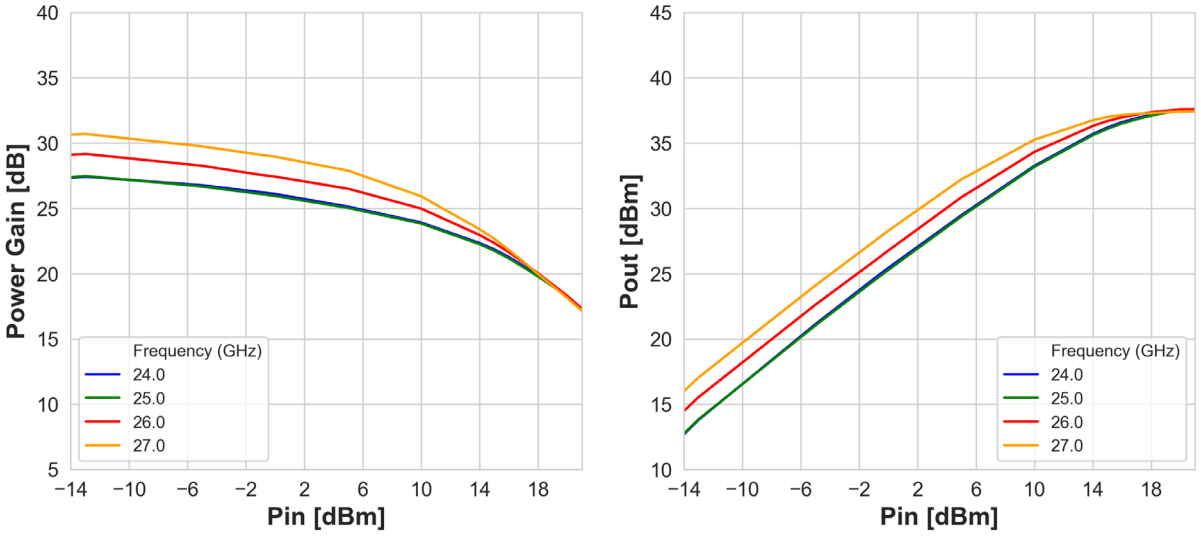


Bât. Charmille - Parc Mosaic - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34 - www.ums-rf.com

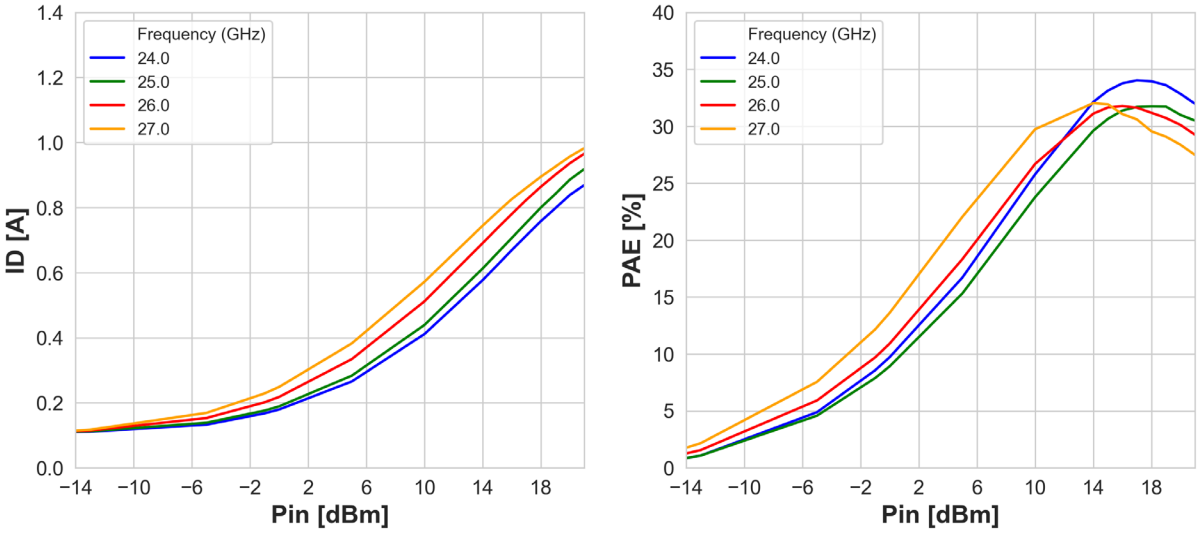
Typical Board Measurements : Non-linear performances

CW measurements : T_{case} = 25°C, Vd = 20V, Idq = 115mA (adjusted at 25°C)
Board losses are de-embedded. Measurements are given in die reference planes.

Power Gain & Output power vs Input Power & Frequency



Drain current & Power Added Efficiency vs Input Power & Frequency

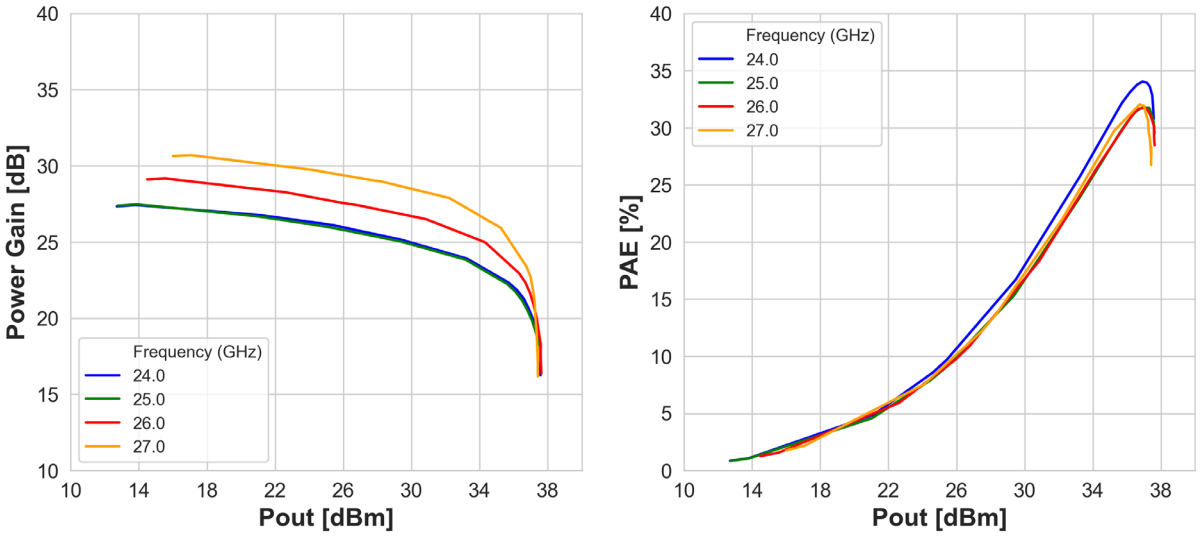


Bât. Charmille - Parc Mosaic - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34 - www.ums-rf.com

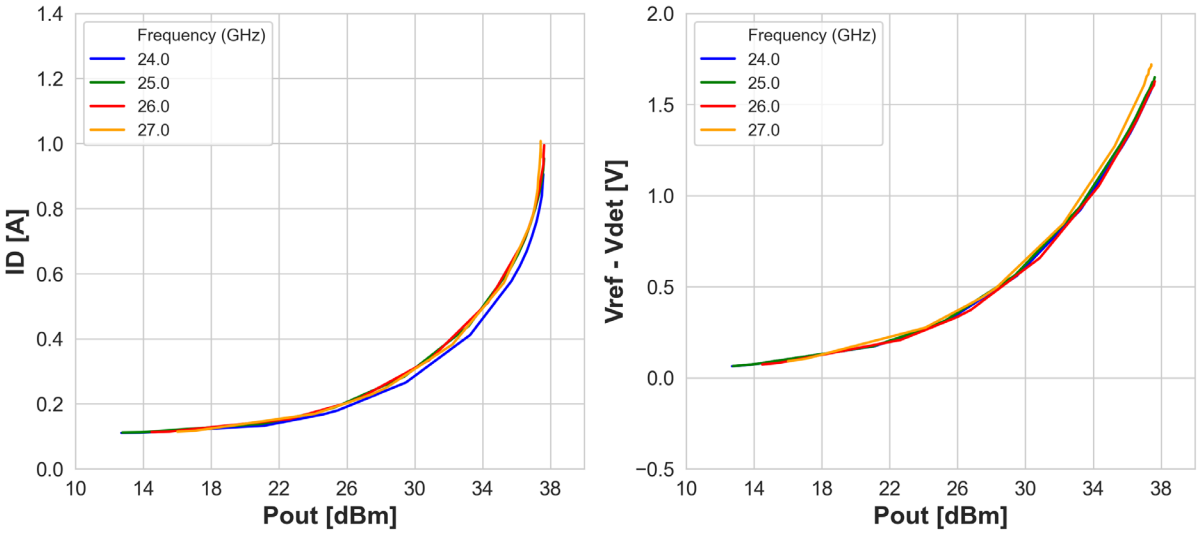
Typical Board Measurements : Non-linear performances

CW measurements : T_{case} = 25°C, Vd = 20V, Idq = 115mA (adjusted at 25°C)
Board losses are de-embedded. Measurements are given in die reference planes.

Power Gain & Power Added Efficiency vs Output Power & Frequency

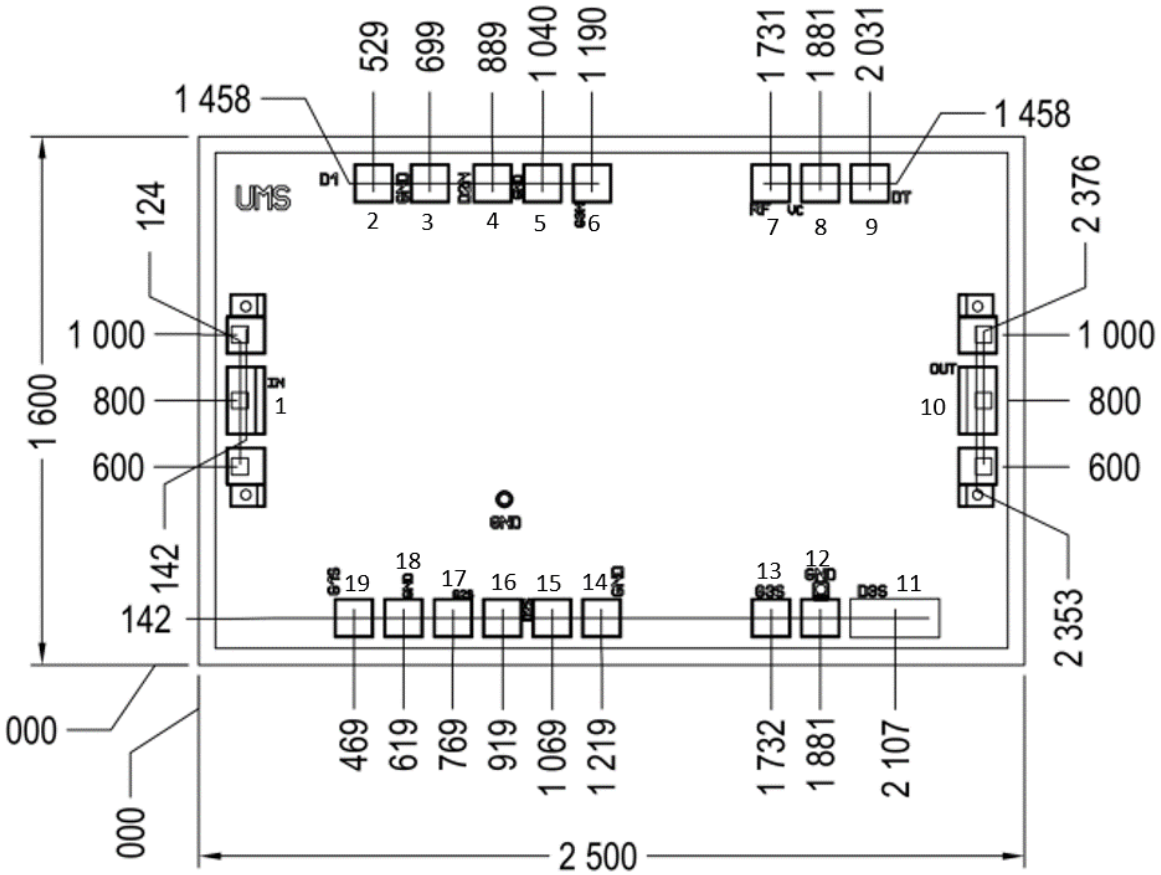


Drain current & Vref - Vdet vs Output Power & Frequency



Bât. Charmille - Parc Mosaic - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34 - www.ums-rf.com

Mechanical data



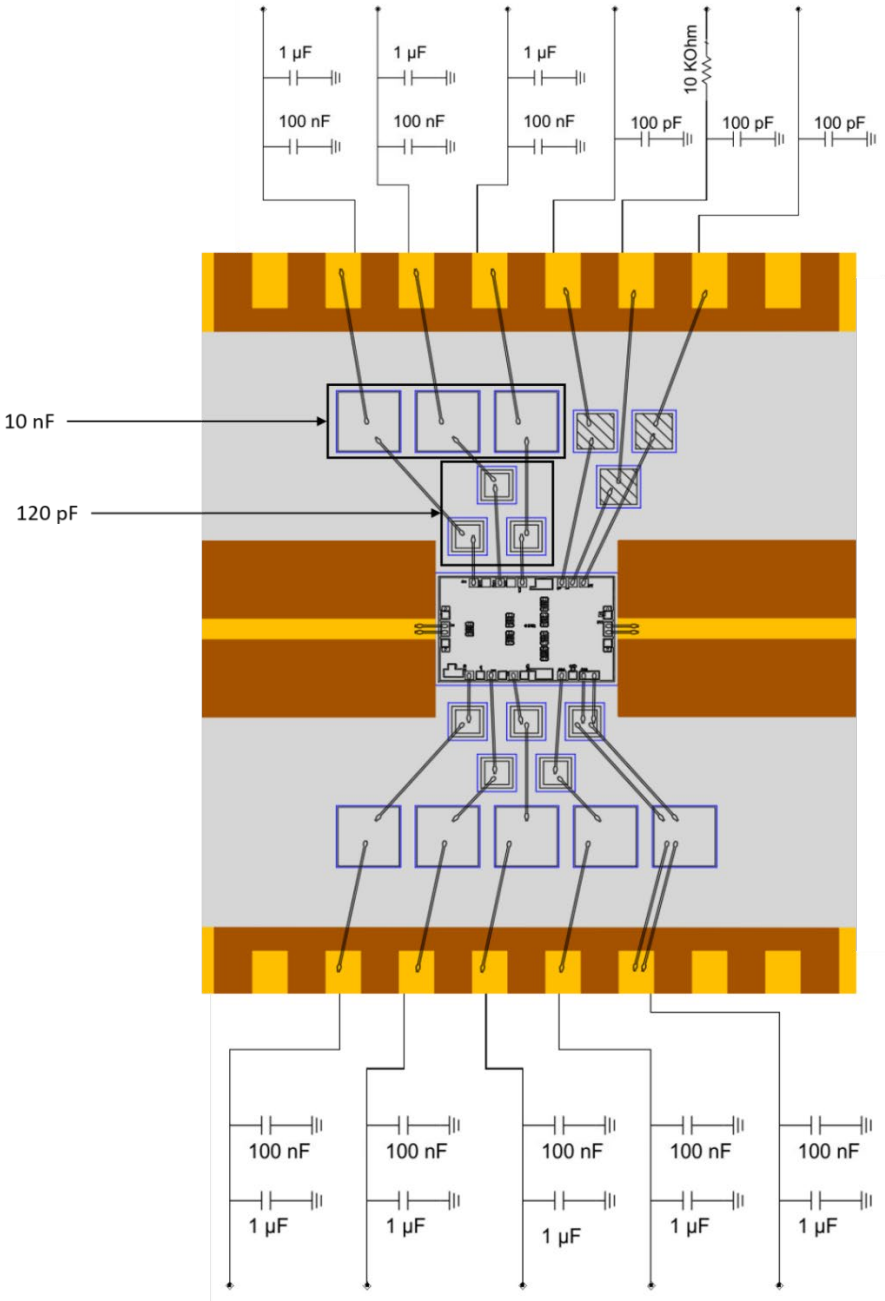
Chip thickness: 70µm.
Chip size: 2500x1600 ±35µm
All dimensions are in micrometers
DC pads (2, 3, 4, 5, 6, 7, 8, 9, 12, 13, 14, 15, 16, 17, 18, 19) size is 116x116µm²
DC pad (1, 10) opening is 216x116µm²
DC pads (11) opening is 269x116µm²

1-	RF_IN	8-	Vc	15-	VD2S
2-	VD1N	9-	VDET	16-	GND(1)
3-	GND(1)	10-	RF_OUT	17-	VG2S
4-	VD2N	11-	VD3S	18-	GND(1)
5-	GND(1)	12-	GND(1)	19-	VG1S
6-	VG3N	13-	VG3S		
7-	VREF	14-	GND(1)		

(1) Ground all pins marked “GND” through the PCB board is strongly recommended. Ensure that the PCB board is designed to provide the best possible ground to the die.

Bât. Charmille - Parc Mosaic - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34 - www.ums-rf.com

Recommended Assembly Plan



The decoupling network used is composed of 4 levels of parallel capacitors. The first level is 120pF chip capacitor, the second level is 10nF chip capacitor, the third level is 100nF chip capacitor and the fourth level is 1µF SMD capacitor. The first two levels should be as close as possible to the die.

ESD sensitivity

Parameter	Classification	Standard
Human Body Model (HBM)	1A	ANSI/ESDA/JEDEC - JS-001

Bât. Charmille - Parc Mosaic - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34 - www.ums-rf.com

Recommended reflow process assembly

Refer to the application note AN0001 available at https://www.ums-rf.com for die attach.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at https://www.ums-rf.com.

Recommended ESD management

Refer to the application note AN0020 available at https://www.ums-rf.com for ESD sensitivity and handling recommendations for the UMS products.

Ordering Information

Chip form :	CHA6682-98F/00

Bât. Charmille - Parc Mosaic - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34 - www.ums-rf.com