United Monolithic Semiconductors

CHK5010-99F

4W Power Transistor

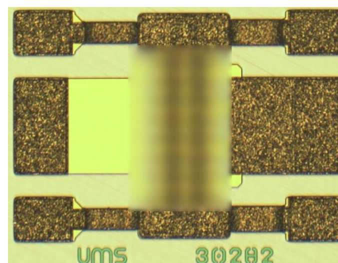
GaN HEMT on SiC

Description

The CHK5010-99F is a 4W Gallium Nitride High Electron Mobility Transistor. This product offers a general purpose and broadband solution for a variety of RF power applications.

The circuit is manufactured with a GaN HEMT technology on SiC substrate.

It is proposed in a bare die form and requires external matching circuitries.



Main Features

- ■ Wide band capability up to 12GHz
- ■ Pulsed and CW operating modes
- ■ GaN technology: High Pout & High PAE
- ■ DC bias: V_D=30V @I_{D_Q}=50mA
- ■ Chip size 0.90x0.80x0.1mm
- ■ Compliance with RoHS N°2011/65
- ■ Compliance with REACh N°1907/2006

Main Electrical Characteristics

Tb [(1)] = +25°C CW mode, Freq = 6GHz, V_{DS} = 30V, I_{D_Q} = 50mA

Symbol	Parameter	Min	Typ	Max	Unit
G_{SS}	Small Signal Gain		21.6		dB
P_{SAT}	Saturated Output Power		36		dBm
PAE	Max Power Added Efficiency		72		dB
G_{PAE_MAX}	Associated Gain at Max PAE		14		dB

[(1)] Tb: Chip Backside Temperature

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Recommended Operating Ratings

T_b = +25°C

Symbol	Parameter	Min	Typ	Max	Unit
V_{DS}	Drain to Source Voltage			30	V
V_{GS}	Gate to Source Voltage		-3.3		V
V_{DG_peak}	Drain-Gate Voltage		80		V
V_{GS_peak}	Gate-Source Voltage	-20			V
I_{D_Q}	Quiescent Drain Current		0.05		A
I_{D_TYP}	Drain Current (1)		0.2		A
I_{G_MAX}	Gate Current in forward mode		0	16	mA
T_{j_MAX}	Junction temperature			200	°C

(1) Power dissipation must be considered, typical drain current at max PAE

DC Characteristics

T_{ref} = +25°C

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
V_P	Pinch-Off Voltage	-4	-3.4	-2.8	V	V_D=10V,I_D= I_{DSS} /100
I_{D_SAT}	Saturated Drain Current		1		A	(1) V_D=10V, V_G=1V
V_{BDG}	Drain-Gate Break-down Voltage		120		V	V_G=-7V, I_D=20mA

(1) For information, limited by I_{D_MAX} , see on ROR & AMR

RF Characteristics

T_{ref} = +25°C, CW mode, Freq = 6GHz, V_{DS} = 30V, I_{D_Q} = 50mA

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
G_{SS}	Small Signal Gain		21.6		dB	
P_{SAT}	Saturated Output Power		36		dBm	
PAE	Max Power Added Efficiency		72		%	
G_{PAE_MAX}	Associated Gain at Max PAE		14		dB	

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Absolute Maximum Ratings [1]

T_{ref} = +25°C[1] [2] [3]

Symbol	Parameter	Values	Unit
V_{DS_Q}	Drain-Source Biasing Voltage	55	V
V_{GS_Q}	Gate-Source Biasing Voltage	-10, -1	V
V_{DG_peak}	Drain-Gate Voltage (DC+RF)	120	V
V_{GS_peak}	Gate-Source Voltage (DC+RF)	-25	V
I_{D_MAX}	Maximum Drain Current (DC+RF)	See note [4]	A
I_{G_MAX}	Maximum Gate Current (DC+RF)	40	mA
P_{IN}	Maximum Input Power	See note [5]	dBm
T_{STG}	Storage Temperature	-55 to +150	°C
$T_{Backside}$	Backside Operating Temperature	See note [4]	°C

[1] Operation of this device above anyone of these parameters may cause permanent damage.

[2] Duration < 1s.

[3] The given values must not be exceeded at the same time even momentarily for any parameter, since each parameter is independent from each other, otherwise deterioration or destruction of the device may take place.

[4] Max junction temperature must be considered.

[5] Linked to and limited by Ig_max value. Maximum input power depends on frequency and should not exceed 2dB above P_{IN} value at PAE_max.

Biasing procedure

1. Bias power bar gate voltage at Vg close to $V_{pinch\text{-}off}$ (Typically: $V_{GS} \approx -5V$)
2. Apply V_{DS} bias voltage (Typically: V_{DS} = 30V)
3. Increase V_{GS} up to quiescent bias drain current I_{D_Q}

The quiescent current steady state must be carefully controlled as it is influenced by the operating mode, the temperature and the overall thermal resistance.
A drain current control is recommended on the biasing network.

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Device thermal information

All the figures given in this section are obtained assuming that the device is only cooled down by conduction through the backside (no convection mode considered).
The temperature is monitored at the chip back-side interface (Tb).
The system maximum temperature must be adjusted in order to guarantee that Tjunction remains below the maximum value specified in the Absolute Maximum Ratings table.
So, the system PCB must be designed to comply with this requirement.

Parameters	**Symbol**	**Conditions**	**Value**	**Unit**
Typical Thermal Resistance	Rth	Bare die characteristic Tb=85°C Pdiss=1.6W Pout=3.7W **CW**	15	°C/W
Junction Temperature	Tj		109	°C

The back side temperature (Tb) is considered uniform on all the surface

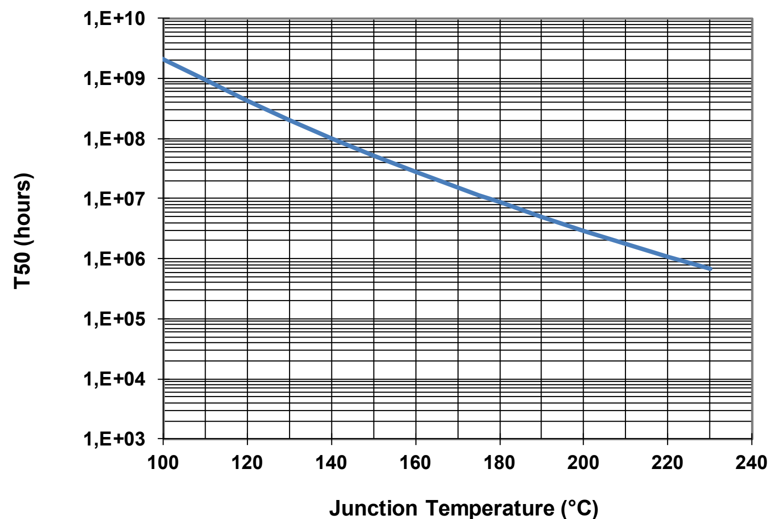
Parameters	**Symbol**	**Conditions**	**Value**	**Unit**
Typical Thermal Resistance	Rth	Bare die characteristic Tb=105°C Pdiss=1.7W Pout=3.5W **CW**	16.1	°C/W
Junction Temperature	Tj		132	°C

The back side temperature (Tb) is considered uniform on all the surface

Parameters	**Symbol**	**Conditions**	**Value**	**Unit**
Typical Thermal Resistance	Rth	Bare die characteristic Tb=125°C Pdiss=1.7W Pout=3.4W **CW**	17.2	°C/W
Junction Temperature	Tj		154	°C

The back side temperature (Tb) is considered uniform on all the surface

Median Life Time versus Junction Temperature



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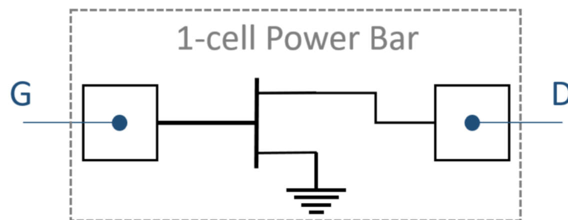
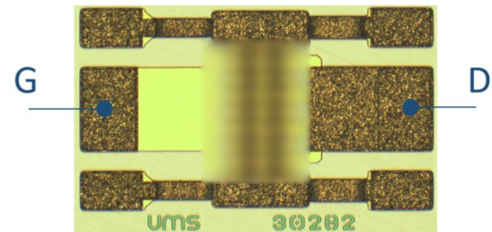
Power Bar Description

The device is composed of 1 elementary 4W cell. The reference plans are on the center of the bonding pads.

A non-linear model is available on request.





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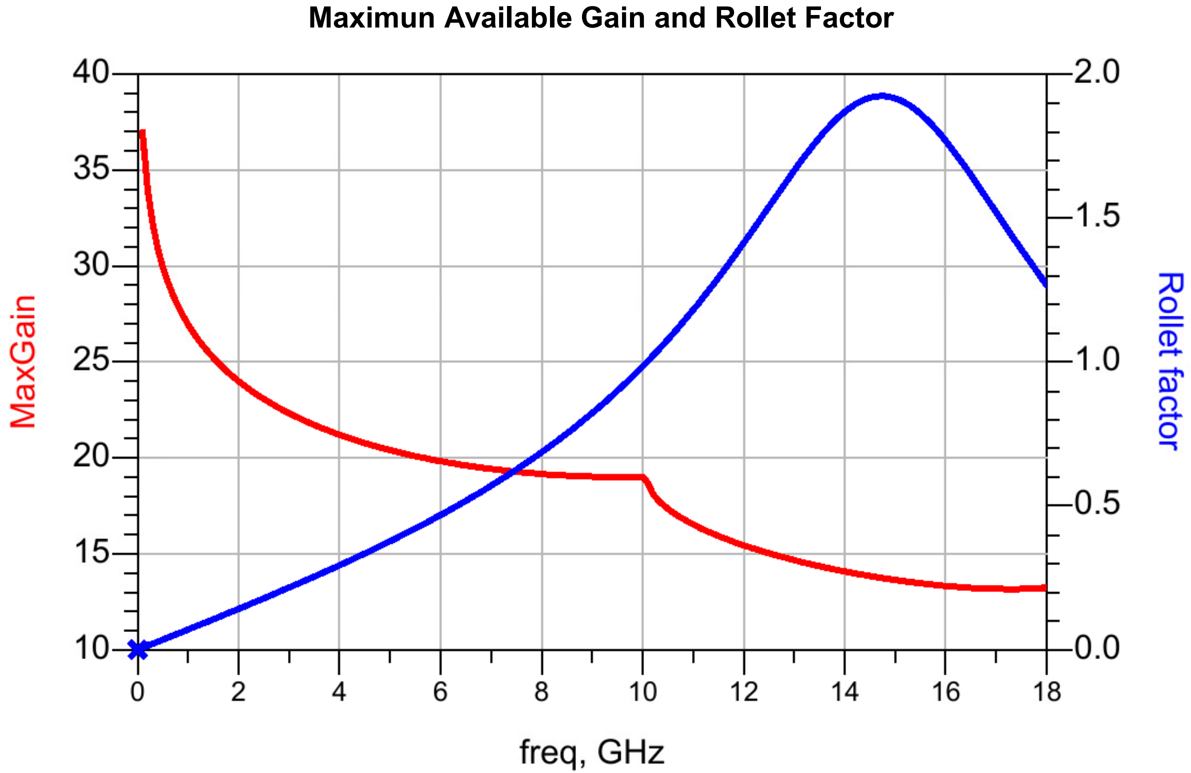
Elementary Cell Maximum Gain & Stability Characteristics

AT +25°C $T_{Backside}$
Frequency range: 0GHz - 18GHz
Bias point: 30V – 50mA/mm



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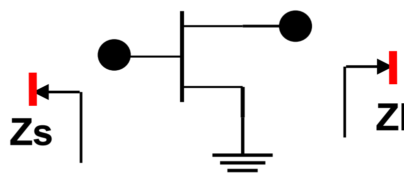
Elementary Cell Load Pull Performances

T_{ref} = +25°C, V_{DS} = +30V, I_{D_Q} = 50mA, simulated results



The impedances are chosen as a trade-off between Output Power, PAE and Stability of the device. Second harmonic of output load has been tuned.
These values are given in the bonding pads reference plan.

Frequency (GHz)	Zs	Zl	Gain (dB) @PAE_{max}	PAE_{max} (%)	Pout (W) @PAE_{max}
2	1.9 + j31	100 + j72	20	72	4.0
4	3 + j15	39 + j68	16	72	4.0
6	2.5 + j10	16.5 + j45	14	72	4.2
8	1.2 + j5.7	10 + j36	12	70	4.0
10	1.1 + j2.9	7.2 + j*28	9.5	65	4.0
12	0.9 + j1	5 + j22	8.5	60	4.0

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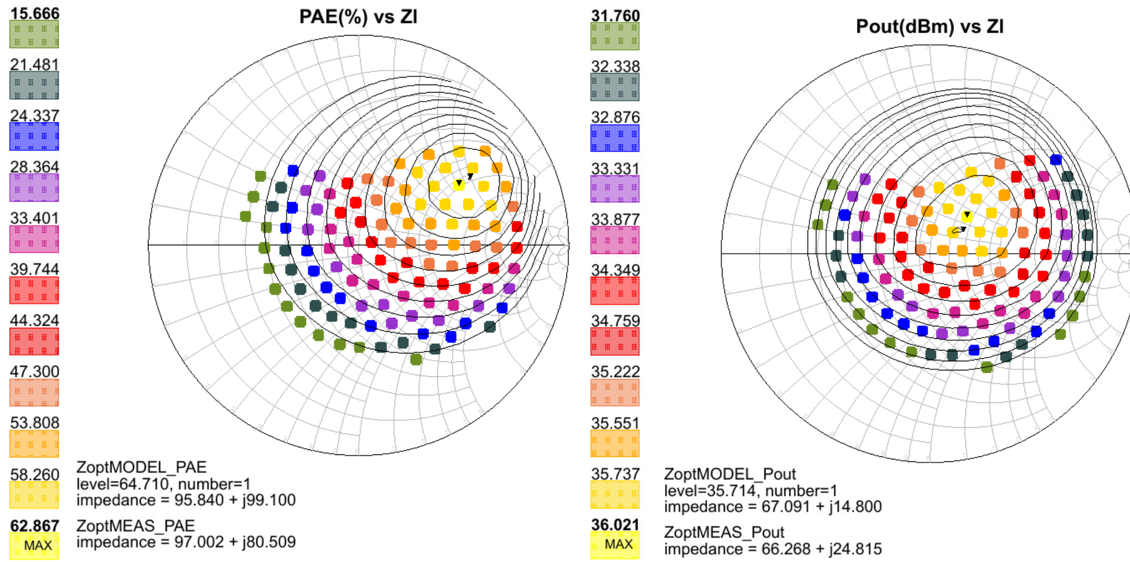
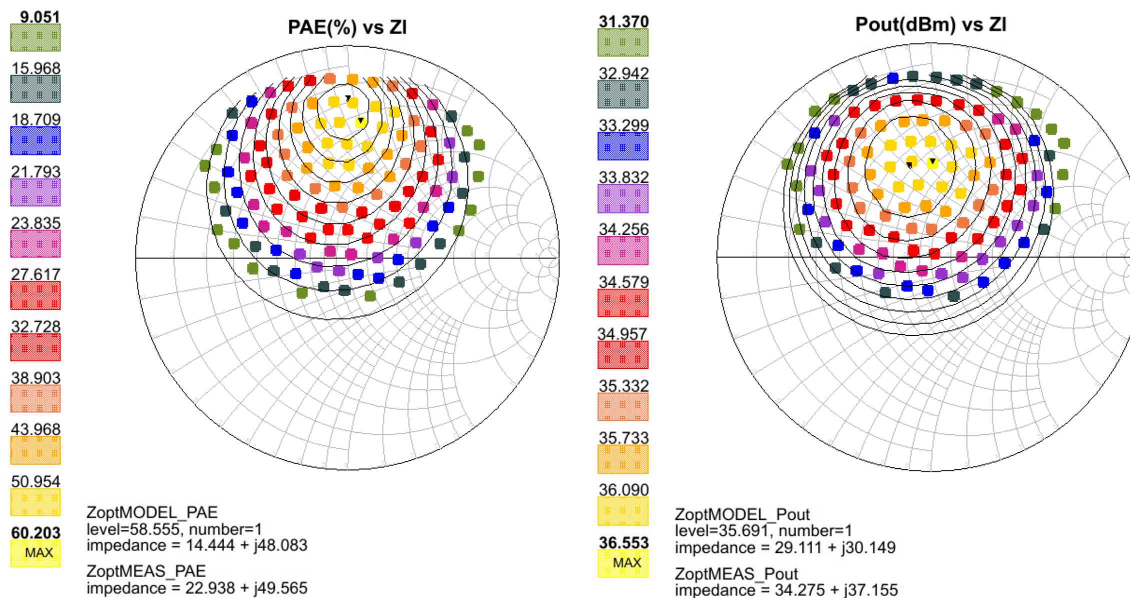
Load-Pull comparison at +25°C $T_{backside}$

Frequency: 2GHz
Bias point: 30V – 50mA/mm
ZoadH2=ZloadH3=50Ω
Zsource=50 Ω



Frequency: 8GHz
Bias point: 30V – 50mA/mm
ZoadH2=ZloadH3=50Ω
Zsource=50 Ω



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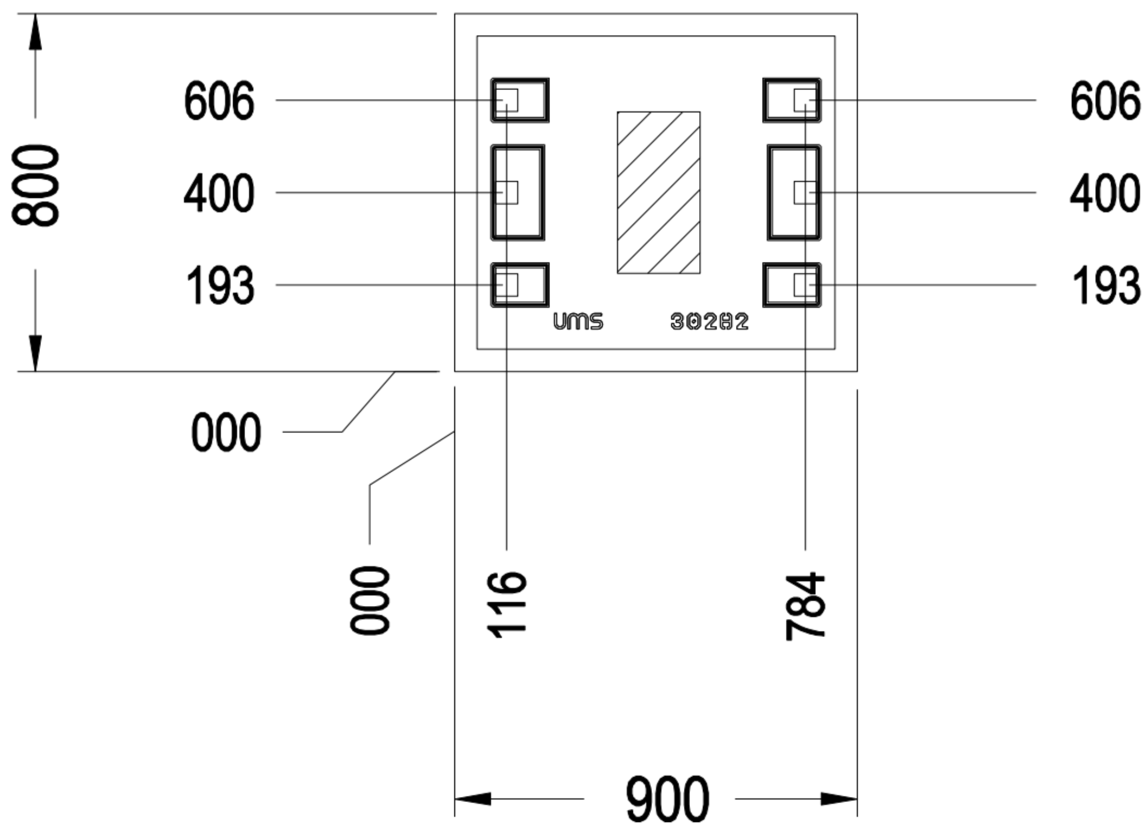
Mechanical data



Chip size: 900µmx800µm +/-50µm
Chip thickness: 100µm +/- 10 µm
All dimensions are in micrometers

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Qualification domain

This part is qualified according to UMS standards, excluding humid environment.

User guide for MMIC storage, pick & place, die attach, wire bonding

Refer to the application note AN0001 available at https://www.ums-rf.com for general recommendations on chip handling.

User guide GaN Power Bars Assembly guide lines

Refer to the application note AN0026 available at https://www.ums-rf.com for general recommendations on GaN-on-SiC Transistor handling and assembly.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at https://www.ums-rf.com.

Recommended ESD management

Refer to the application note AN0020 available at https://www.ums-rf.com for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

Chip form: CHK5010-99F/00

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