United Monolithic Semiconductors

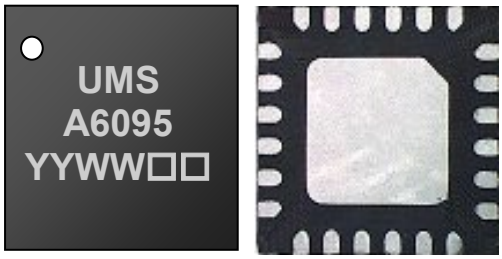
CHA6095-QKB

35-42.5GHz 4W Packaged Power Amplifier

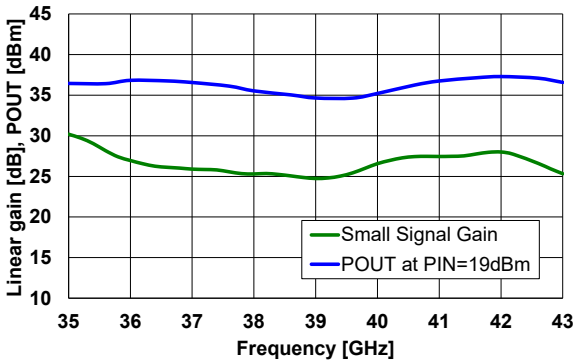
GaN Monolithic Microwave IC in SMD leadless package

Description

The CHA6095-QKB is a GaN packaged monolithic Power Amplifier operating in the 35-42.5GHz frequency range.
It typically exhibits 36dBm saturated output power with 25dB small signal gain. The overall power supply is of 25V/300mA.
It is designed for a wide range of applications, such as 5G applications, active phased array antennas, and telecom applications and systems.
The circuit is available in a standard surface mount 24 leads QFN4x4 cost effective plastic package, compliant with the standards such as the directives RoHS N°2011/65 and REACh N°1907/2006.The input and output are internally matched to 50Ω and integrated ESD RF protection.



Small Signal Gain [dB] and Output Power [dBm] at Pin=20dBm and T°=25°C versus Frequency [GHz]



Main Features

- Frequency range: 35-42.5GHz
- 36dBm Pout for +20dBm input power
- Linear Gain > 25dB
- DC bias: Vd=25V@Idq=300mA
- 24L-QFN plastic package 4x4mm^2
- MSL3

Main Electrical Characteristics

Tcase = +25°C (Tcase: QFN backside temperature)

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	35.0		42.5	GHz
Gain	Linear Gain		25		dB
P_{MAX}	Maximum Output Power at PAE_{MAX}		36		dBm

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Specifications

Tcase = +25°C, Vd = +25V (QFN reference plans)

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	35.0		42.5	GHz
Gain	Linear Gain		25		dB
IRL(*)	Input Return Losses		10		dB
ORL(*)	Output Return Losses		10		dB
PAE_{MAX}	Maximum Power Added Efficiency		12		%
P_{MAX}	Output Power at PAE_{MAX}		36		dBm
Vd	CW Drain Voltage		25		V
Vg	CW Gate Voltage		-2.9		V
Idq	Quiescent Drain bias current		300		mA

These values are representative of measurements performed on evaluation board - see paragraph "Evaluation board".

(*) Input and Output Return Losses are given at RF reference plan of Evaluation board (see Definition of the Sii reference planes section).

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Absolute Maximum Ratings (1)

Tcase = +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	27	V
Idq	Quiescent Drain bias current	400	mA
Vg	Gate bias voltage	-7 to -2	V
Pin	Maximum Input Power	23	dBm

(1) Operation of this device above anyone of these parameters may cause permanent damage.

Recommended Operating Range (2), (3)

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	20 to 25	V
Id	Quiescent Drain bias current	140 to 300	mA
Vg	Gate bias voltage	-5 to-2.8	V
Pin	Maximum Input Power	21	dBm

(2) Electrical performances are defined for specified test conditions

(3) Electrical performances are not guaranteed over all recommended operating conditions

Temperature Range

Tcase	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +150	°C

Typical Bias Conditions

Tcase=+25°C

Symbol	Pad N°	Parameter	Values	Unit
VG12N	1	North 1st Gate bias voltage	-2.9	V
VG3N	23	North 2nd Gate bias voltage	-2.9	V
VG4N	22	North 3th Gate bias voltage	-2.9	V
VD12N	21	North 1st Drain bias voltage	25	V
VD3N	20	North 2nd Drain bias voltage	25	V
VD4N	18	North 3th Drain bias voltage	25	V
VG12S	7	South 1st Gate bias voltage	-2.9	V
VG3S	8	South 2nd Gate bias voltage	-2.9	V
VG4S	9	South 3th Gate bias voltage	-2.9	V
VD12S	10	South 1st Drain bias voltage	25	V
VD3S	11	South 2nd Drain bias voltage	25	V
VD4S	12	South 3th Drain bias voltage	25	V

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"Power ON" sequence

1. Bias HPA gate voltage Vg (VG12N, VG3N, VG4N, VG12S, VG3S, VG4S) close to Vpinch-off (Typically: Vg ≈ -5V)
2. Apply drain bias voltage Vd (VD12N, VD3N, VD4N, VD12S, VD3S, VD4S) (Typically: Vd = 25V)
3. Increase gate voltage Vg (VG12N, VG3N, VG4N, VG12S, VG3S, VG4S) up to quiescent bias drain current Idq
4. Apply RF signal

"Power OFF" sequence

1. Turn off RF signal
2. Bias HPA gate voltage Vg (VG12N, VG3N, VG4N, VG12S, VG3S, VG4S) close to Vpinch-off (Typically: Vg ≈ -5V)
3. Check that quiescent bias drain current Idq is close to 0mA
4. Turn drain bias voltage Vd (VD12N, VD3N, VD4N, VD12S, VD3S, VD4S) to 0V
5. Check that quiescent bias drain current Idq is close to 0mA
6. Turn gate voltage Vg (VG12N, VG3N, VG4N, VG12S, VG3S, VG4S) to 0V

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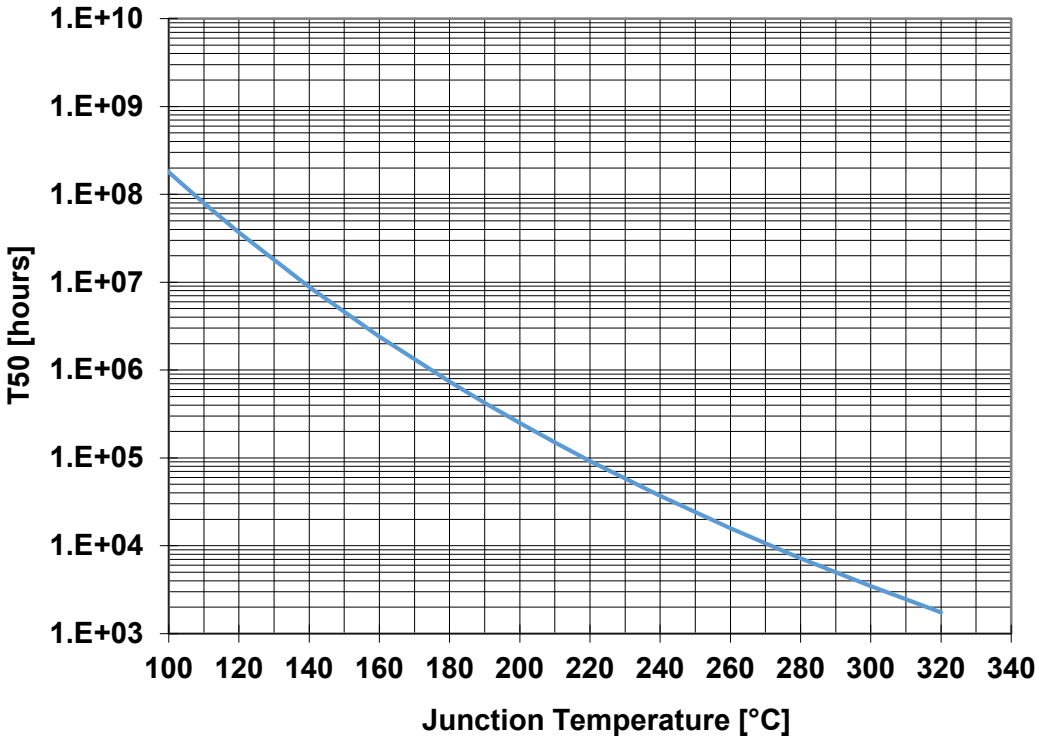
Device thermal performances

The temperature is monitored at the package back-side interface (Tcase).
The system maximum temperature must be adjusted in order to guarantee that Tjunction remains below the maximum value specified in the Absolute Maximum Ratings table.
The system PCB must be designed to comply with this requirement.

Parameter	DC & RF conditions	Tjunction (°C)	R_{TH} (°C/W)	T50 (hours)
R_{TH} [4] Thermal Resistance (Junction to Case)	Vd= 25V Id= 300mA Pout= 26dBm Pdiss= 12.7W	137	4.10	8.81E+06
	Vd= 25V Id= 300mA Pout= 33dBm Pdiss= 21.7W	200	5.30	2.50E+05

[4] Assuming 85°C Tcase



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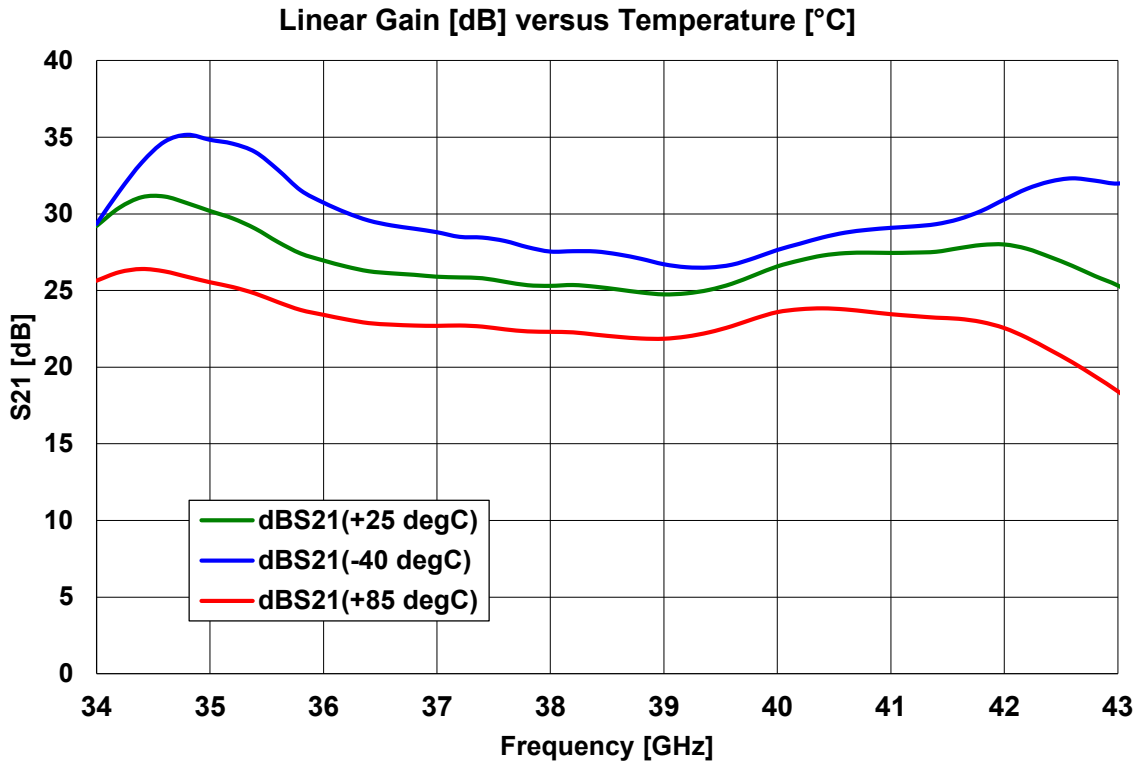
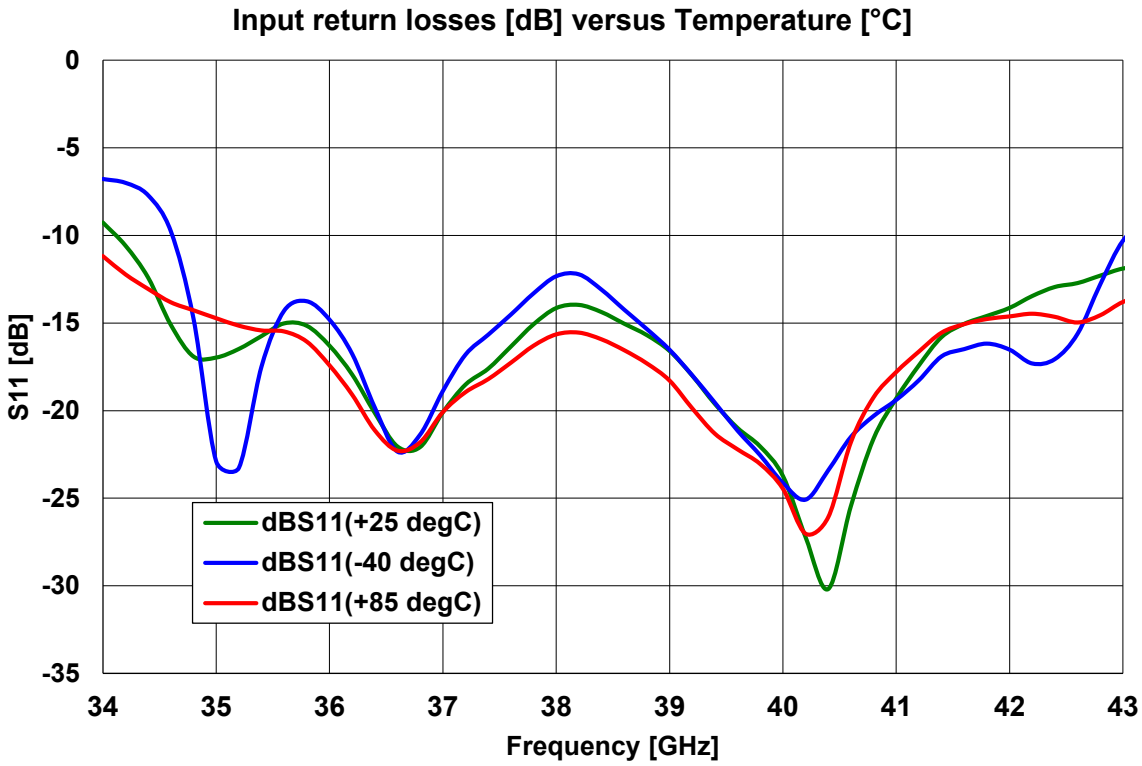
Typical on board Measurements: Small signal performance

Tcase=-40°C/+25°C/+85°C (QFN backside), Vd = +25V, Idq = 300mA





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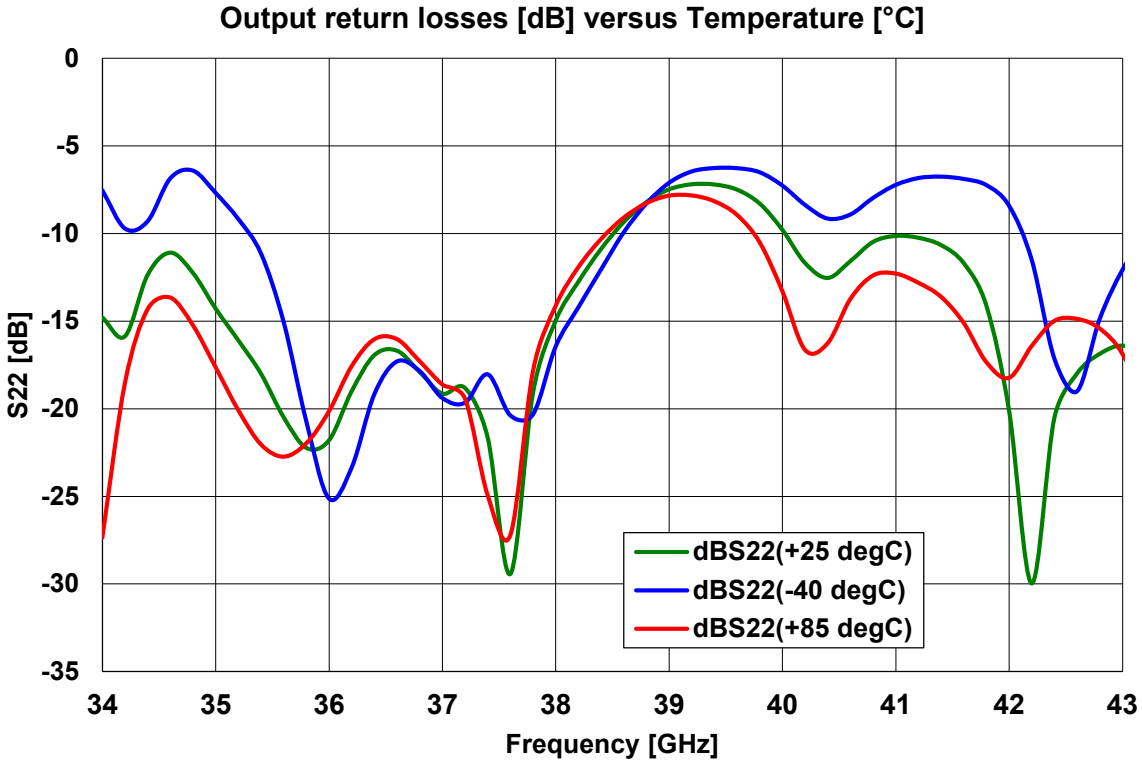
Typical on board Measurements: Small signal performance

Tcase=-40°C/+25°C/+85°C (QFN backside), Vd = +25V, Idq = 300mA



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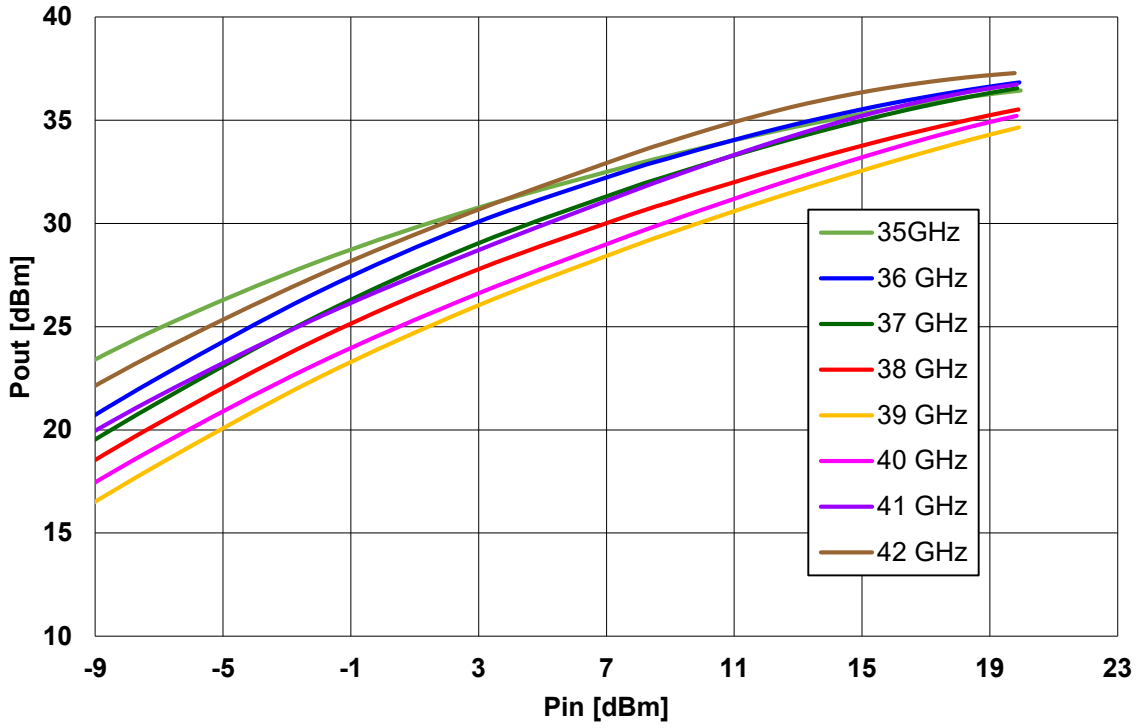
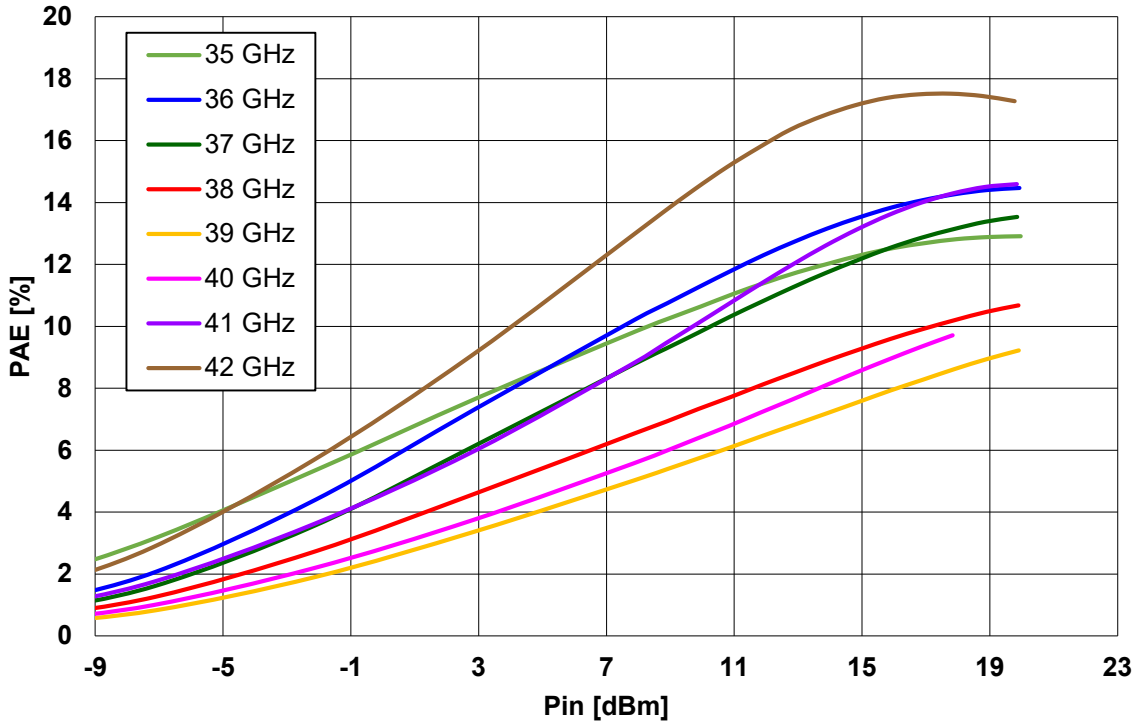
Typical on board Measurements: Large signal performance

Tcase=+25°C (QFN backside), Vd = +25V, Idq = 300mA

Output Power [dBm] versus Available Input Power [dBm](5)



Power Added Efficiency [%] versus Available Input Power [dB](5)



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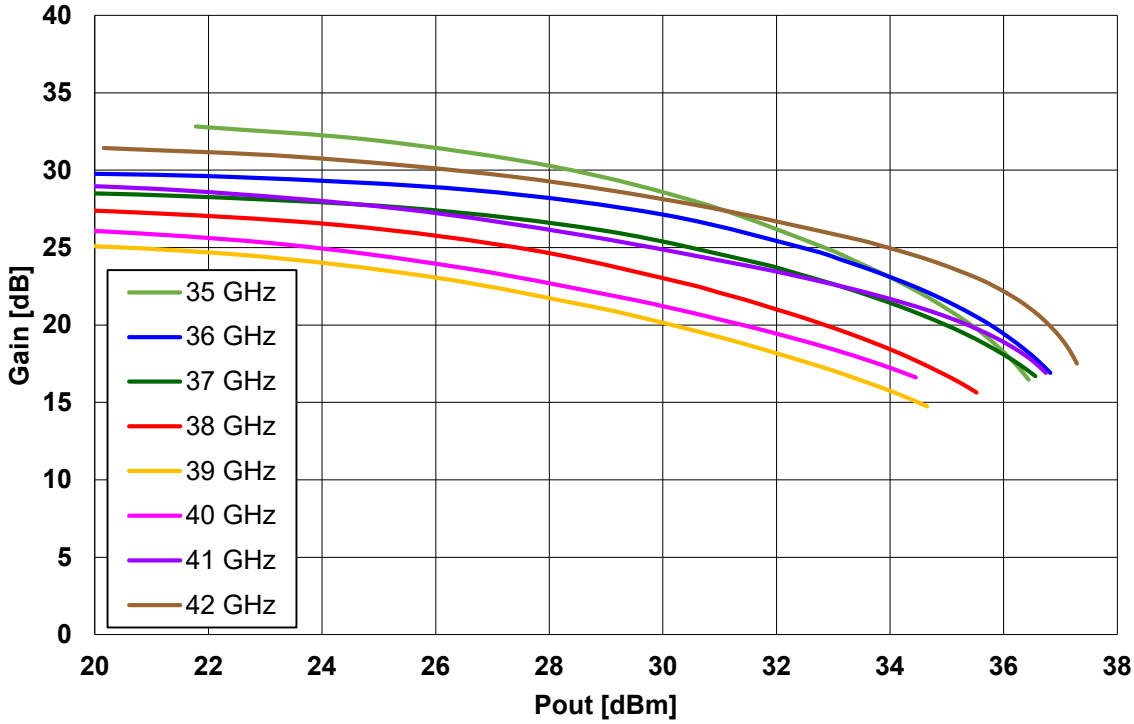
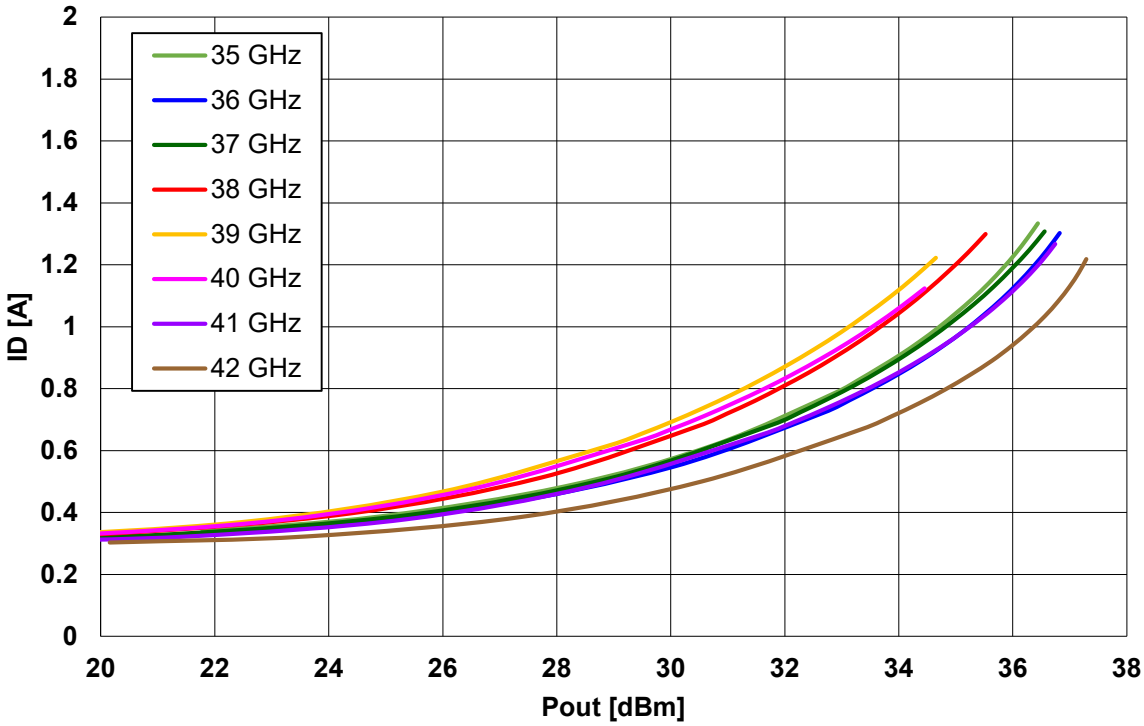
Typical on board Measurements: Large signal performance

Tcase=+25°C (QFN backside), Vd = +25V, Idq = 300mA

Gain [dB] versus Output Power [dBm][5]



Drain current [A] versus Output Power [dBm][5]



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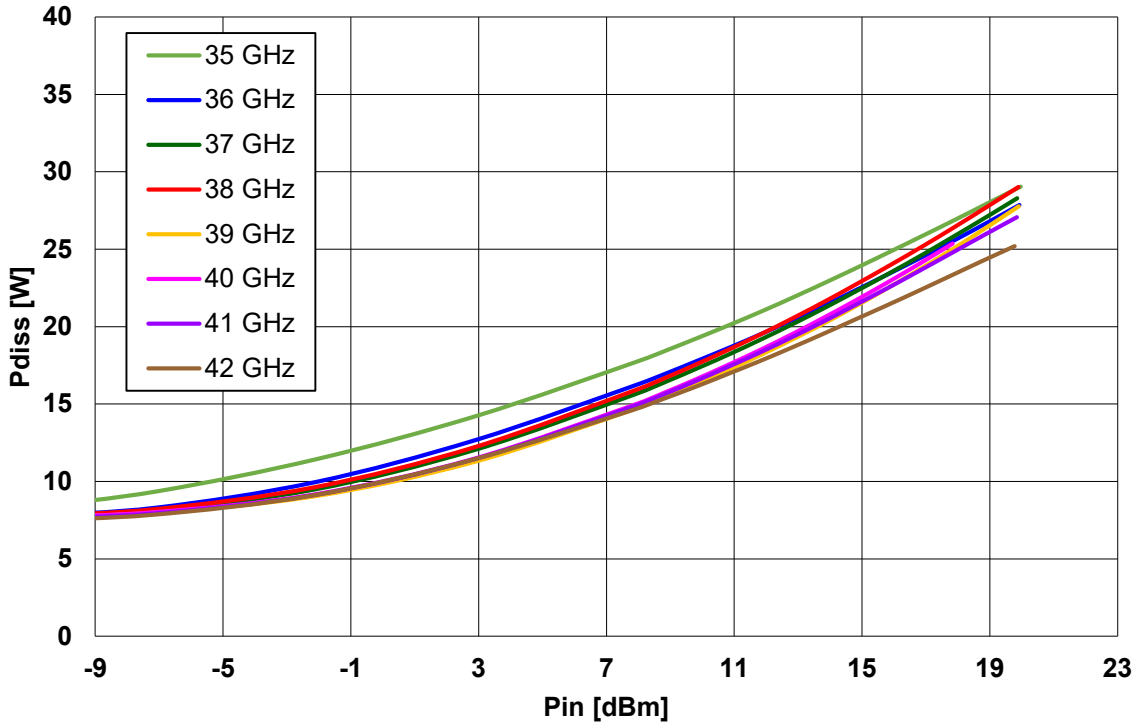
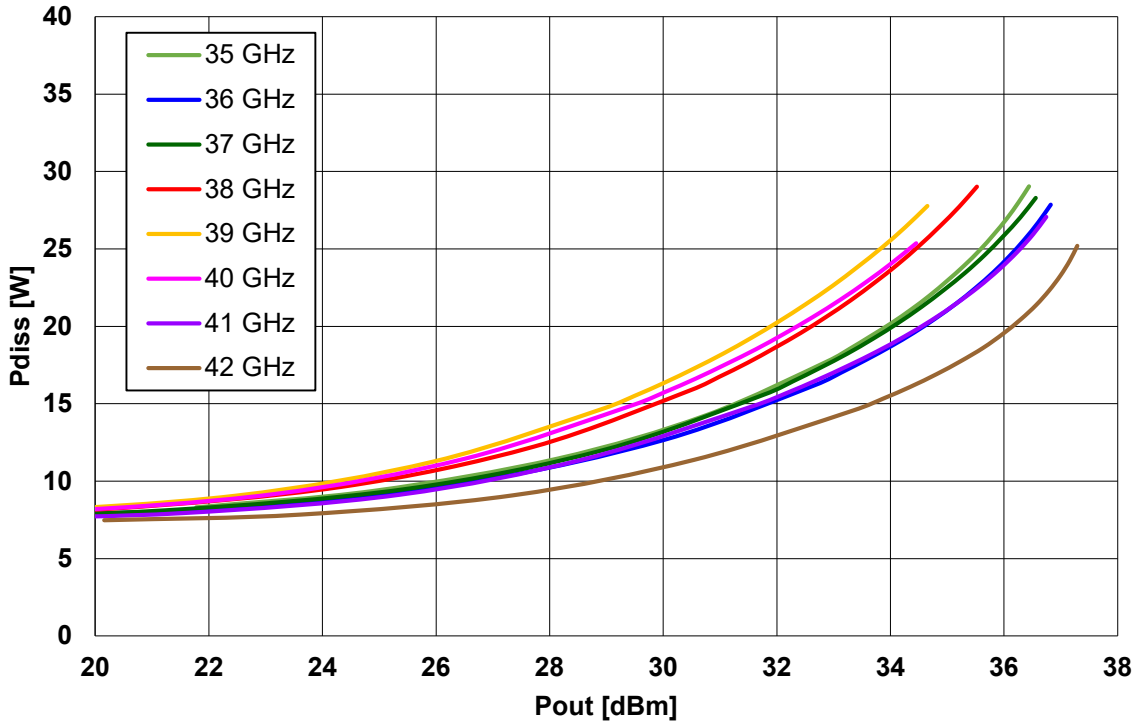
Typical on board Measurements: Large signal performance

Tcase=+25°C (QFN backside), Vd = +25V, Idq = 300mA

Dissipated power [W] versus Available Input Power [dBm](5)



Dissipated power [W] versus Output Power [dBm](5)



(5) The temperature is fixed at 25°C at the SMD QFN package for Pout = 36dBm.

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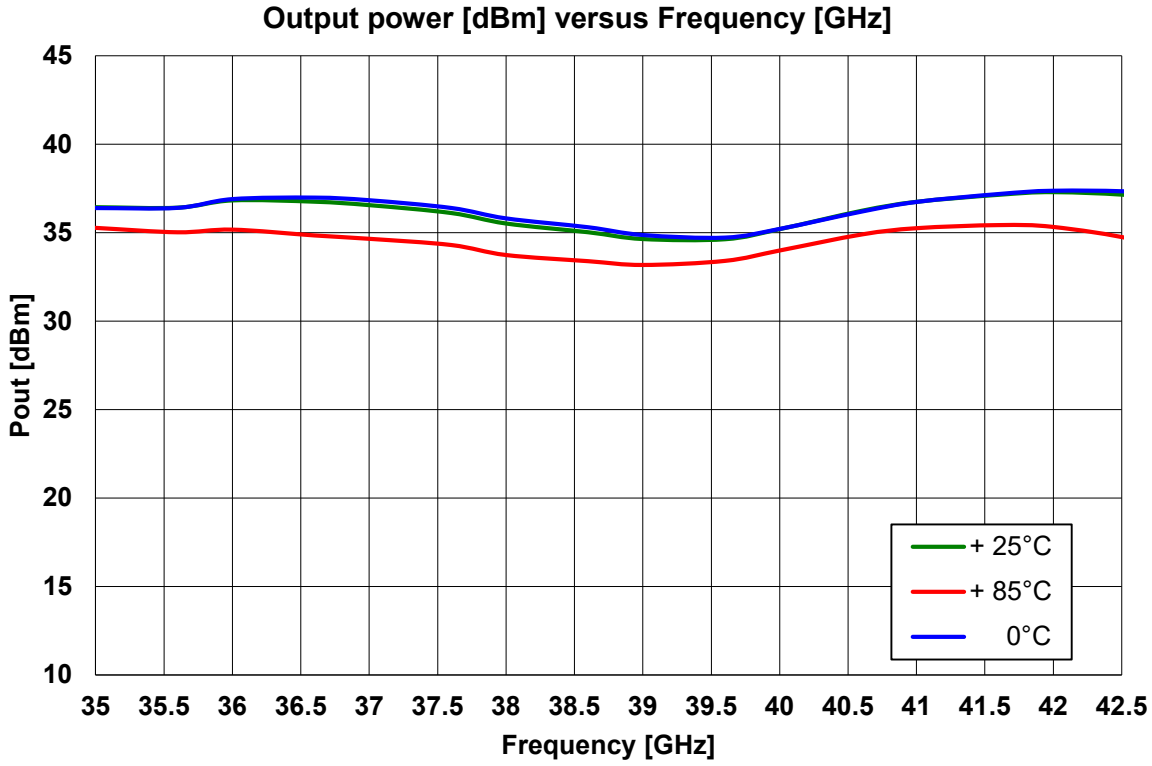
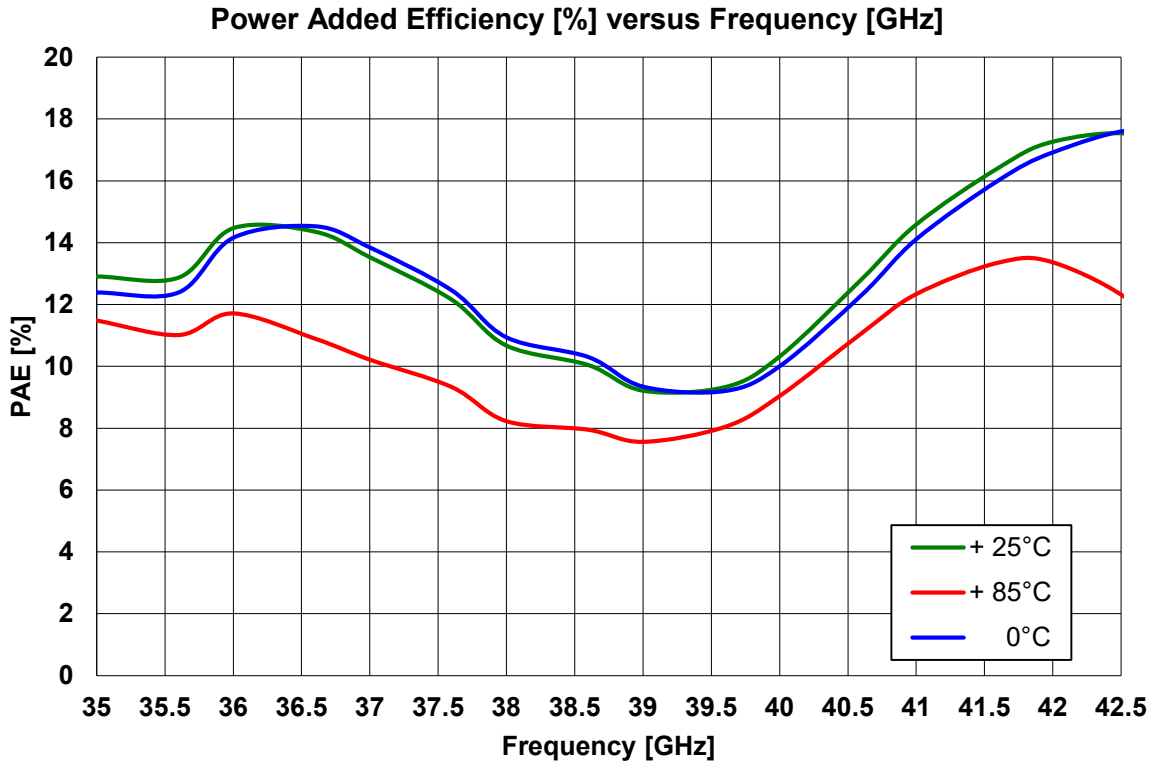
Typical on board Measurements: Large signal performance

Tcase= 0°C/+25°C/85°C (QFN backside), Vd = +25V, Idq = 300mA, Pin = 20dBm





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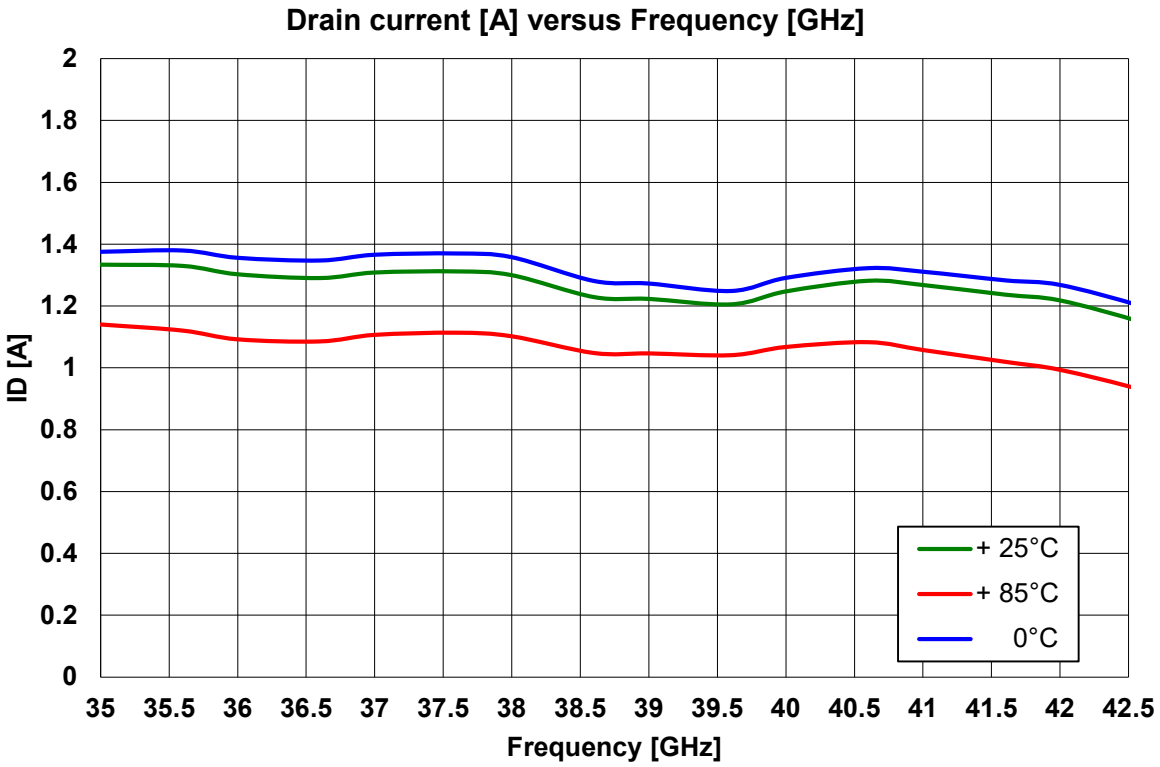
Typical on board Measurements: Large signal performance

Tcase= 0°C/+25°C/85°C (QFN backside), Vd = +25V, Id = 300mA, Pin= 20dBm



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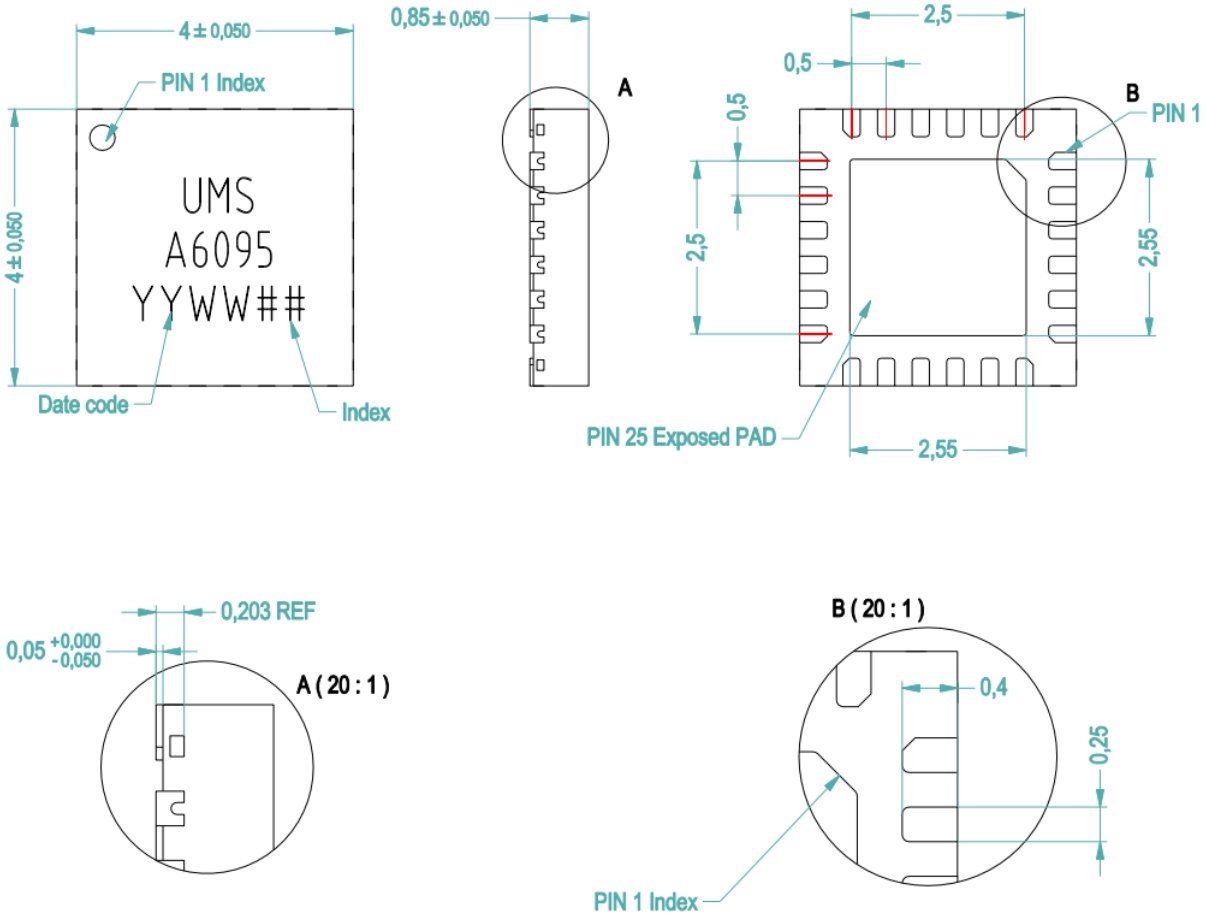
Package outline



Package pinout

Matte tin, Lead Free (Green)		1- VG12N	9- VG4S	17- NC
Units : mm		2- NC	10- VD12S	18- VD4N
From the standard : JEDEC MO-220		3- GND(6)	11- VD3S	19- GND(6)
(VGGD)		4- RF in	12- VD4S	20- VD3N
25- GND(6)		5- GND(6)	13- NC	21- VD12N
		6- NC	14- GND(6)	22- VG4N
		7- VG12S	15- RF out	23- VG3N
		8- VG3S	16- GND(6)	24- GND(6)

(6) It is strongly recommended to ground all pins marked “GND” through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package. See application note AN0017 for details.

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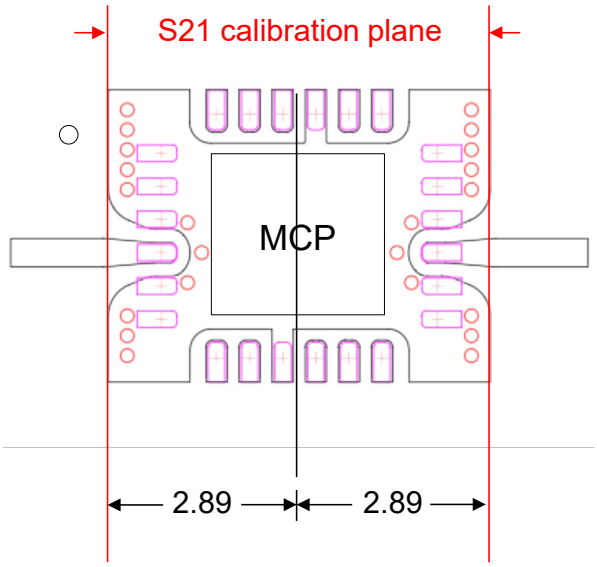
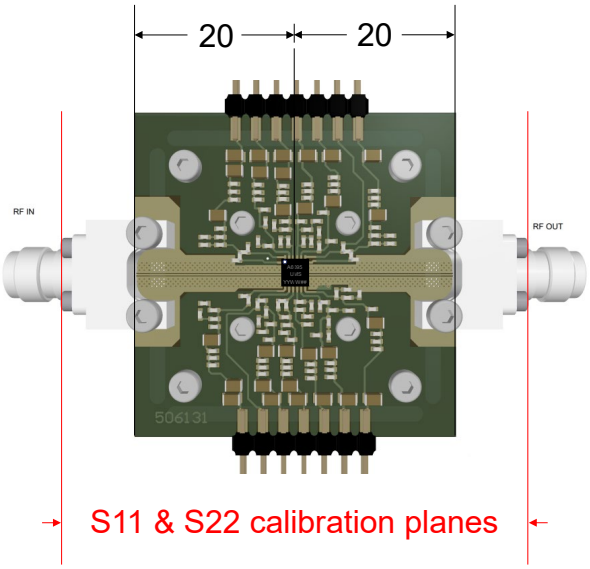
Definition of the Sij reference planes

The reference planes used for S21 measurements are symmetrical from the central axis of the package (see drawing beside). The input and output reference planes are located at 2.89mm offset from the central axis. The S21 parameter measurements include this given PCB pattern (see paragraph "Evaluation board").



Definition of the Sii reference planes

The reference planes used for S11 and S22 measurements are symmetrical from the central axis of the package (see drawing beside). The input and output reference planes are located at 20mm offset from the central axis. The S11 and S22 measurements include this given PCB patter, the RF lines of the evaluation board and the RF connectors.



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ESD sensitivity

ESD – Human Body Model (HBM)
Class 1A / 250V to < 500V

ESD – Machine Model (MM)
Class M1 / < 100V
Class M2 / 100V up to 200V

Package Information

Parameter	Value
Package body material	RoHS-compliant
	Low stress Injection Molded Plastic
Lead finish	100% matte tin (Sn)
MSL Rating	MSL3

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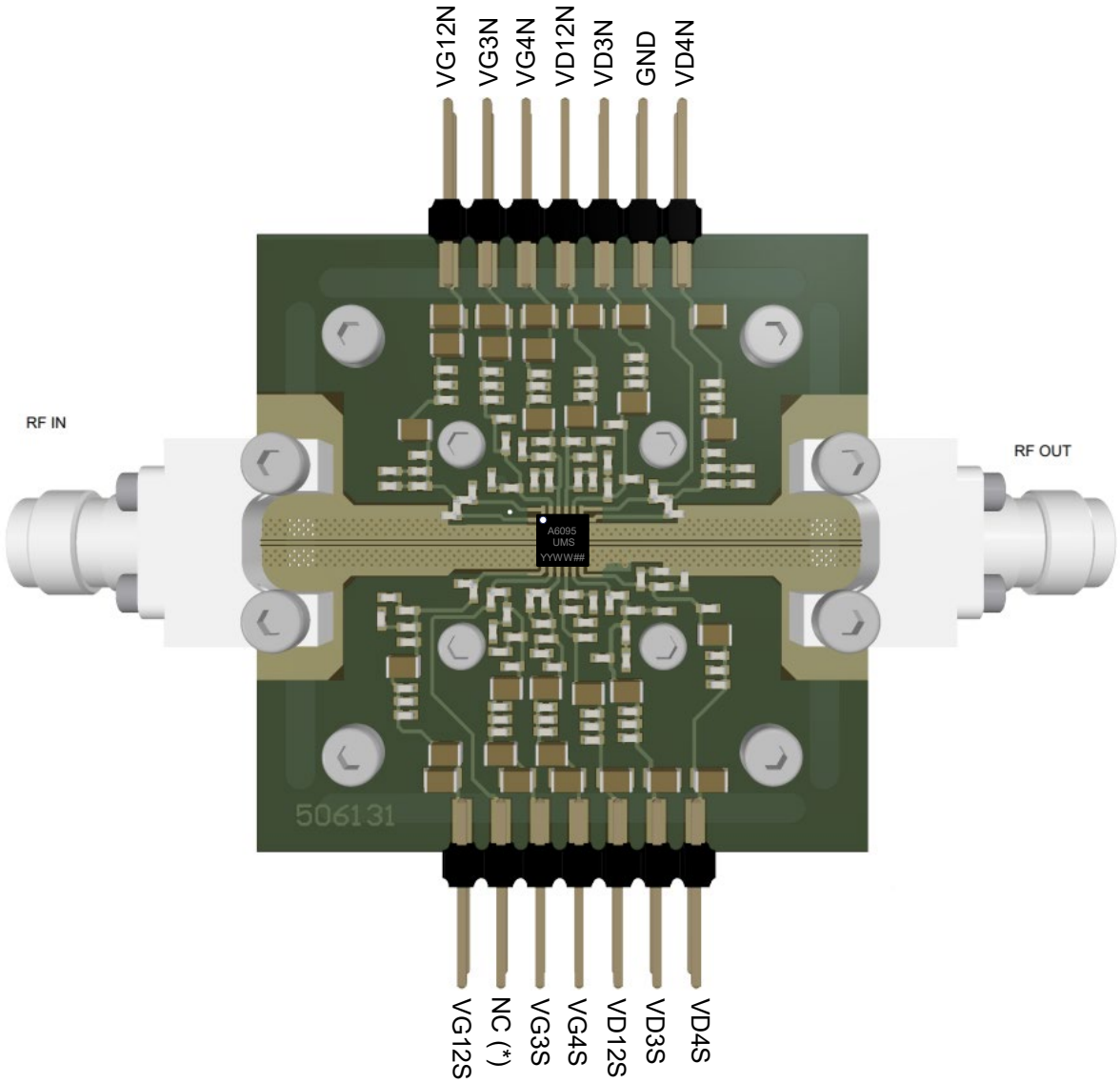
Evaluation board

- Compatible with the proposed footprint.
- Based on typically MT77 / 10mils or equivalent.
- Using a micro-strip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 100pF ±5%, 10nF ±10% and 1µF ±10% are recommended for all DC accesses.
- To ensure safe operation, all measurements must be performed using **shielded cables**, **even for DC bias**.



(*) Pins not connected.

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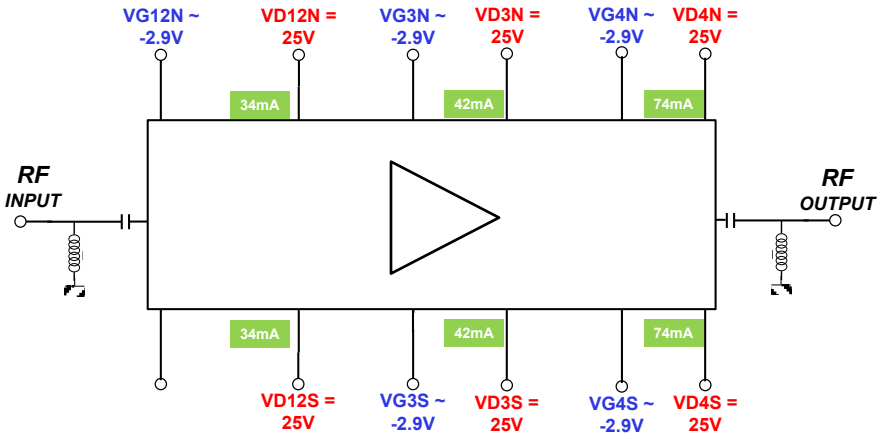
DC Schematic



The DC pins do not include any decoupling capacitor in package, therefore it is mandatory to provide a good external DC decoupling (100pF ±5%, 10nF ±10% and 1µF ±10%) on the PC board, as close as possible to the package.

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Recommended package footprint

Refer to the application note AN0017 available at https://www.ums-rf.com for package foot print recommendations.

SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017 at https://www.ums-rf.com.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at https://www.ums-rf.com.

Recommended ESD management

Refer to the application note AN0020 available at https://www.ums-rf.com for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

QFN 4x4 package:	CHA6095-QKB/XY	
	Stick: XY = 20	Tape & reel: XY = 21

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