

## 35-42.5GHz 2W Packaged Power Amplifier GaN Monolithic Microwave IC in SMD leadless package

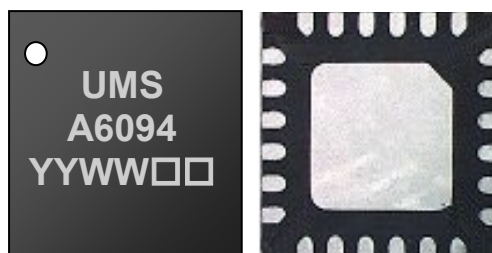
### Description

The CHA6094-QKB is a GaN packaged monolithic Power Amplifier operating in the 35-42.5GHz frequency range.

It typically exhibits 33dBm saturated output power with 26dB small signal gain. The overall power supply is of 25V/150mA.

It is designed for a wide range of applications, such as 5G applications, active phased array antennas, and telecom applications and systems.

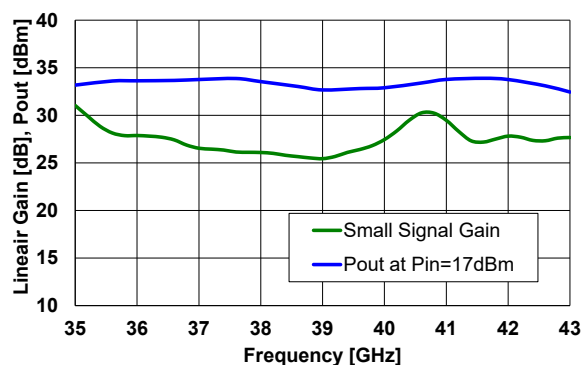
The circuit is available in a standard surface mount 24 leads QFN4x4 cost effective plastic package, compliant with the standards such as the directives RoHS N°2011/65 and REACH N°1907/2006. The input and output are internally matched to 50Ω and integrate ESD RF protection.



Small Signal Gain [dB] and Output Power [dBm] at Pin=17dBm, T°=25°C versus Frequency [GHz]

### Main Features

- Frequency range: 35-42.5GHz
- 33dBm Pout for +17dBm input power
- Linear Gain : 26dB
- DC bias: Vd=25V@Idq=150mA
- 24L-QFN plastic package 4x4mm<sup>2</sup>
- MSL3



### Main Electrical Characteristics

Tcase = +25°C (Tcase: QFN backside temperature)

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	35.0		42.5	GHz
Gain	Linear Gain		26		dB
P <sub>MAX</sub>	Maximum Output Power at PAE <sub>MAX</sub>		33		dBm

## Specifications

Tcase = +25°C, Vd = +25V (QFN reference plans)

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	35.0		42.5	GHz
Gain	Linear Gain		26		dB
IRL <sup>(*)</sup>	Input Return Losses		10		dB
ORL <sup>(*)</sup>	Output Return Losses		10		dB
PAE <sub>MAX</sub>	Maximum Power Added Efficiency		13		%
P <sub>MAX</sub>	Output Power at PAE <sub>MAX</sub>		33		dBm
Vd	CW Drain Voltage		25		V
Vg	CW Gate Voltage		-2.9		V
Idq	Quiescent Drain bias current		150		mA

These values are representative of measurements performed on evaluation board - see paragraph "Evaluation board".

(\*) Input and Output Return Losses are given at RF reference plan of Evaluation board (see Definition of the Sii reference planes section).

**Absolute Maximum Ratings** <sup>(1)</sup>T<sub>case</sub> = +25°C

Symbol	Parameter	Values	Unit
V <sub>d</sub>	Drain bias voltage	27	V
I <sub>dq</sub>	Quiescent Drain bias current	250	mA
V <sub>g</sub>	Gate bias voltage	-7 to -2	V
P <sub>in</sub>	Maximum Input Power	21	dBm

<sup>(1)</sup> Operation of this device above anyone of these parameters may cause permanent damage.

**Recommended Operating Range** <sup>(2), (3)</sup>

Symbol	Parameter	Values	Unit
V <sub>d</sub>	Drain bias voltage	20 to 25	V
I <sub>d</sub>	Quiescent Drain bias current	0 to 200	mA
V <sub>g</sub>	Gate bias voltage	-5 to -2.8	V
P <sub>in</sub>	Maximum Input Power	19	dBm

<sup>(2)</sup> Electrical performances are defined for specified test conditions

<sup>(3)</sup> Electrical performances are not guaranteed over all recommended operating conditions

**Temperature Range**

T <sub>case</sub>	Operating temperature range	-40 to +85	°C
T <sub>stg</sub>	Storage temperature range	-55 to +150	°C

**Typical Bias Conditions**T<sub>case</sub>=+25°C

Symbol	Pad N°	Parameter	Values	Unit
VG12	24	1 <sup>st</sup> Gate bias voltage	-2.9	V
VG3	23	2 <sup>nd</sup> Gate bias voltage	-2.9	V
VG4	22	3 <sup>th</sup> Gate bias voltage	-2.9	V
VD12	21	1 <sup>st</sup> Drain bias voltage	25	V
VD3N <sup>(*)</sup>	20	North 2 <sup>nd</sup> Drain bias voltage	25	V
VD4N <sup>(*)</sup>	19	North 3 <sup>th</sup> Drain bias voltage	25	V
VD3S <sup>(*)</sup>	10	South 2 <sup>nd</sup> Drain bias voltage	25	V
VD4S <sup>(*)</sup>	12	South 3 <sup>th</sup> Drain bias voltage	25	V

<sup>(\*)</sup> It is possible to apply biasing on one side only (North or South) or on both sides (North and South)

## “Power ON” sequence

1. Bias HPA gate voltage  $V_g$  (VG12, VG3, VG4) close to  $V_{\text{pinch-off}}$  (Typically:  $V_g \approx -5\text{V}$ )
2. Apply drain bias voltage  $V_d$  (VD12, VD3N, VD4N, VD3S, VD4S) (Typically:  $V_d = 25\text{V}$ )
3. Increase gate voltage  $V_g$  (VG12, VG3, VG4) up to quiescent bias drain current  $I_{dq}$
4. Apply RF signal

## “Power OFF” sequence

1. Turn off RF signal
2. Bias HPA gate voltage  $V_g$  (VG12, VG3, VG4) close to  $V_{\text{pinch-off}}$  (Typically:  $V_g \approx -5\text{V}$ )
3. Check that quiescent bias drain current  $I_{dq}$  is close to  $0\text{mA}$
4. Turn drain bias voltage  $V_d$  (VD12, VD3N, VD4N, VD3S, VD4S) to  $0\text{V}$
5. Check that quiescent bias drain current  $I_{dq}$  is close to  $0\text{mA}$
6. Turn gate voltage  $V_g$  (VG12, VG3, VG4) to  $0\text{V}$

**Device thermal performances**

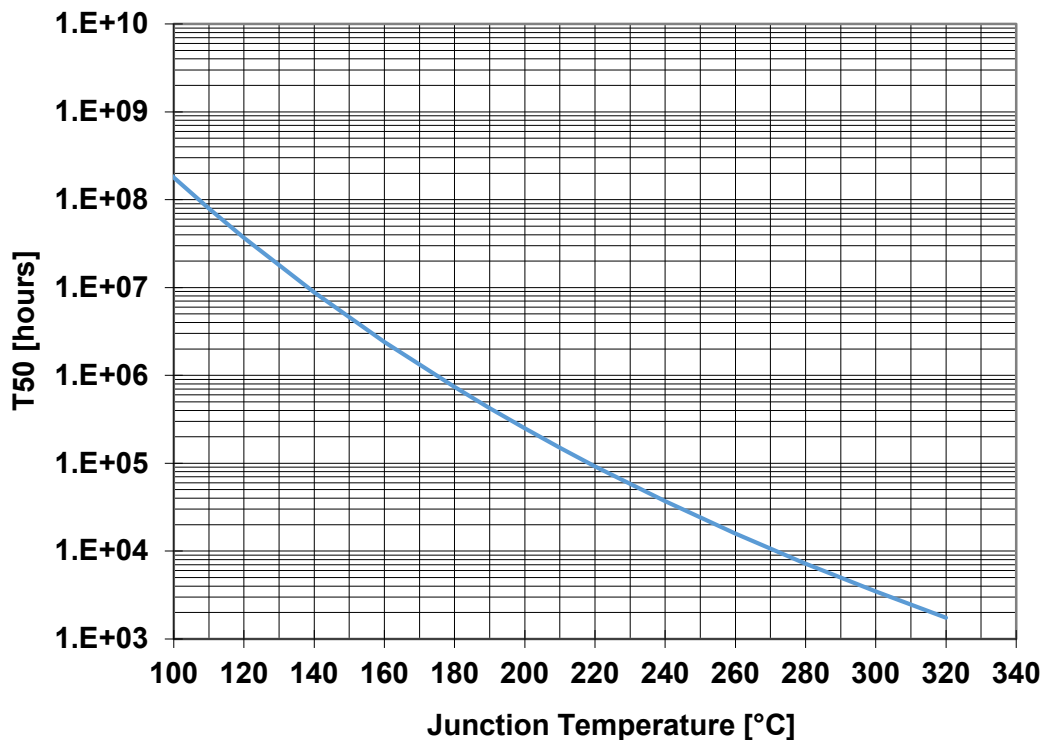
The temperature is monitored at the package back-side interface (Tcase).

The system maximum temperature must be adjusted in order to guarantee that Tjunction remains below the maximum value specified in the Absolute Maximum Ratings table.

The system PCB must be designed to comply with this requirement.

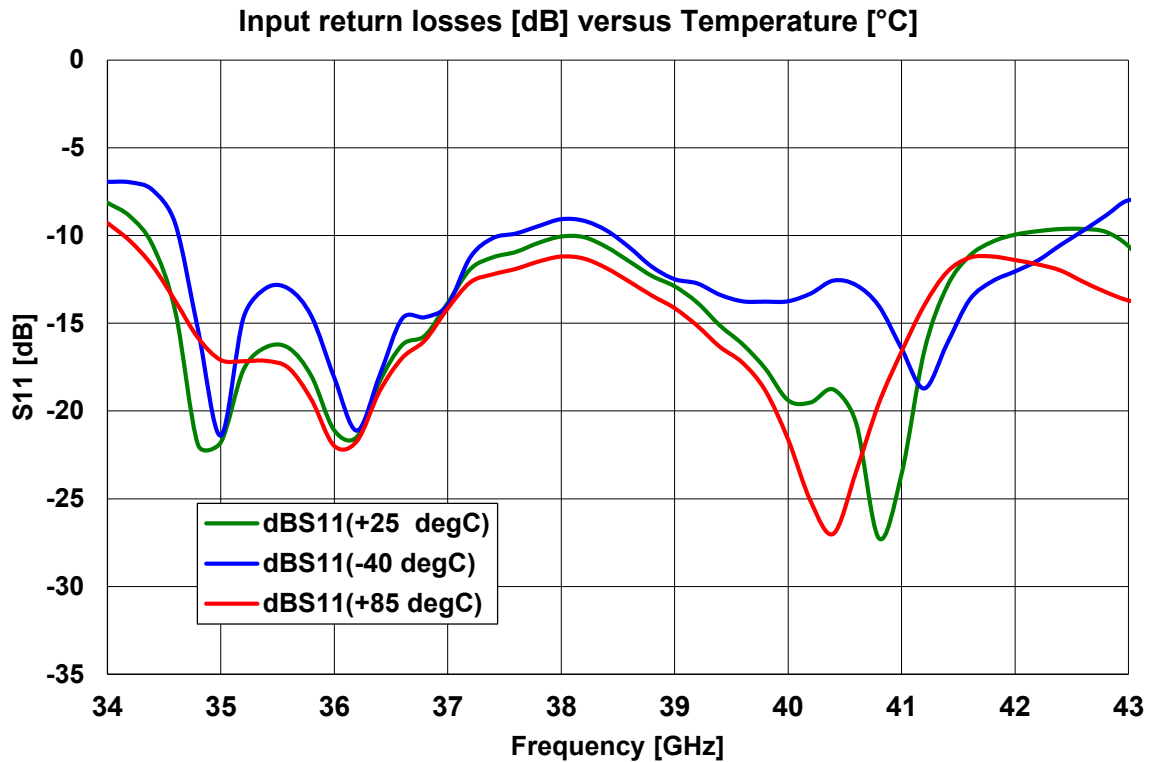
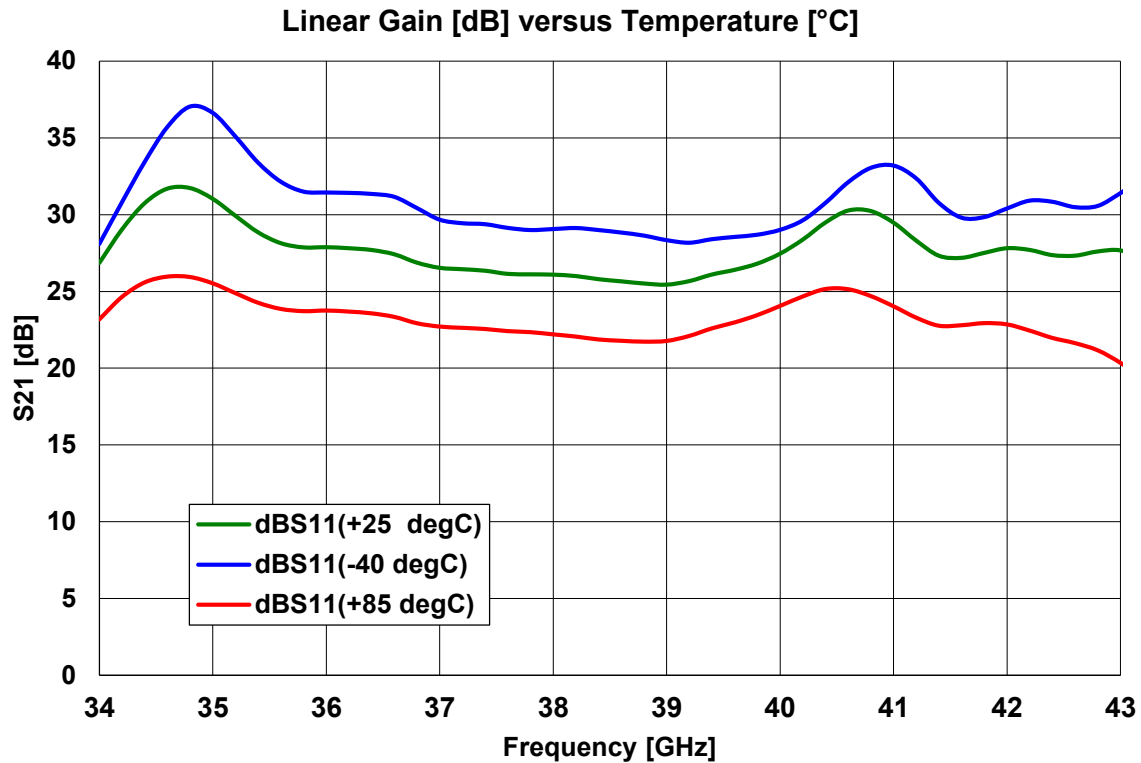
Parameter	DC & RF conditions	Tjunction (°C)	RTH (°C/W)	T50 (hours)
RTH <sup>(4)</sup> Thermal Resistance (Junction to Case)	Vd= 25V Id= 150mA Pout= 23dBm Pdiss= 6 W	135	8.21	8.81E+06
	Vd= 25V Id= 150mA Pout= 31.5dBm Pdiss= 10.8W	200	10.64	2.50E+05

<sup>(4)</sup> Assuming 85°C Tcase



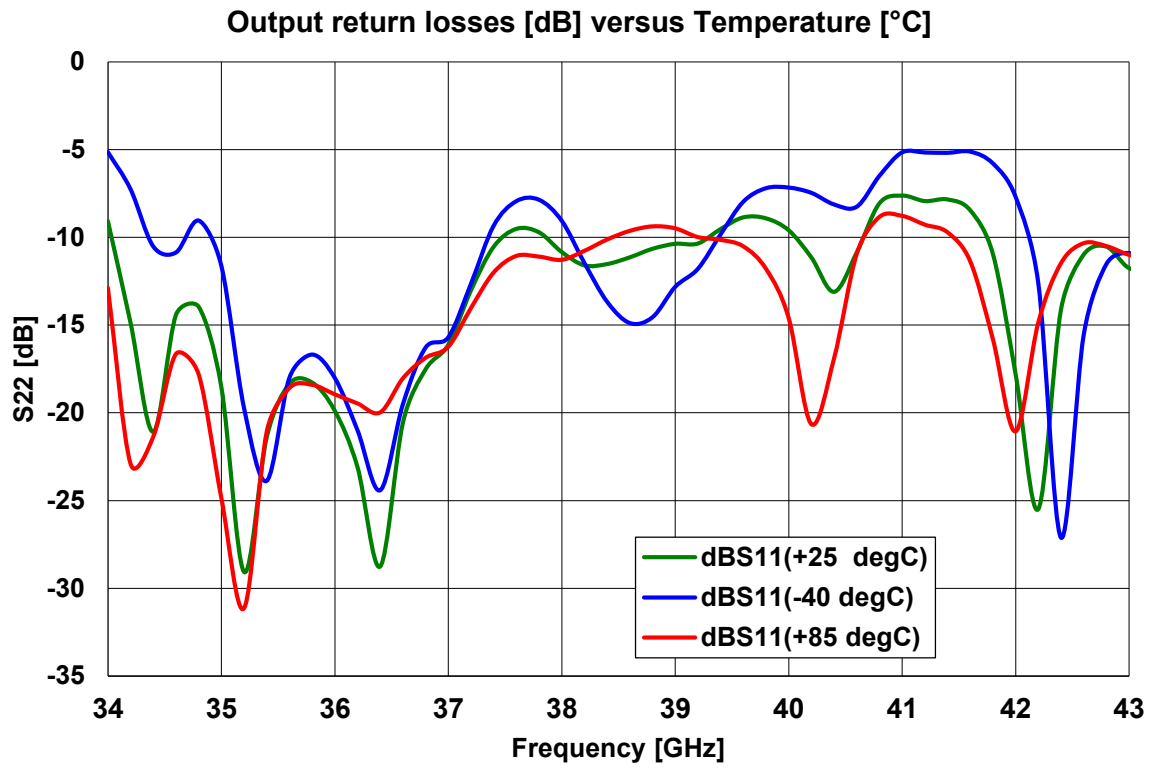
## Typical on board Measurements: Small signal performance

Tcase=-40°C/+25°C/+85°C (QFN backside), Vd = +25V, Idq = 150mA



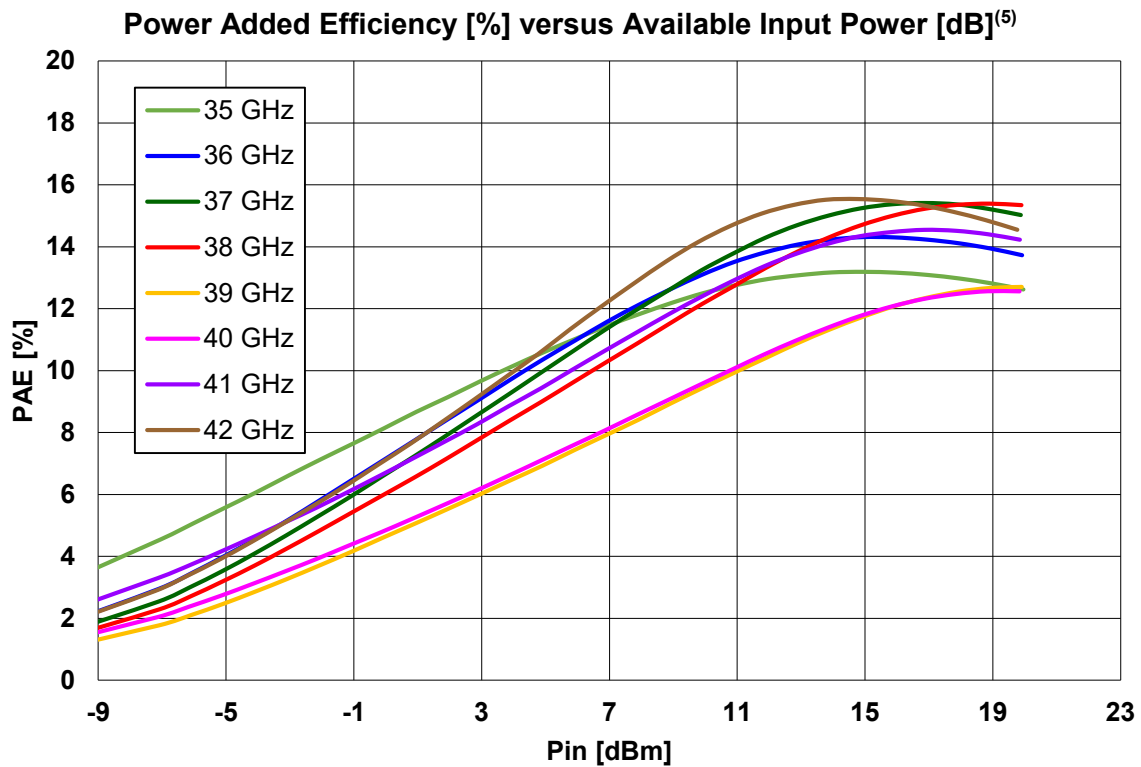
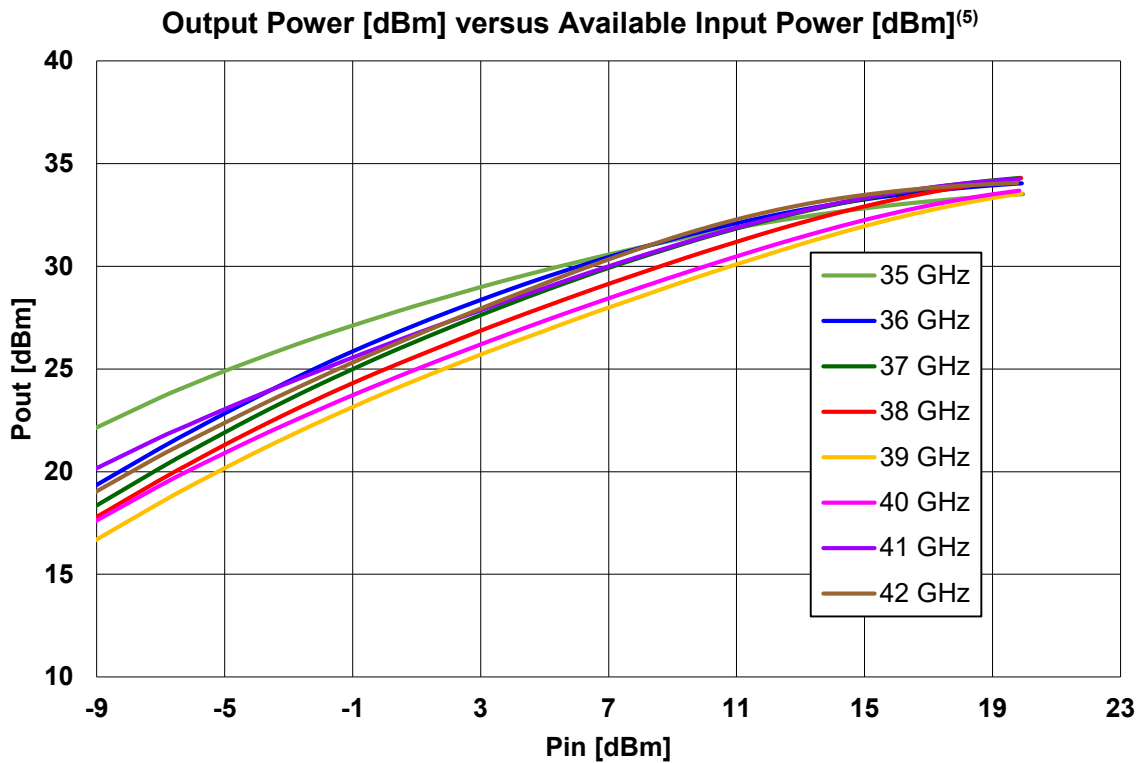
**Typical on board Measurements: Small signal performance**

Tcase=-40°C/+25°C/+85°C (QFN backside), Vd = +25V, Idq = 150mA



### Typical on board Measurements: Large signal performance

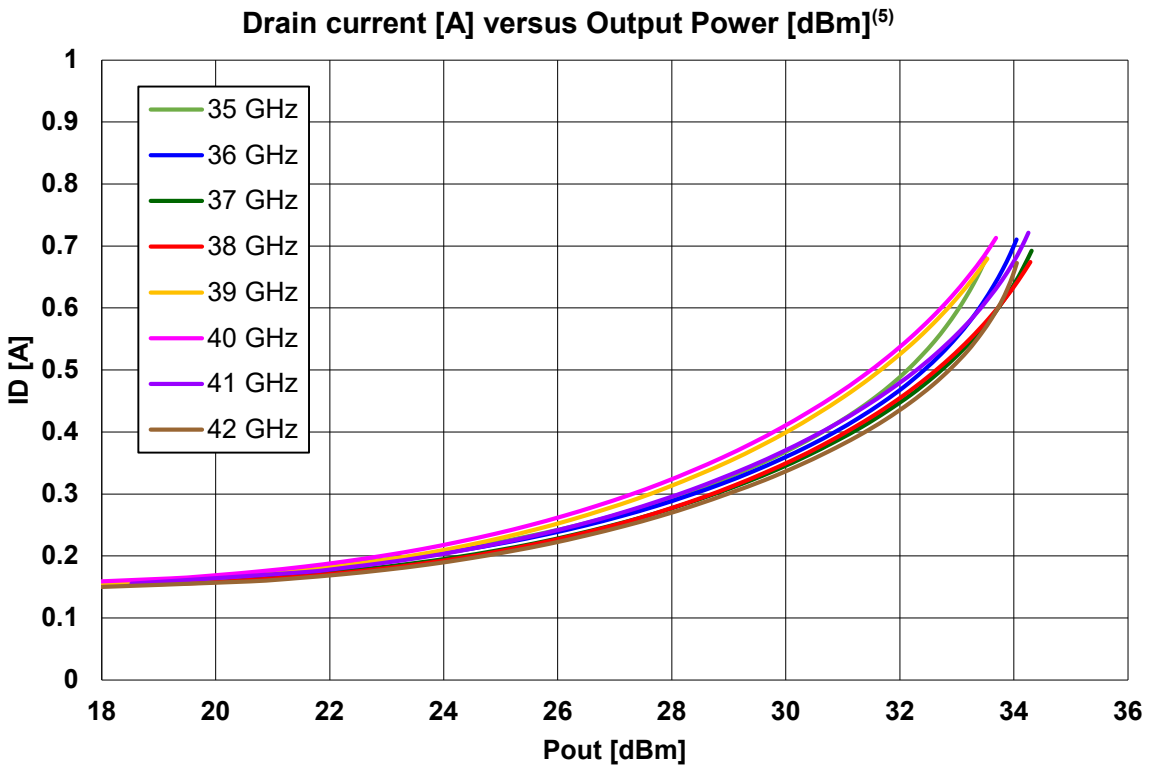
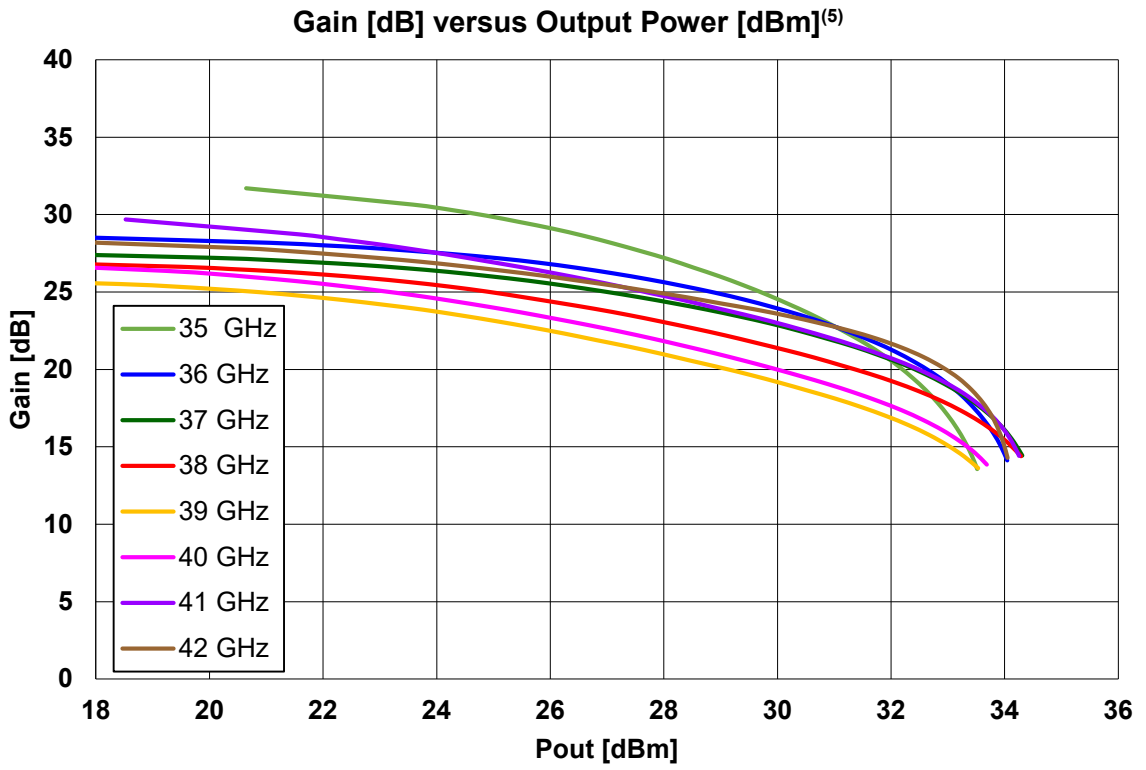
Tcase=+25°C (QFN backside), Vd = +25V, Idq = 150mA





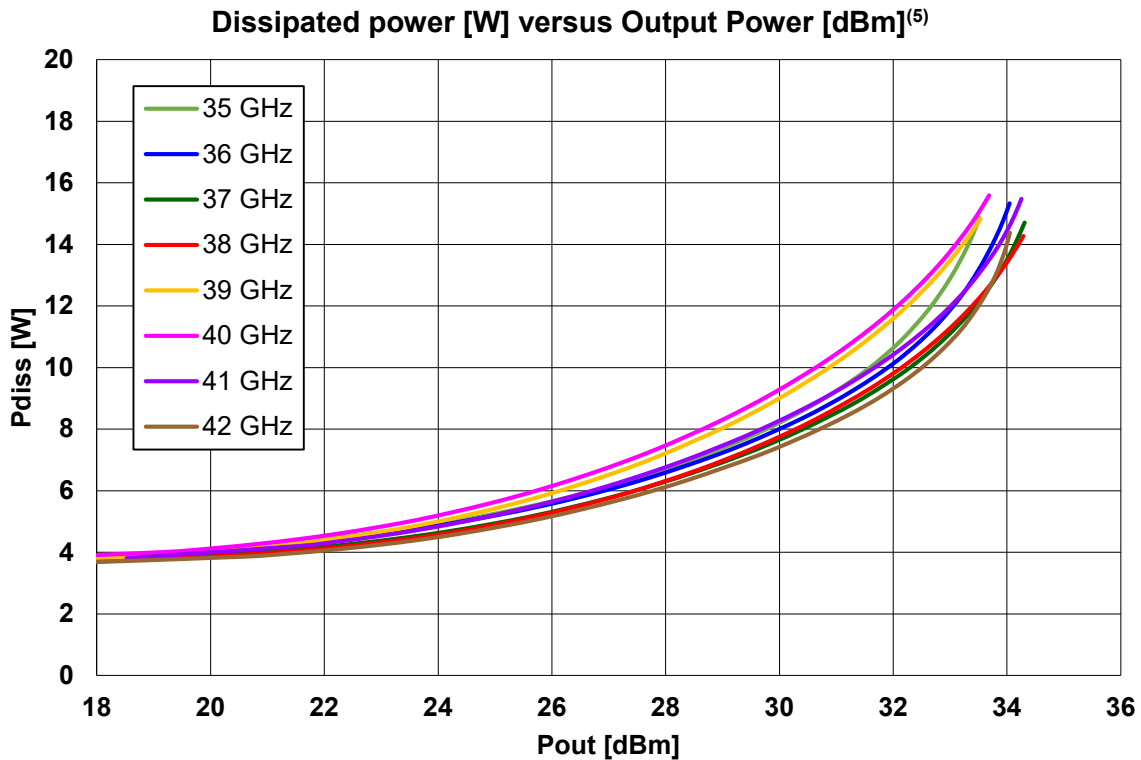
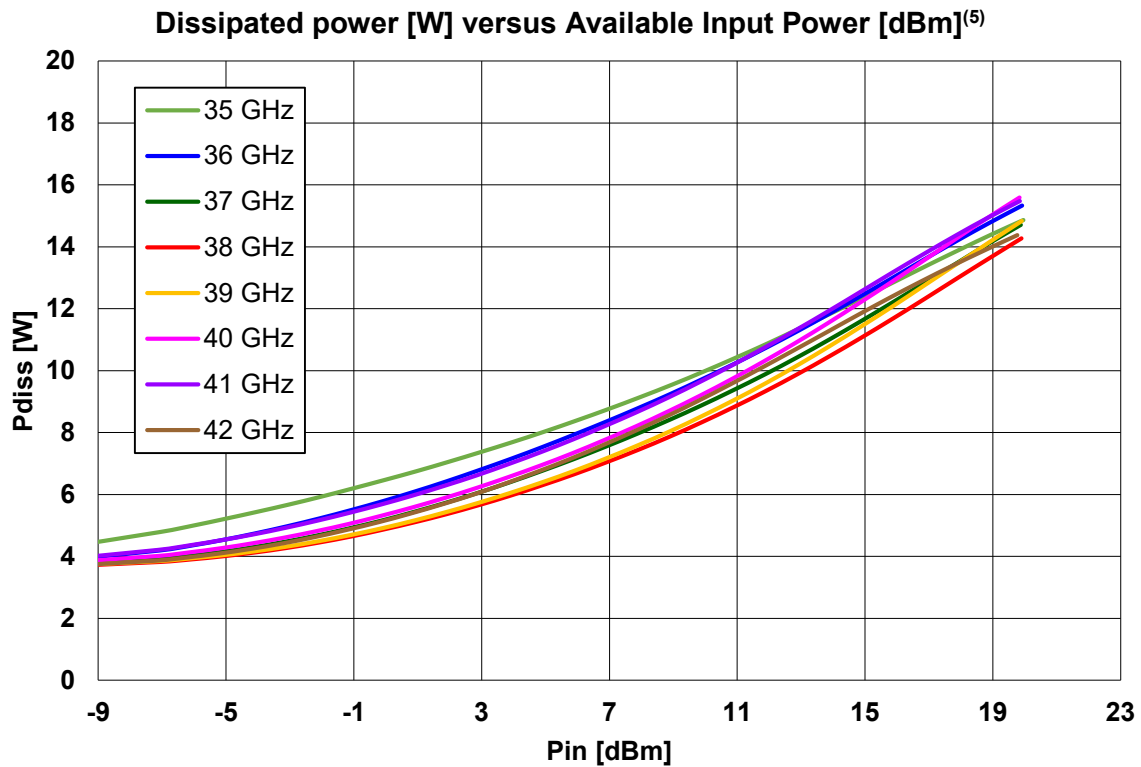
**Typical on board Measurements: Large signal performance**

T<sub>case</sub>=+25°C (QFN backside), V<sub>d</sub> = +25V, I<sub>dq</sub> = 150mA



### Typical on board Measurements: Large signal performance

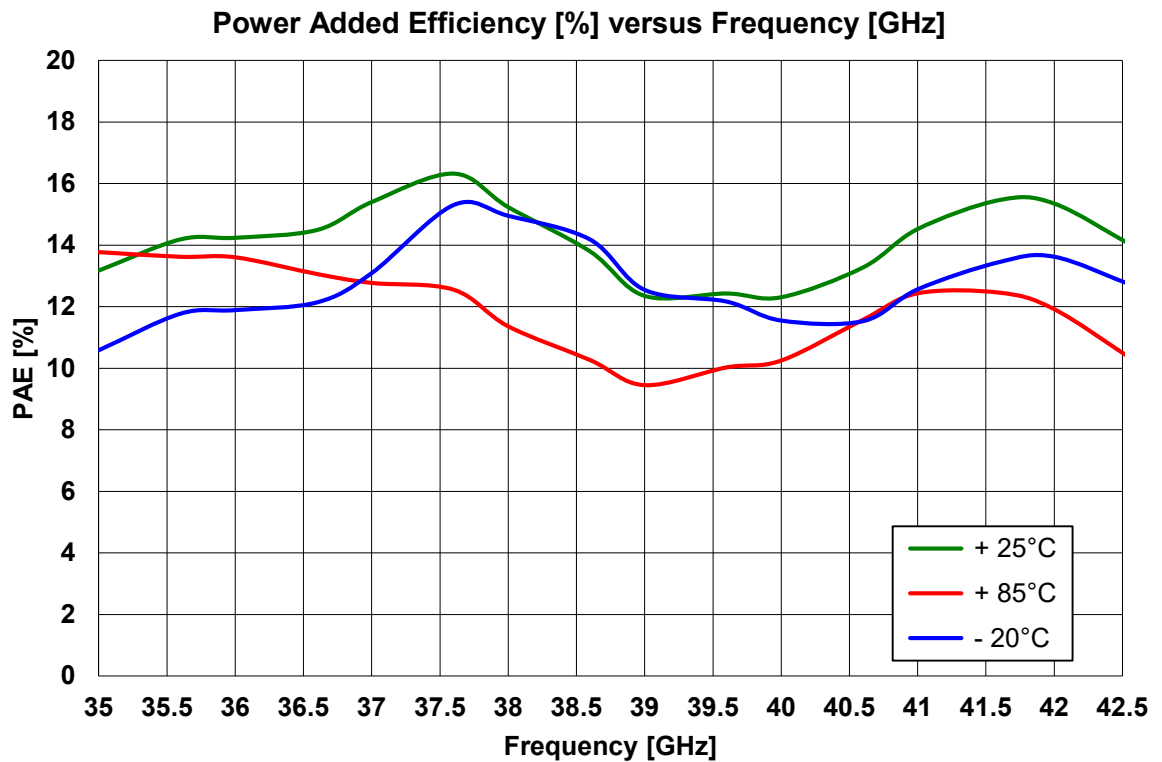
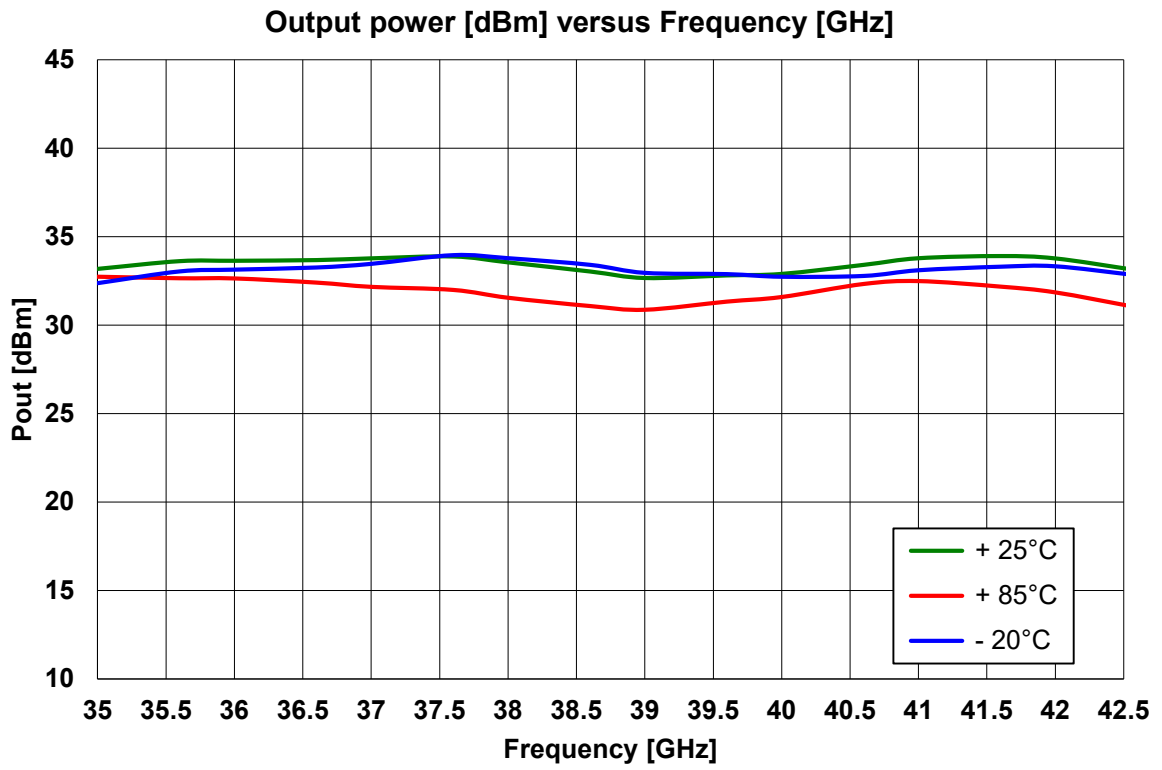
Tcase=+25°C (QFN backside), Vd = +25V, Idq = 150mA



<sup>(5)</sup> The temperature is fixed at 25°C at the QFN package for Pout = 33dBm.

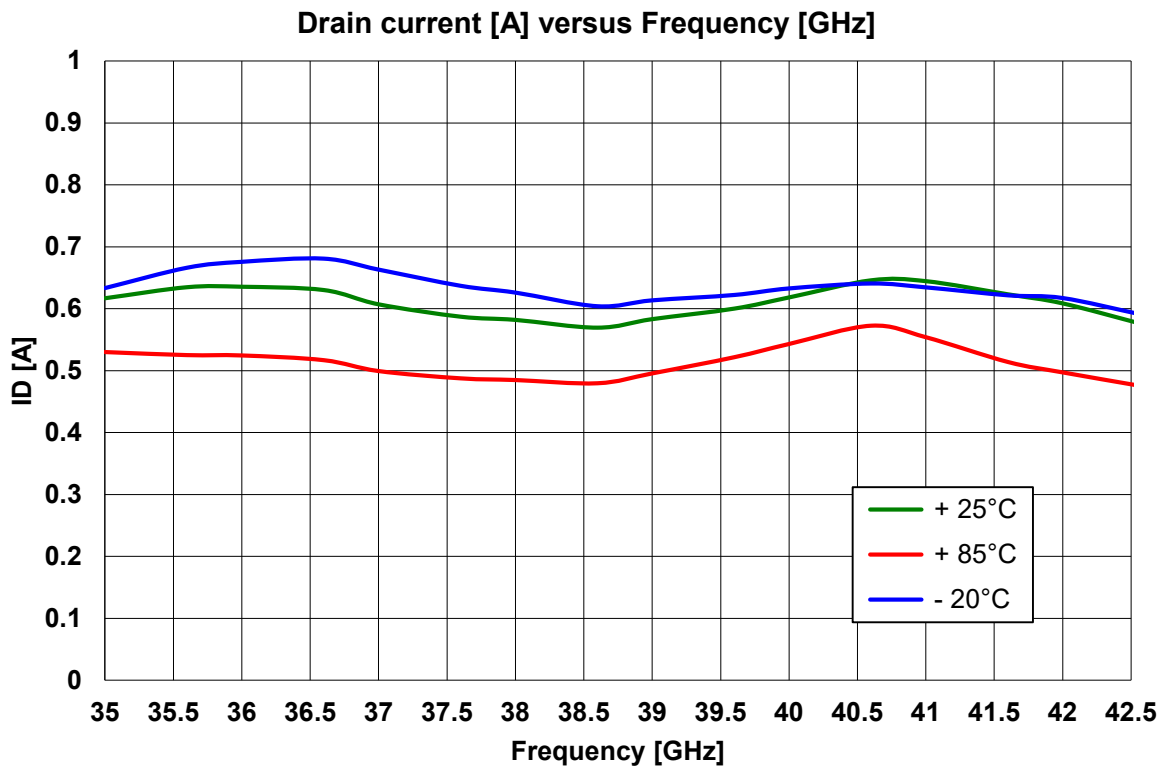
**Typical on board Measurements: Large signal performance**

Tcase= -20°C/+25°C/85°C (QFN backside), Vd = +25V, Idq = 150mA, Pin= 17dBm

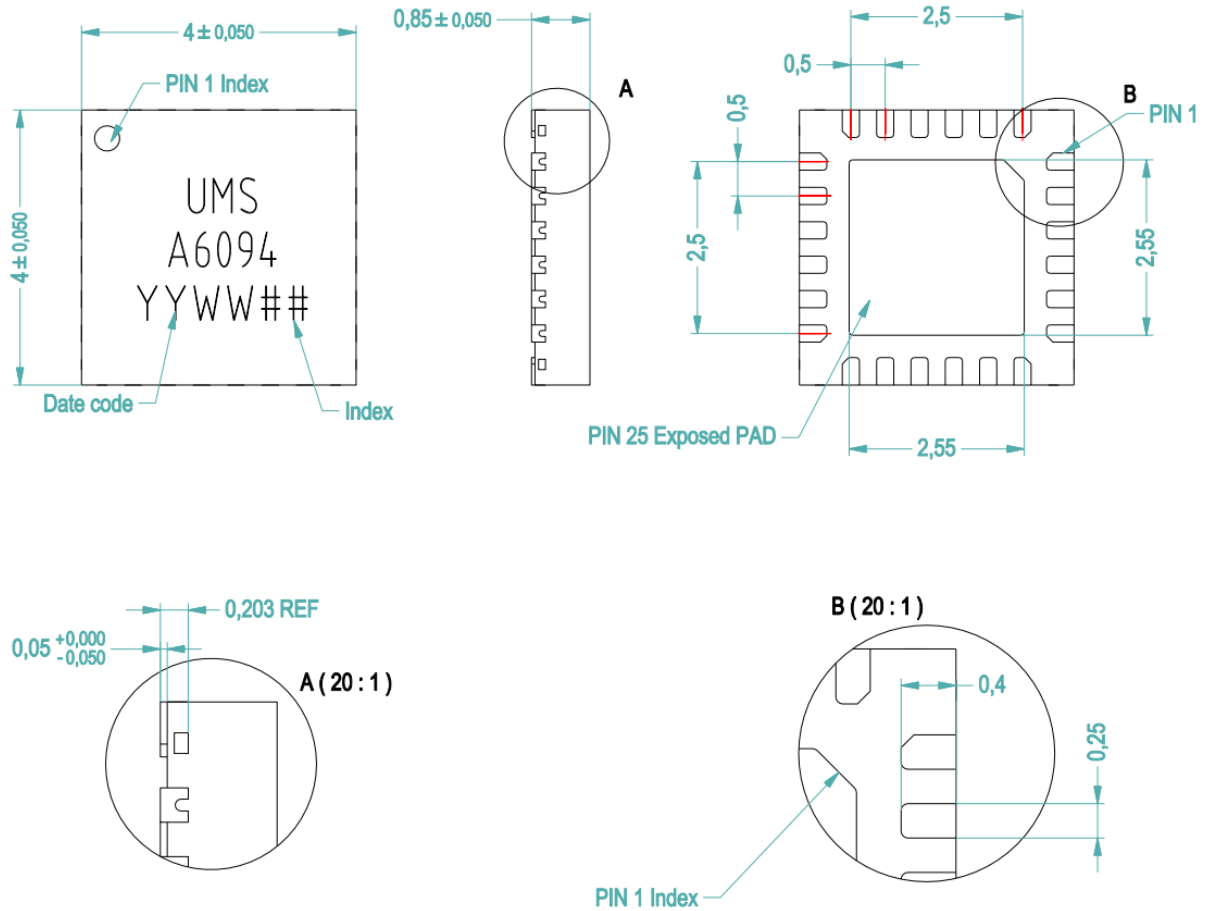


### Typical on board Measurements: Large signal performance

Tcase= -20°C/+25°C/85°C (QFN backside), Vd = +25V, Id = 150mA, Pin= 17dBm



**Package outline**



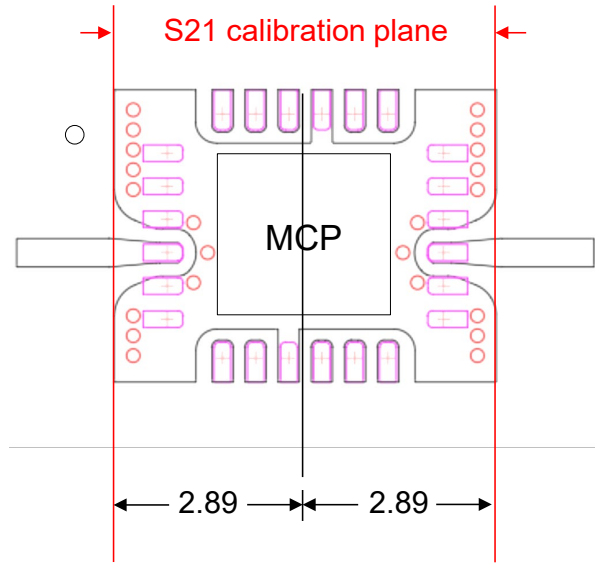
**Package pinout**

Matte tin, Lead Free (Green)	1- NC	9- NC	17- NC
Units : mm	2- NC	10- VD3S	18- NC
From the standard : JEDEC MO-220	3- GND <sup>(6)</sup>	11- GND <sup>(6)</sup>	19- VD4N
(VGGD)	4- RF in	12- VD4S	20- VD3N
25- GND <sup>(6)</sup>	5- GND <sup>(6)</sup>	13- NC	21- VD12
	6- NC	14- GND <sup>(6)</sup>	22- VG4
	7- NC	15- RF out	23- VG3
	8- GND <sup>(6)</sup>	16- GND <sup>(6)</sup>	24- VG12

<sup>(6)</sup> It is strongly recommended to ground all pins marked “GND” through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package. See application note AN0017 for details.

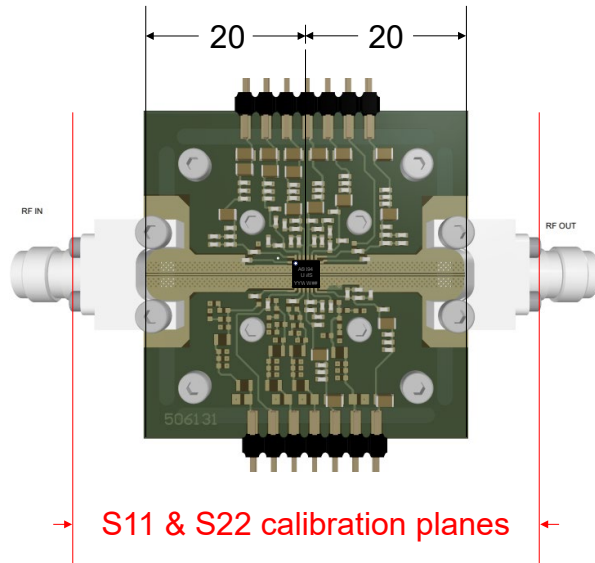
### Definition of the Sij reference planes

The reference planes used for S21 measurements are symmetrical from the central axis of the package (see drawing beside). The input and output reference planes are located at 2.89mm offset from the central axis. The S21 parameter measurements include this given PCB pattern (see paragraph "Evaluation board").



### Definition of the Sii reference planes

The reference planes used for S11 and S22 measurements are symmetrical from the central axis of the package (see drawing beside). The input and output reference planes are located at 20mm offset from the central axis. The S11 and S22 measurements include this given PCB pattern, the RF lines of the evaluation board and the RF connectors.



**ESD sensitivity**

ESD – Human Body Model (HBM)  
Class 1A / 250V to < 500V

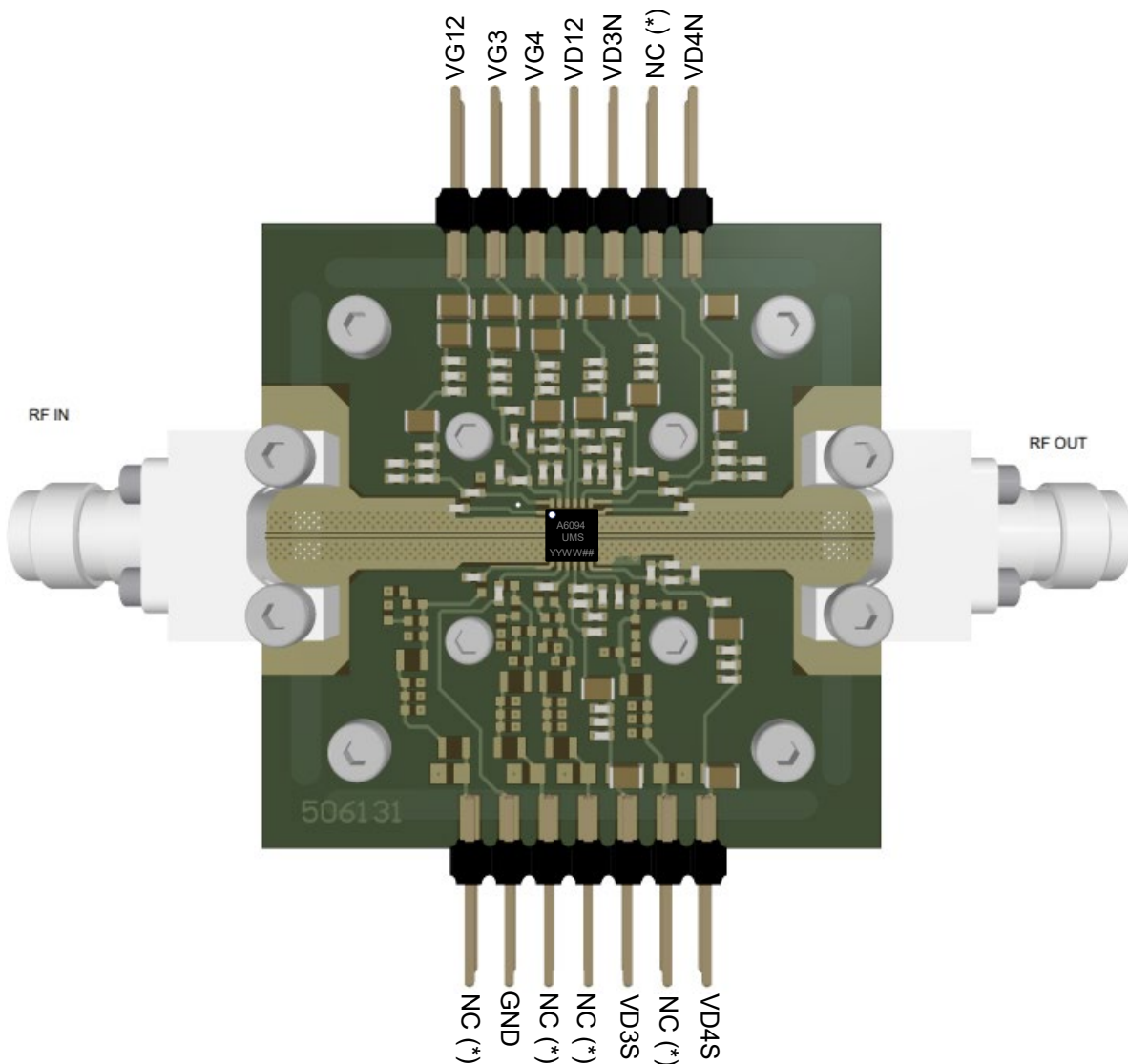
ESD – Machine Model (MM)  
Class M1 / < 100 volts  
Class M2 / 100V up to 200V

**Package Information**

<b>Parameter</b>	<b>Value</b>
Package body material	RoHS-compliant
	Low stress Injection Molded Plastic
Lead finish	100% matte tin (Sn)
MSL Rating	MSL3

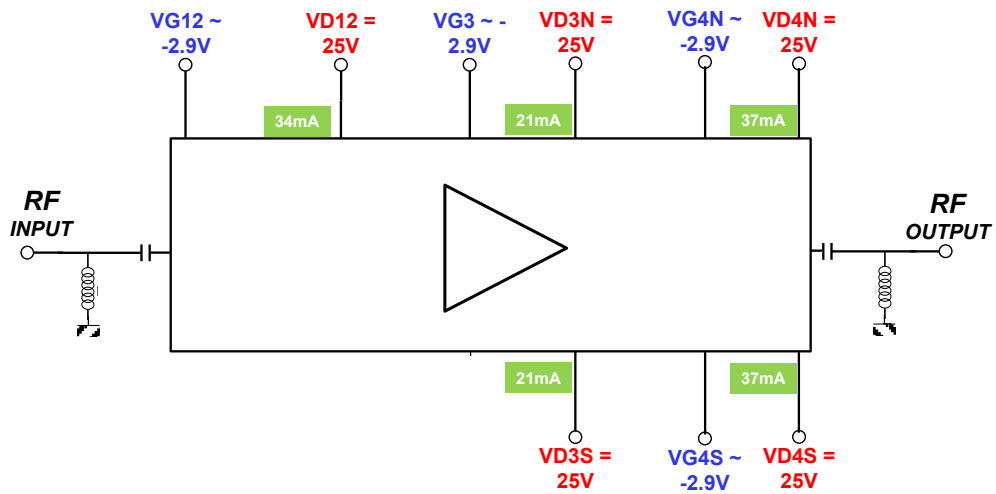
### Evaluation board

- Compatible with the proposed footprint.
- Based on typically MT77 / 10mils or equivalent.
- Using a micro-strip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 100pF  $\pm$ 5%, 10nF  $\pm$ 10% and 1 $\mu$ F  $\pm$ 10% are recommended for all DC accesses.
- To ensure safe operation, all measurements must be performed using **shielded cables**, even for DC bias.



(\*) Pins not connected.



**DC Schematic**

The DC pins do not include any decoupling capacitor in package, therefore it is mandatory to provide a good external DC decoupling (100pF  $\pm$ 5%, 10nF  $\pm$ 10% and 1 $\mu$ F  $\pm$ 10%) on the PC board, as close as possible to the package.

## Recommended package footprint

Refer to the application note AN0017 available at <https://www.ums-rf.com> for package footprint recommendations.

## SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017 at <https://www.ums-rf.com>.

## Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACH N°1907/2006. More environmental data are available in the application note AN0019 also available at <https://www.ums-rf.com>.

## Recommended ESD management

Refer to the application note AN0020 available at <https://www.ums-rf.com> for ESD sensitivity and handling recommendations for the UMS package products.

## Ordering Information

QFN 4x4 package:

CHA6094-QKB/XY

Stick: XY = 20

Tape & reel: XY = 21

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