United Monolithic Semiconductors

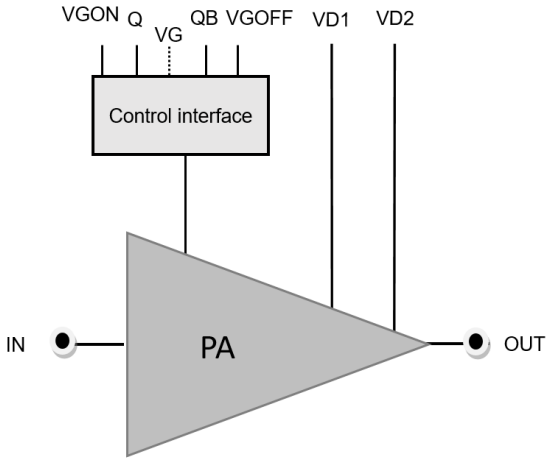
CHA5618-99F

6-18 GHz Power Amplifier

GaN Monolithic Microwave IC

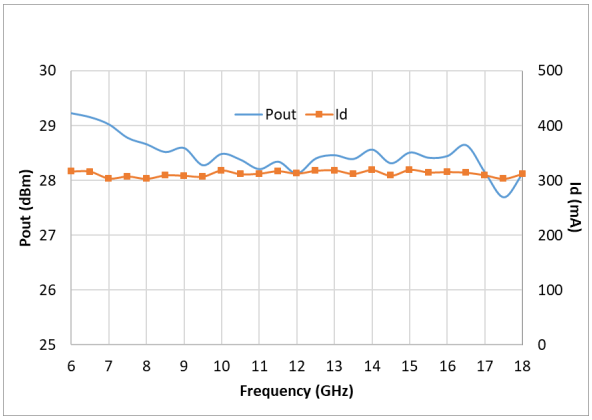
Description

The CHA5618-99F is a monolithic GaN Driver Amplifier in the frequency band 6-18GHz with a control interface for speed switching. This driver provides 28dBm of Output Power. The circuit exhibits a small signal gain of 22dB. The overall power supply is of 20V/150mA (quiescent current).
It is designed for a wide range of applications, for military systems, such as electronic warfare, and test instrumentation.
The part is manufactured on robust GaN HEMT technology and is available as a bare die.



Main Features

- Broadband performances: 6-18GHz
- Linear Gain = 22dB
- Pout = 28dBm for +12dBm Input Power
- Id associated current = 300mA
- DC bias: Vd=20V @Idq = 150mA
- 2.6x3.0mm²



Main Electrical Characteristics

Tcase = +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	6		18	GHz
Gain	Linear Gain		22		dB
Pout	Output Power @3dB comp. (Pin = 8dBm)		26		dBm
Psat	Output Power @saturation (Pin = 12dBm)		28		dBm
Id	Drain current @saturation (Pin = 12dBm)		300		mA

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Specifications

Tcase = +25°C, Vd = +20V, Idq = 150mA

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	6		18	GHz
Gain	Linear Gain		22		dB
Pout	Output Power @3dB comp. (Pin = 8 dBm)		26		dBm
Psat	Output Power @saturation. (Pin = 12dBm)	28			
Id	Drain current @saturation. (Pin = 12 dBm)		300		mA
S11	Input return loss		-15		dB
S22	Output return loss		-15		dB
Idq	Quiescent current		150		mA
Vd	Drain voltage		20		V
Vg	Gate voltage		-2.7		V

These values are representative of measurements done in test fixture with a bonding wire of typically 0.25nH to 0.3nH.

Absolute Maximum Ratings (1) (2)

Tcase = +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	27	V
Pin	Maximum peak input power overdrive	15	dBm

(1) Operation of this device above anyone of these parameters may cause permanent damage.

(2) See Device thermal performances section page 5/20

Recommended Operating Range

Tcase = +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	20	V
Id	Drain bias current (no RF)	150	mA
Pin	Maximum peak input power overdrive	12	dBm
Tj	Maximum Junction temperature (2)	200	°C

These values are representative of measurements done in test fixture with a bonding wire of typically 0.25nH to 0.3nH.

Temperature Range

Tcase	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +150	°C

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Typical Bias Conditions

Two biasing procedures are available:

1. By using standard VG biasing
2. By using the control interface

Standard VG biasing

Tcase=+25°C

Symbol	Pad N°	Parameter	Values	Unit
VG	17	Gate voltage tuned for Idq ≈ 150mA	-2.7	V
VD1	13	1st stage drain voltage	20	V
VD2	11	2nd stage drain voltage	20	V

"Power ON" sequence

1. Bias PA gate voltage at VG close to Vpinch-off (Typically: Vg ≈ -5V)
2. Apply VD1 & VD2 bias voltage (Typically: VD = 20V)
3. Increase VG up to quiescent bias drain current Idq (pulsed applied on the gate)
4. Apply RF signal

"Power OFF" sequence

1. Turn off RF signal
2. Bias HPA gate voltage at VGON close to Vpinch-off (Typically: Vg ≈ -5V)
3. Turn VD1 & VD2 bias voltage to 0V
4. Turn VG bias voltage to 0V

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Typical Bias Conditions

Control interface

Tcase=+25°C

Symbol	Pad Nº	Parameter	Values	Unit
VGON	19	Gate voltage tuned for Idq ≈ 150mA	≈-2.7	V
VGOFF	14	Gate pinch off voltage	-5	V
VD1	13	1st stage drain voltage	20	V
VD2	11	2nd stage drain voltage	20	V

Truth table

Driver State	Q	QB	VGON	VGOFF
Mode ON	-4V	-11V	≈-2.7V	-5V
Mode OFF	-11V	4V	≈-2.7V	-5V

"Power ON" sequence

1. PA gate voltage at VGON & VGOFF close to Vpinch-off (Typically: Vg ≈ -5V)
2. Bias PA gate voltage at QB = -11V
3. Bias PA gate voltage at Q = -4V
4. Apply VD1 & VD2 bias voltage (Typically: VD = 20V)
5. Increase VGON up to quiescent bias drain current Idq
6. Apply RF signal

"Power OFF" sequence

1. Turn off RF signal
2. Bias HPA gate voltage at VGON close to Vpinch-off (Typically: Vg ≈ -5V)
3. Turn VD1 & VD2 bias voltage to 0V
4. Turn VGON bias voltage to 0V
5. Turn VGOFF bias voltage to 0V
6. Turn Q & QB voltage to 0V

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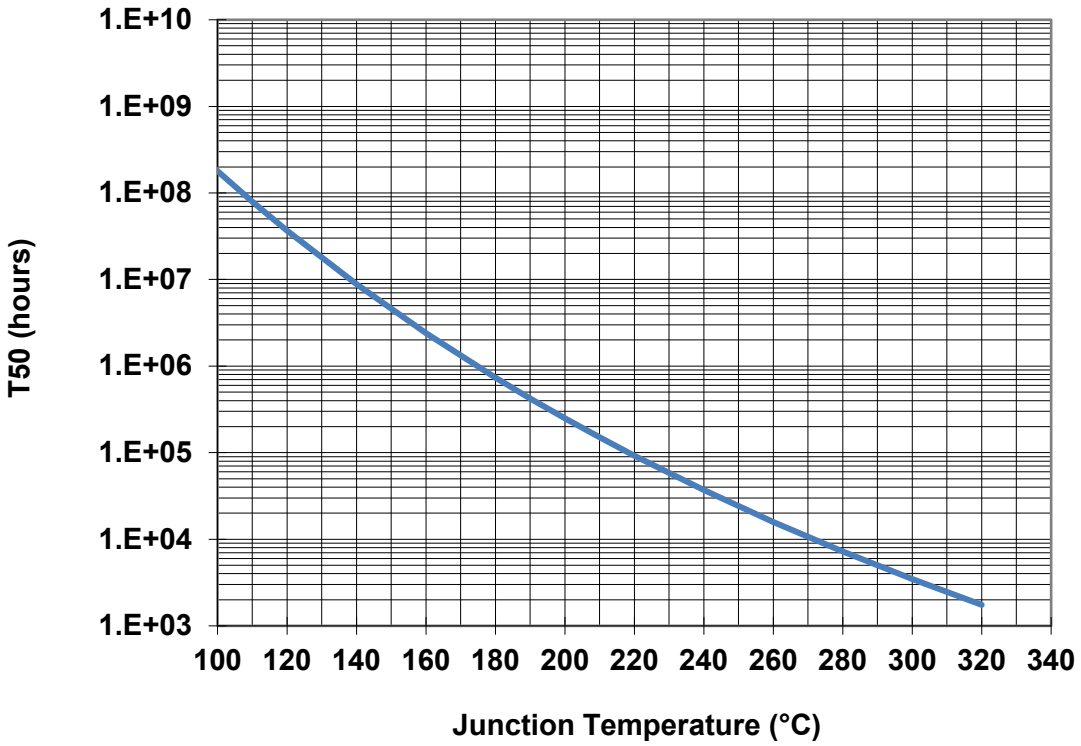
Device thermal performances

All the figures given in this section are obtained assuming that the die is only cooled down by conduction through the chip backside.
The temperature is monitored at the chip back-side interface (Tbackside).
The system maximum temperature must be adjusted in order to guarantee that Tjunction remains below the maximum value specified in the Absolute Maximum Ratings table.
So, the system PCB must be designed to comply with this requirement.

Parameter	Biasing conditions	Tjunction (°C)	R_{TH} (°C/W)	T50 (hours)
R_{TH} [1] Thermal Resistance (Junction to Case)	Vd= 20V Pout= 28dBm Pdiss= 8W	140	6.9	1.9E+06

[1] Assuming 85°C Tcase



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Typical On wafer measurements: Sij parameters

Tcase=+25°C, Vd = +20V, Id = 150mA

Freq (GHz)	S11 (dB)	PhS11 (°)	S12 (dB)	PhS12 (°)	S21 (dB)	PhS21 (°)	S22 (dB)	PhS22 (°)
6	-26.35	98.67	-56.40	-5.03	22.30	142.03	-7.94	-82.87
6.5	-28.19	101.23	-54.53	-26.76	22.29	118.85	-9.53	-91.72
7	-28.86	104.35	-54.13	-47.93	22.24	95.32	-11.73	-97.14
7.5	-28.60	108.45	-53.07	-72.01	22.27	72.85	-14.25	-95.47
8	-27.20	103.65	-52.17	-90.59	22.06	50.48	-16.27	-82.43
8.5	-25.40	96.48	-51.16	-111.99	22.10	28.37	-15.90	-65.43
9	-24.75	81.05	-50.64	-128.57	21.92	6.15	-14.17	-57.06
9.5	-23.51	67.34	-50.51	-150.34	21.86	-15.64	-12.38	-57.27
10	-23.02	52.24	-49.96	-170.72	21.80	-36.88	-10.96	-63.77
10.5	-22.47	38.80	-49.34	170.98	21.80	-58.66	-9.91	-70.33
11	-21.71	27.18	-48.33	153.12	21.82	-80.99	-9.33	-78.86
11.5	-21.35	14.00	-48.34	135.31	21.70	-103.17	-9.17	-88.15
12	-21.12	13.09	-47.23	117.07	21.83	-125.20	-9.19	-96.71
12.5	-19.78	8.65	-46.45	95.25	21.94	-149.28	-9.49	-107.32
13	-19.03	5.18	-45.68	70.41	21.86	-171.20	-10.17	-115.82
13.5	-17.41	3.94	-44.89	51.45	22.01	165.03	-11.10	-126.49
14	-15.88	0.79	-43.24	29.15	22.05	141.84	-12.83	-137.08
14.5	-14.49	-8.10	-42.59	3.56	22.00	117.07	-15.62	-141.32
15	-13.28	-12.28	-41.85	-20.19	21.76	93.24	-18.01	-143.78
15.5	-12.48	-21.08	-41.42	-46.87	21.69	66.73	-22.43	-117.27
16	-10.79	-25.58	-40.93	-69.27	21.52	42.44	-22.12	-87.81
16.5	-10.29	-33.07	-40.87	-95.80	21.42	15.79	-19.07	-64.72
17	-9.08	-41.45	-40.54	-116.34	21.13	-8.06	-15.98	-55.68
17.5	-8.30	-52.11	-39.80	-138.50	20.90	-32.31	-14.03	-58.63
18	-8.01	-63.62	-39.80	-156.14	20.89	-56.93	-12.57	-60.57

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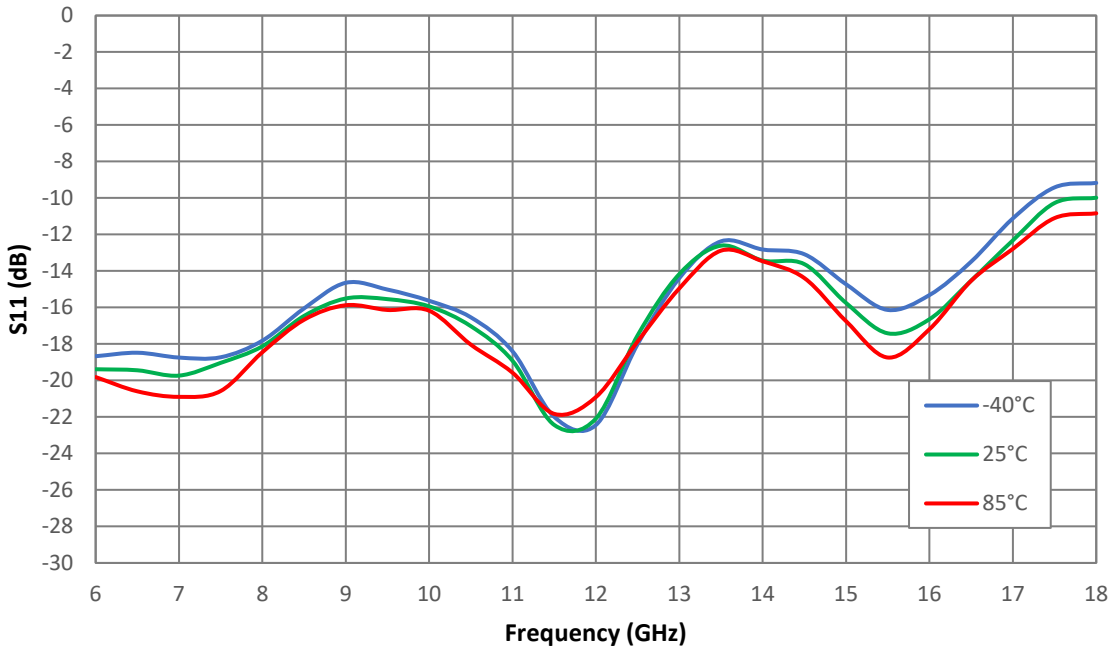
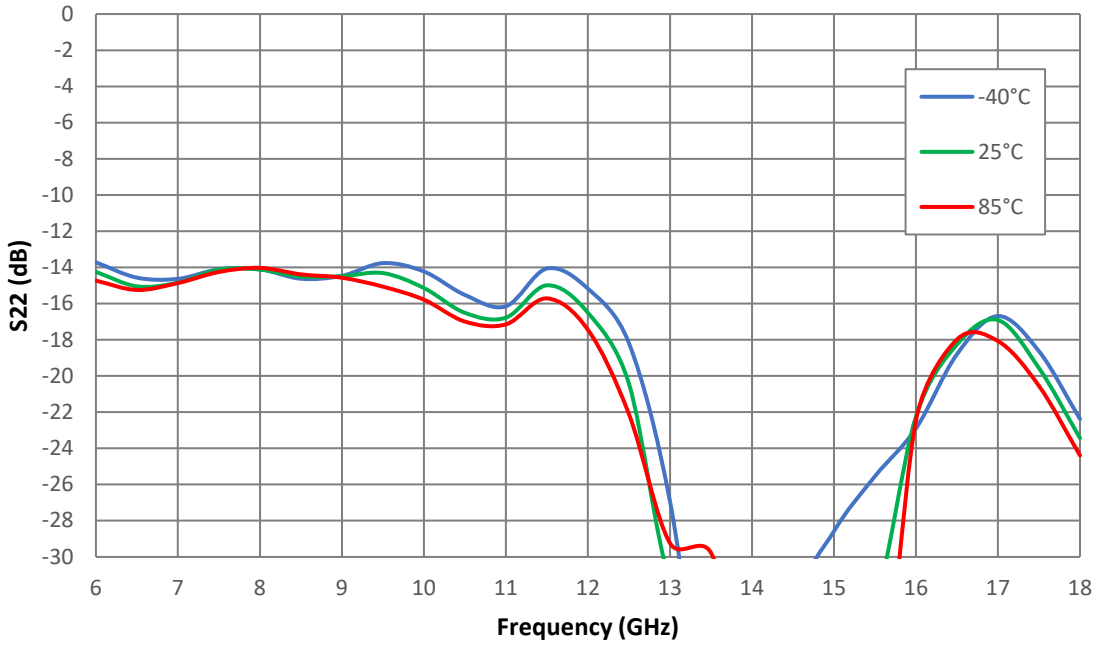
Typical Evaluation Board measurements

Tbackside = -40°C,+25°C & 85°C; Vd = 20V, Id = 150 mA @25°C

Input return loss S11 (dB) vs Frequency (GHz) with temperature variation



Output return loss S22 (dB) vs Frequency (GHz) with temperature variation



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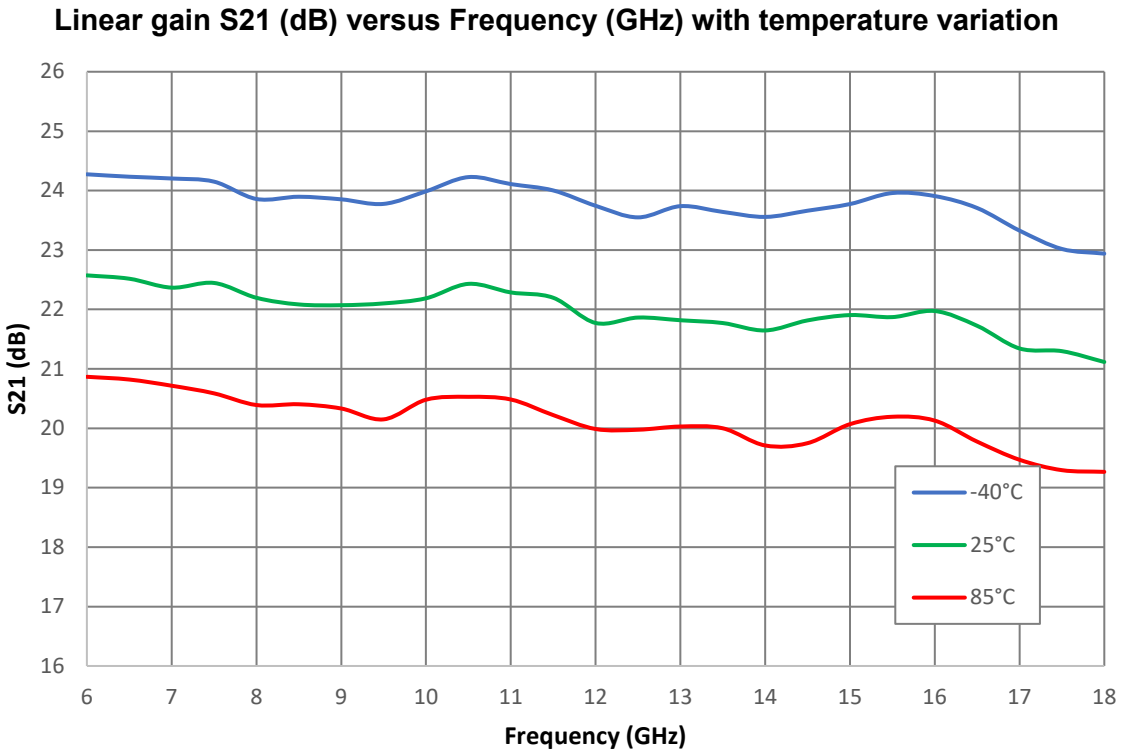
Typical Evaluation Board measurements

Tbackside = -40°C, +25°C & 85°C; Vd = +20, Id = 150 mA @ 25°C



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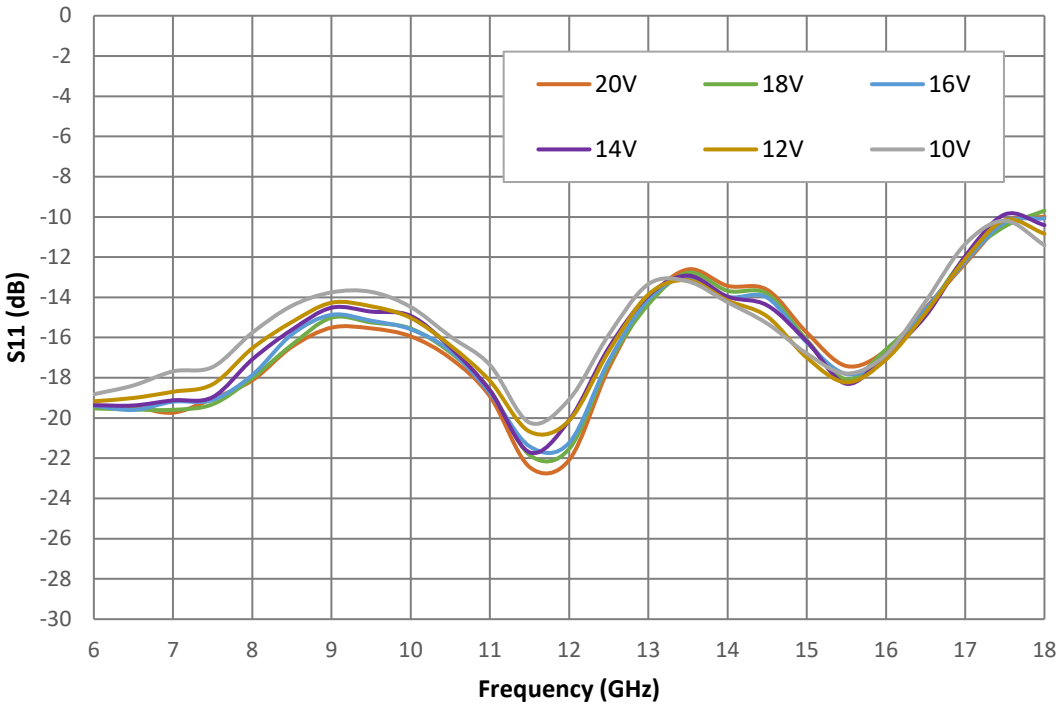
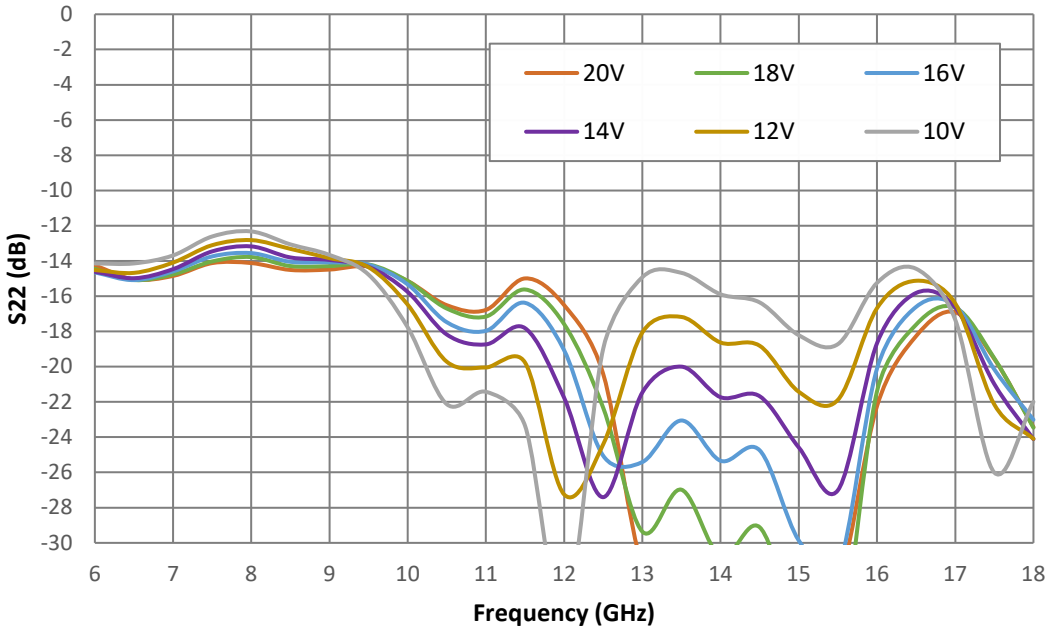
Typical Evaluation Board measurements:

Tbackside = +25°C ; Vd = 10, 12, 14, 16, 18 & 20V, Id = 150 mA

Input return loss S11 (dB) vs Frequency (GHz) with voltage variation



Output return loss S22 (dB) vs Frequency (GHz) with voltage variation



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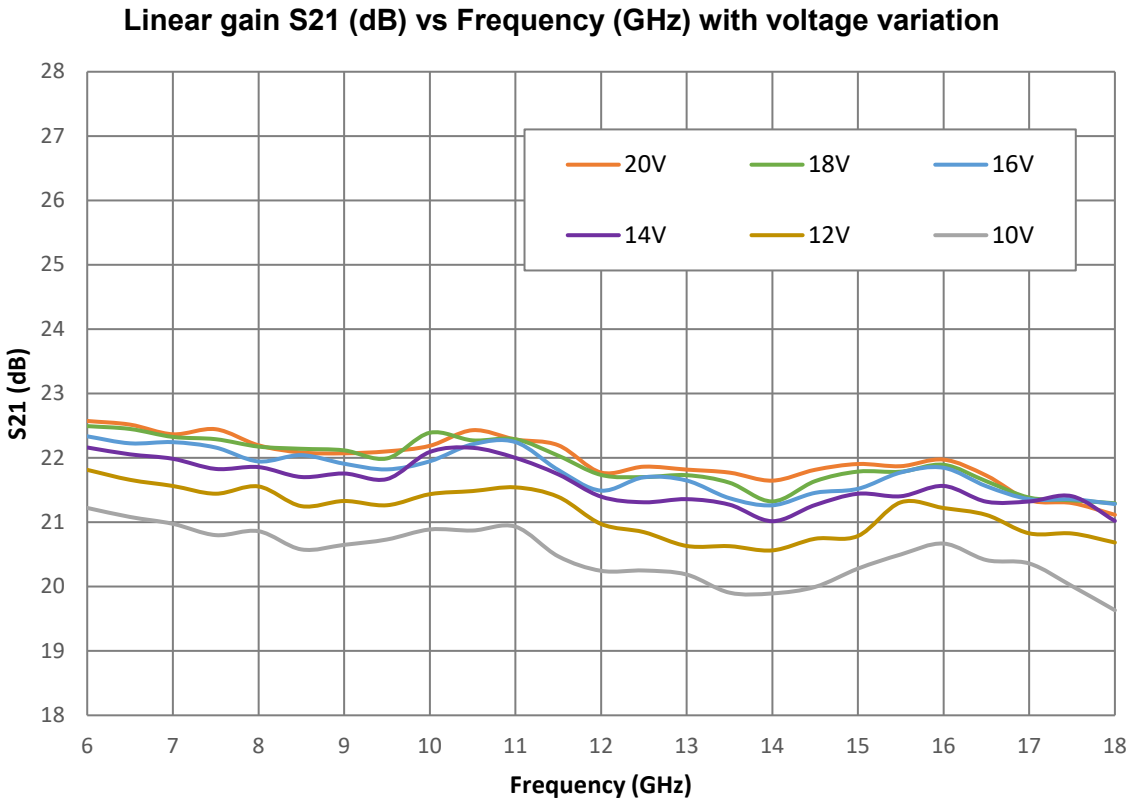
Tbackside = +25°C ; Vd = 10, 12, 14, 16, 18 & 20V, Id = 150 mA



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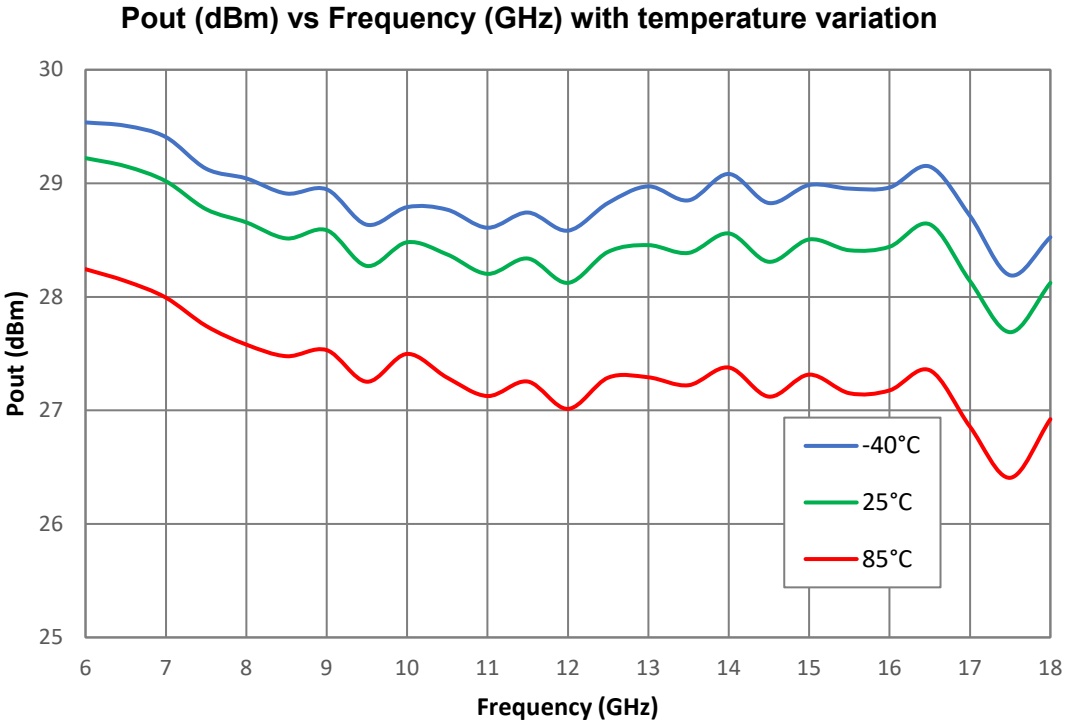
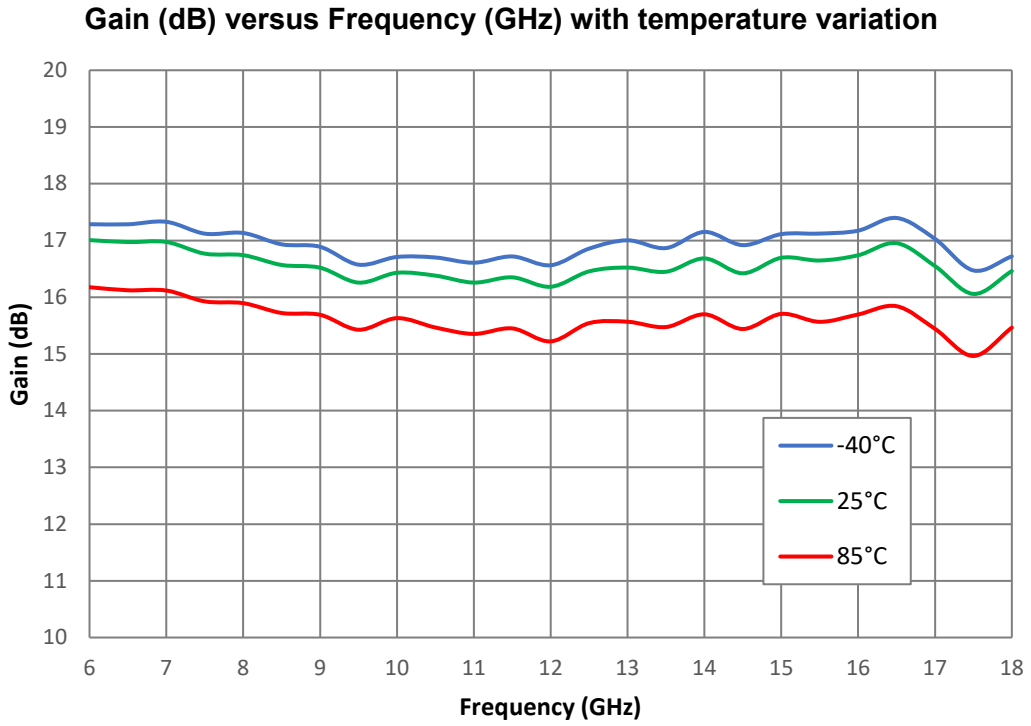
Typical Evaluation Board measurements

Tbackside = -40°C, +25°C & +85°C, Vd = +20V, Id = 150 mA@ 25°C; Pin = 12dBm





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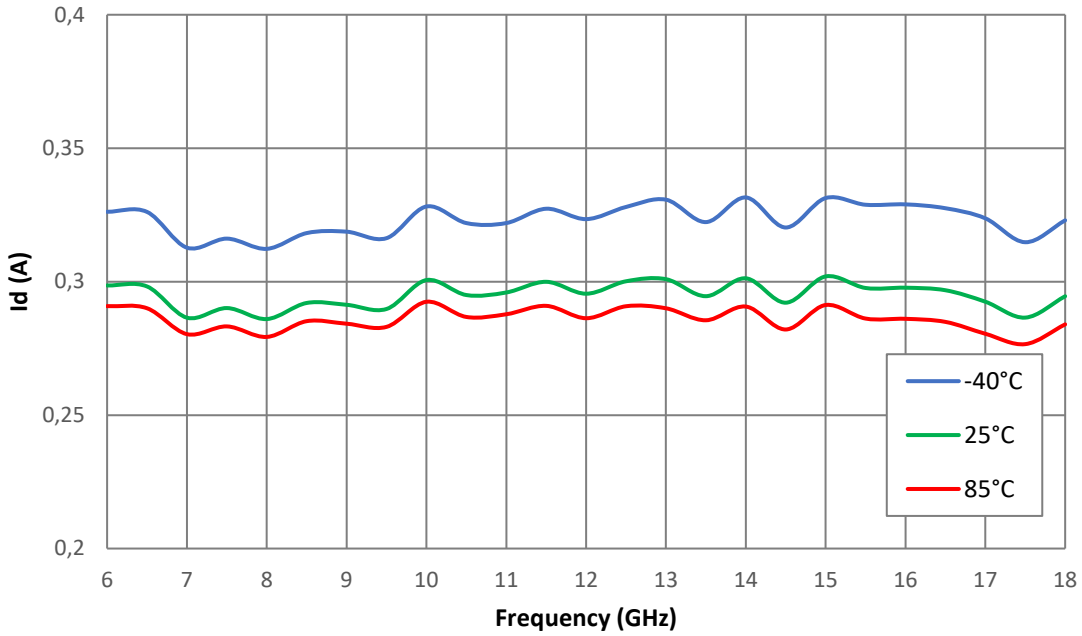
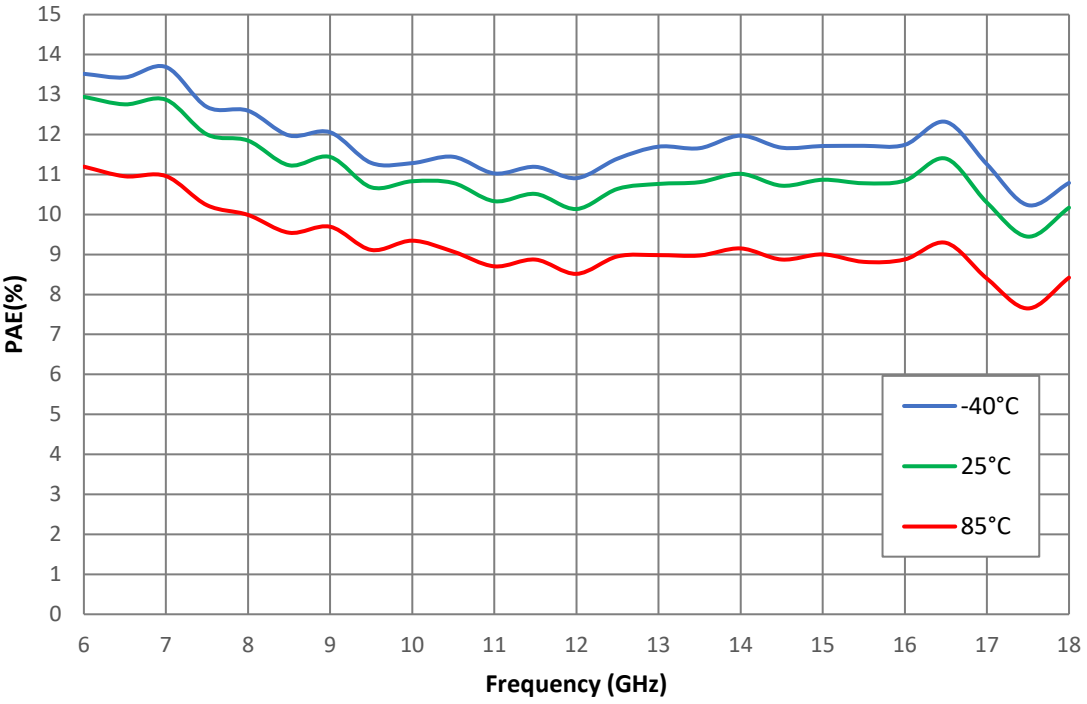
Typical Evaluation Board measurements

Tbackside = -40°C, +25°C & +85°C, Vd = +20V, Id = 150 mA @25°C; Pin = 12dBm

Id (A) versus Frequency (GHz) with temperature variation



PAE (%) versus Frequency (GHz) with temperature variation



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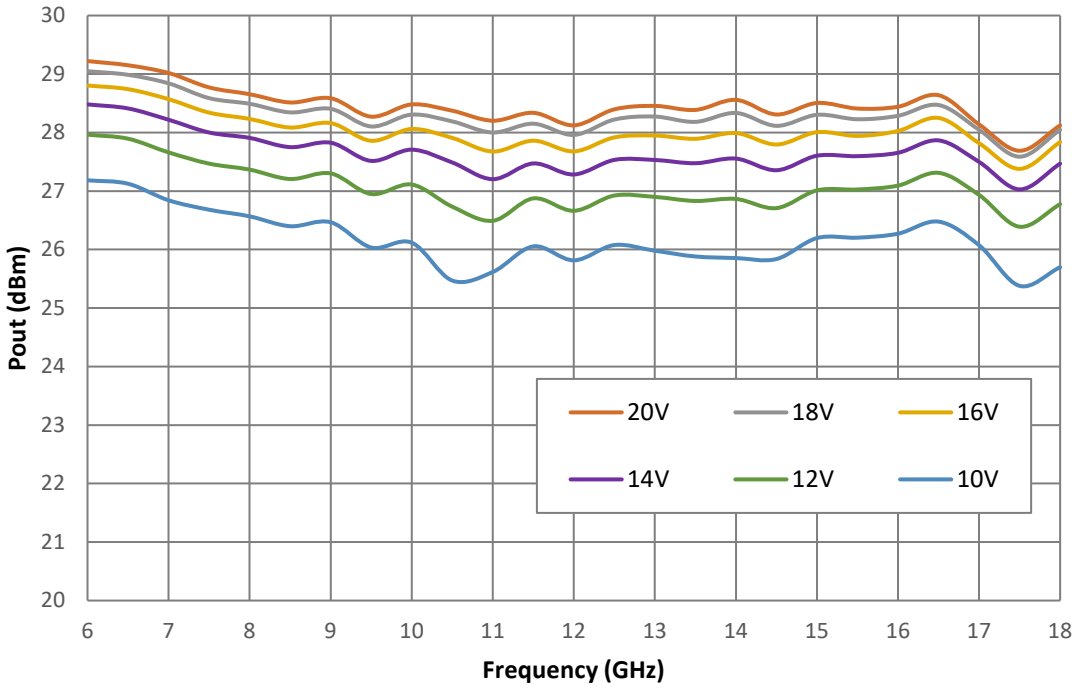
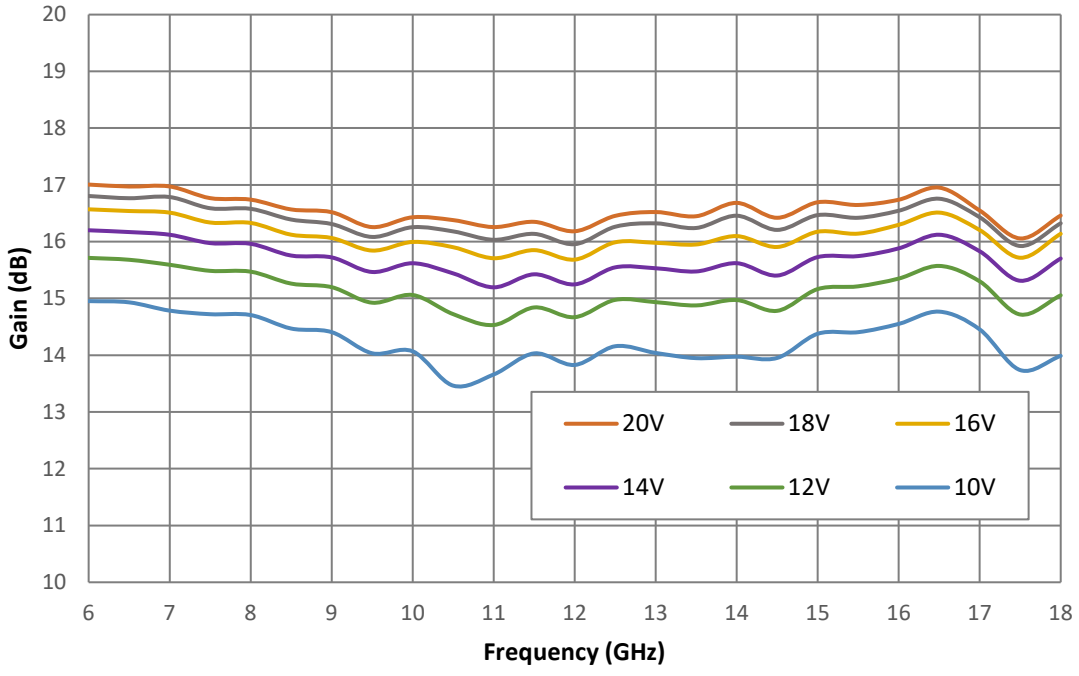
Typical Evaluation Board measurements

Tbackside = 25°C, Vd = 10, 12, 14, 16, 18 & 20V, Id = 150 mA; Pin = 12 dBm

Pout (dBm) versus Frequency (GHz) with voltage variation



Gain (dB) versus Frequency (GHz) with voltage variation



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Typical Evaluation Board measurements

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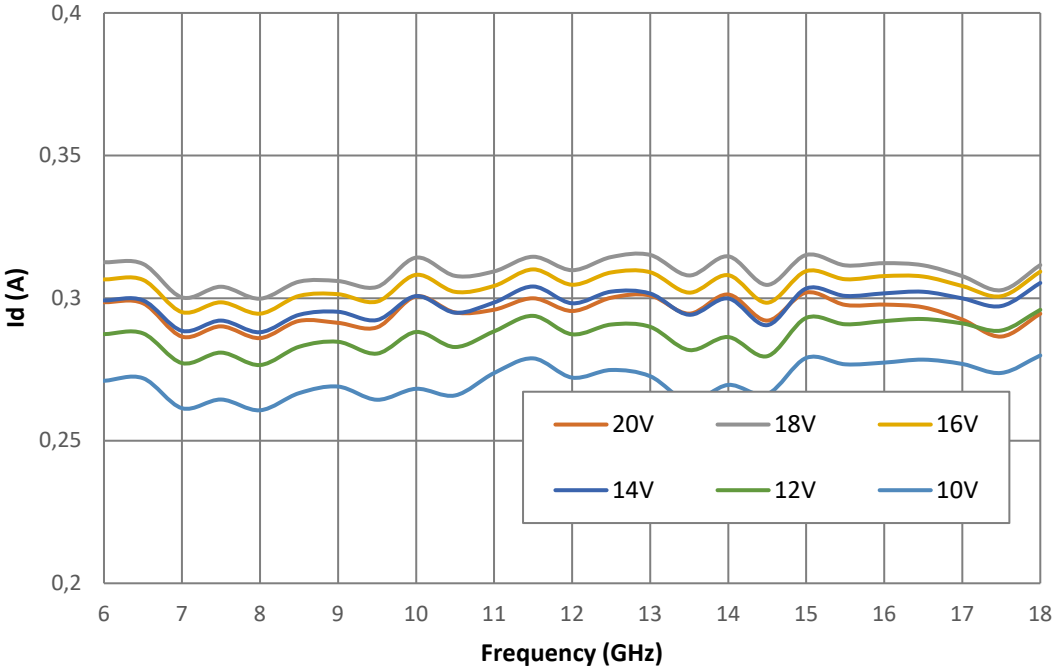
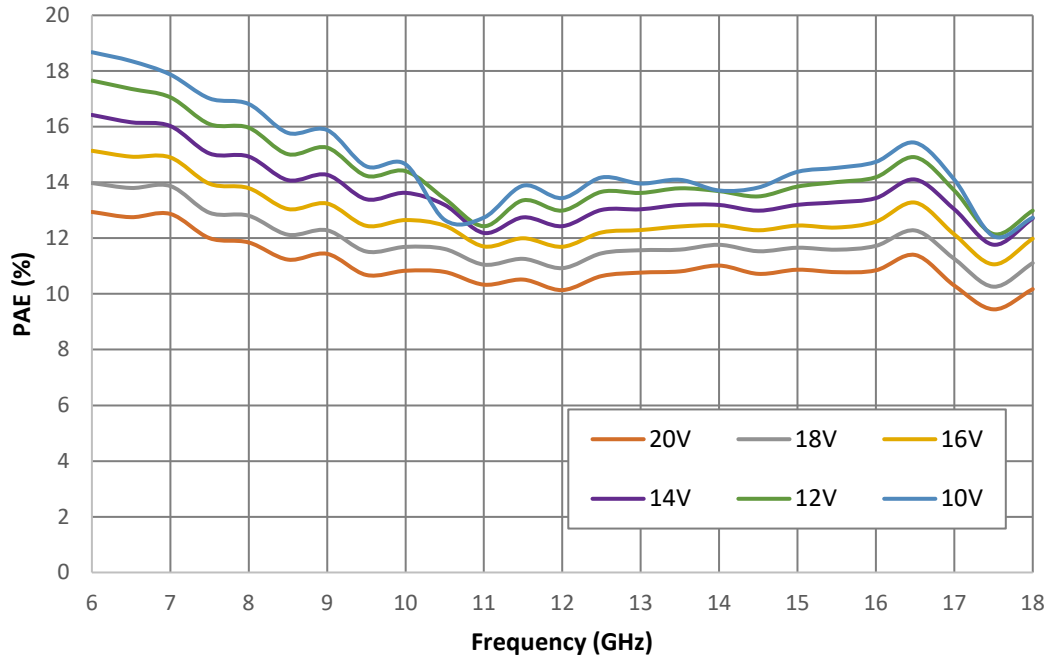
Id (A) versus Frequency (GHz) with voltage variation



PAE (%) versus Frequency (GHz) with voltage variation



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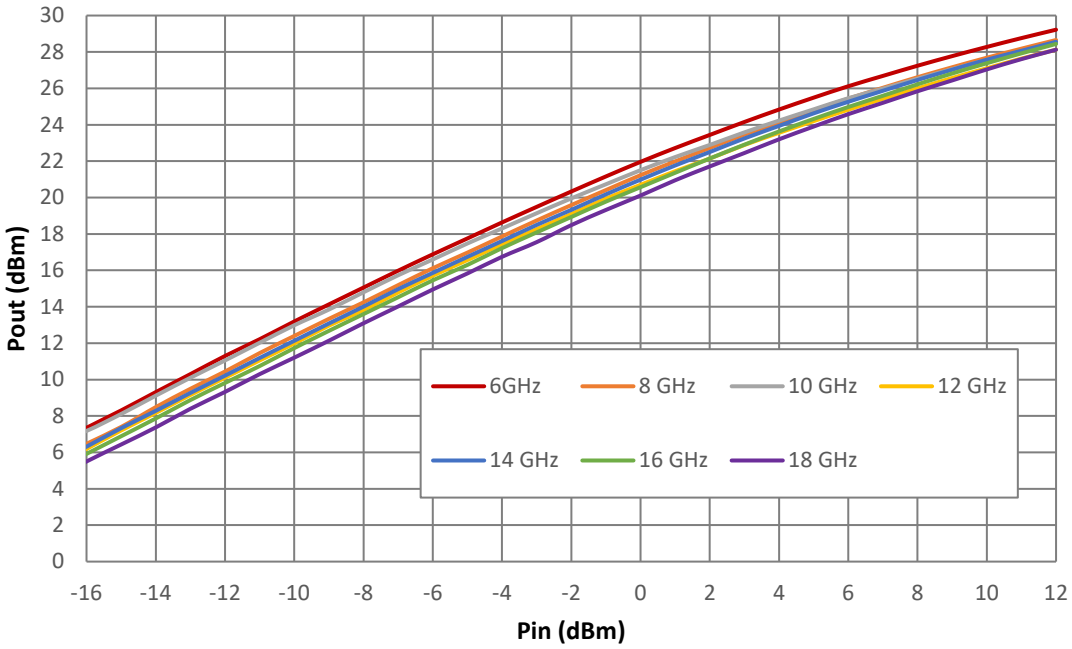
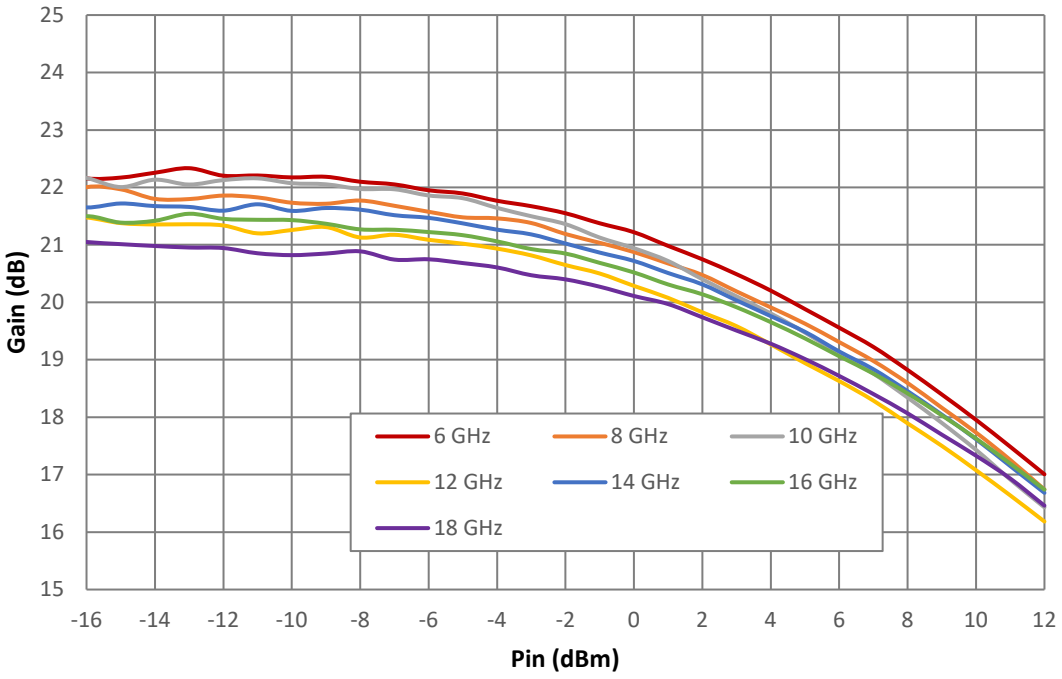
Typical Evaluation Board measurements

Tbackside = +25°C, Vd = +20V, Idq = 150 mA;

Pout (dBm) versus Pin (dBm) with Frequency variation



Gain (dB) versus Pin (dBm) with Frequency variation



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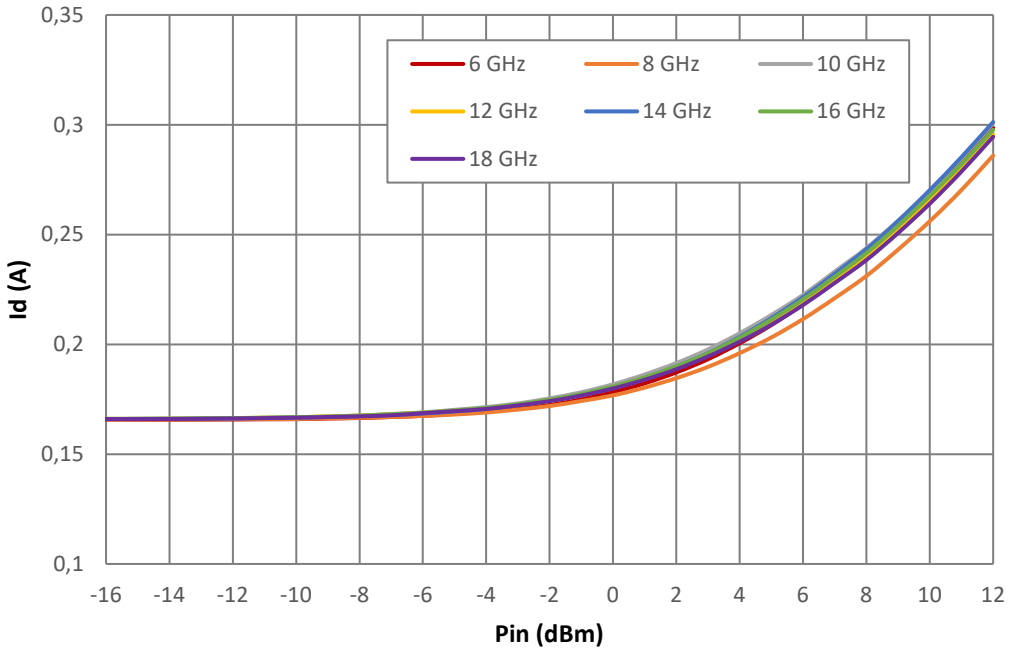
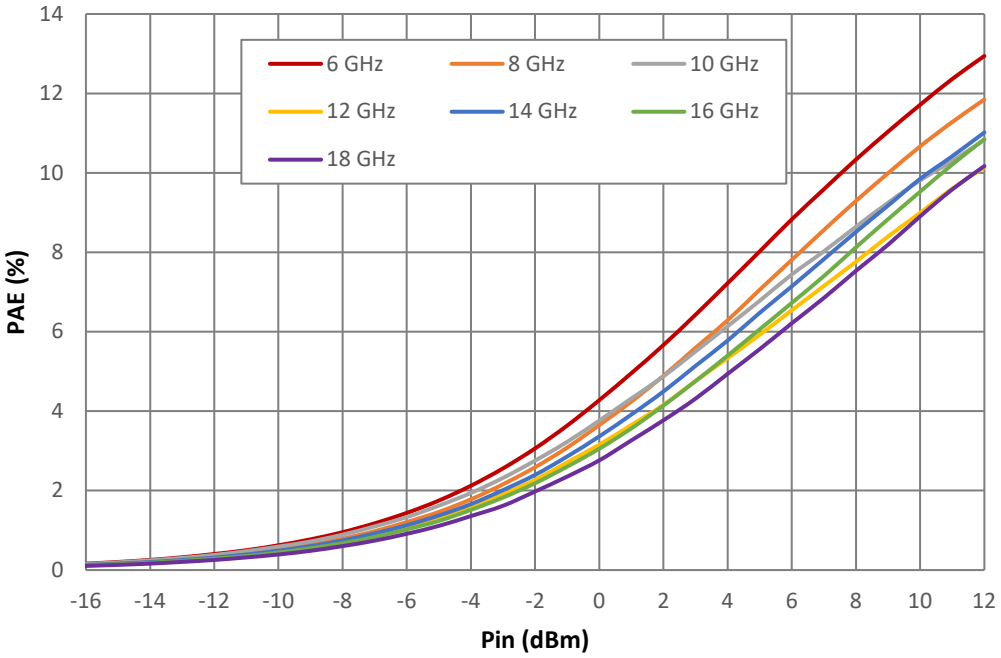
Typical Evaluation Board measurements

Tbackside = +25°C, Vd = +20V, Id = 150 mA

Id (A) versus Pin (dBm) with Frequency variation



PAE (%) versus Pin (dBm) with Frequency variation



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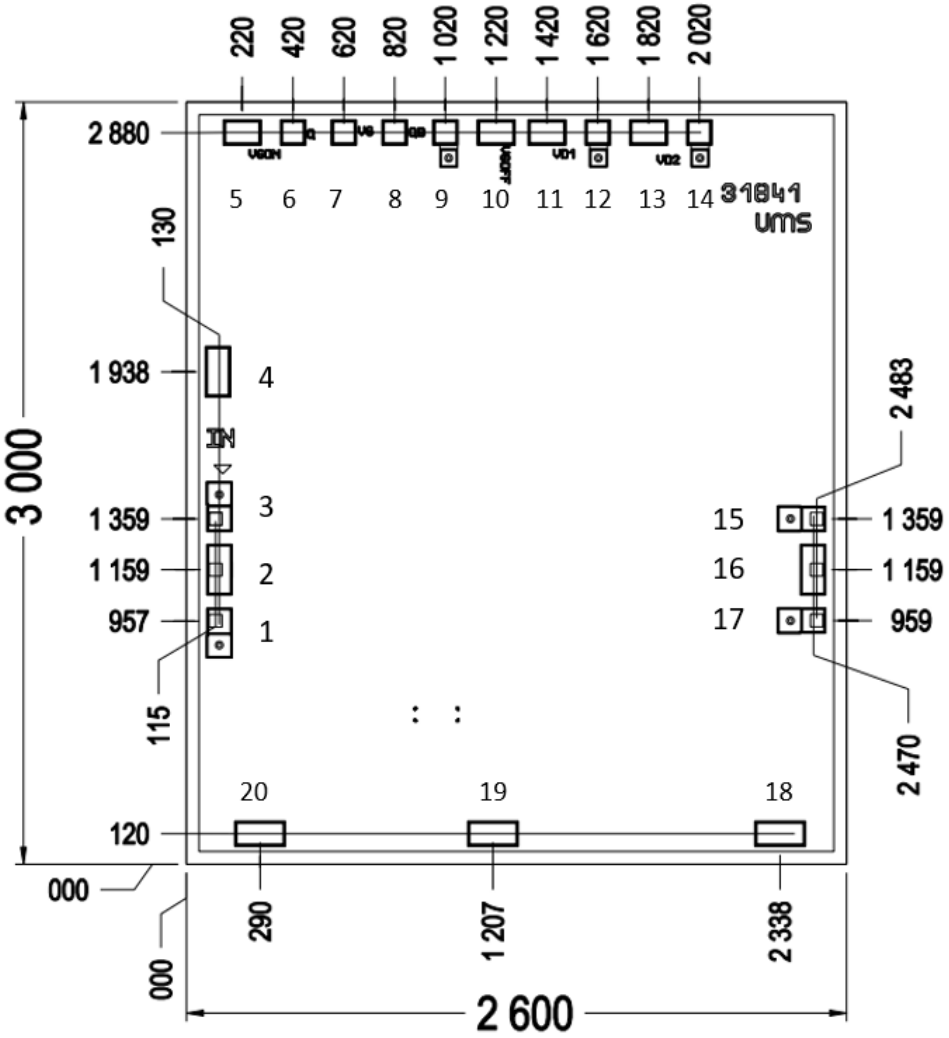
Chip mechanical data



Pad number	Pad name	Pad type	Description
1,3, 15 & 17	GND	RF GND	
9, 12 & 14	GND	DC GND	
2	IN	RF IN	RF input signal
16	OUT	RF OUT	RF output signal
13	VD2	Supply	2nd stage drain supply
11	VD1	Supply	1st stage drain supply
10	VGOFF		Gate pinch off voltage
8	QB		Gate control voltage
7	VG	Supply	Gate supply
6	Q		Gate control voltage
5	VGON		Gate bias voltage
4, 18, 19 & 20	-	Not connected	Relay pad

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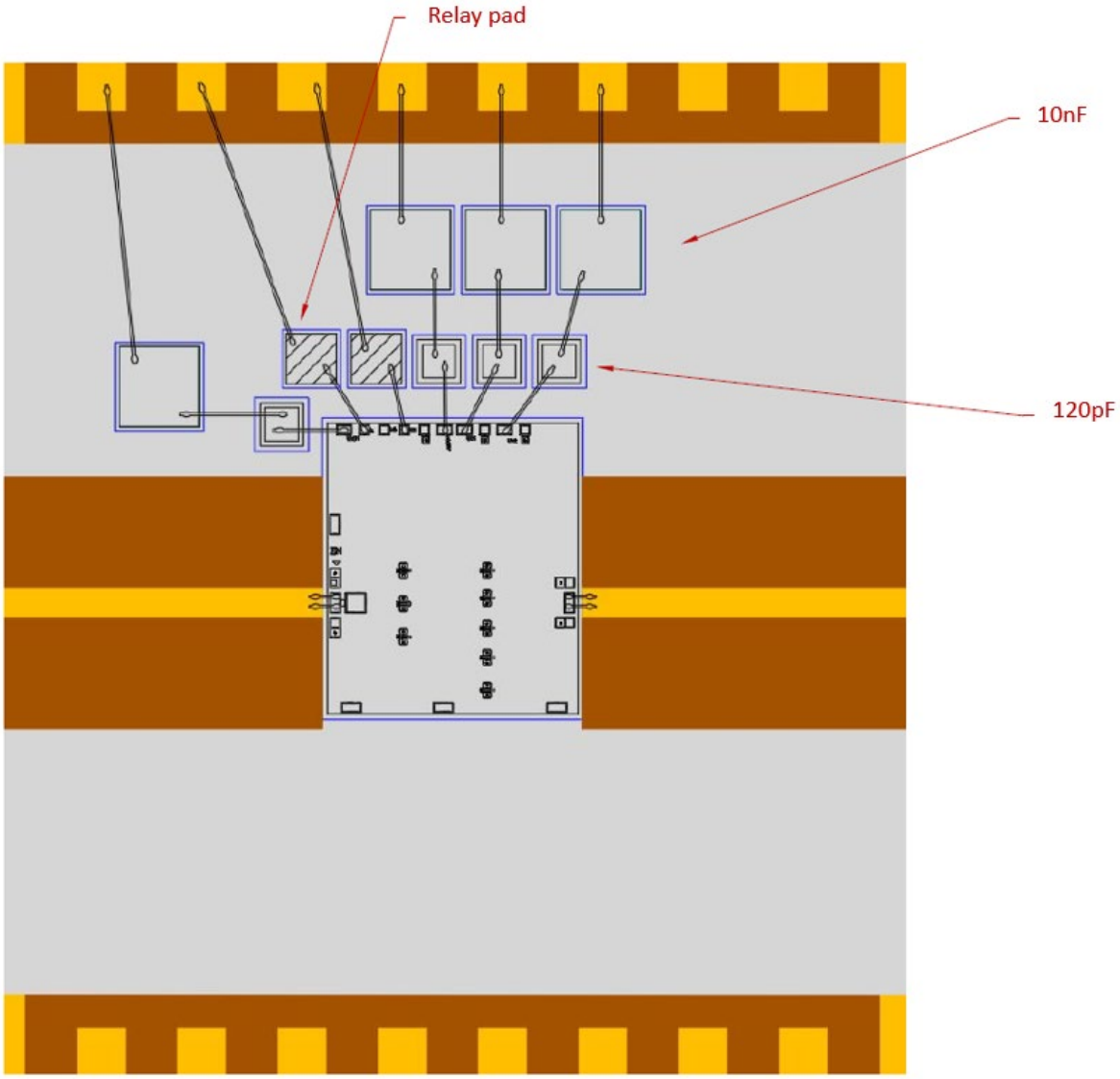
Recommended assembly plan

- Compatible with the proposed footprint.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 120pF, 10nF and 1µF are recommended for all DC accesses.
- See application note AN0030 for details.



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Recommended ESD management

Refer to the application note AN0020 available at https://www.ums-rf.com for ESD sensitivity and handling recommendations for the UMS products.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at https://www.ums-rf.com.

Recommended reflow process assembly

Refer to the application note AN0001 available at https://www.ums-rf.com for die attach.

Ordering Information

Chip form:	CHA5618-99F/00

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