Shared Foundry Offer 2023

United Monolithic Semiconductors

Take advantage of UMS ULRC-20 passive process for Accurate and robust circuit elements

United Monolithic Semiconductors is opening **a shared foundry run on ULRC-20 passive process**. The launch date for the Multi-Project Wafer is **July 21, 2023**

ULRC-20 passive GaAs process allows very diverse passive circuit design including accurate microwave filters, RF power combiners, microwave baluns, matching elements, robust power lines, power bar input and output circuits.

Optimized for reproducibility, power handling and low losses, high frequency and high volume high yield production, **ULRC-20** is widely recommended for the design of hybrid microwave circuits for amplifier modules used into antenna transmitters and receivers such as Radars, Telecommunications and Space Communication systems.

Designers are invited to share a **ULRC-20** run at an affordable entry price of 1 400€/mm².

What are the main characteristics of ULRC-20?

Element	Parameter	Typical value	Conditions
MIM Cap.	Density (pF/mm²)	175	@ 1 MHz
Spiral Inductor	Inductance (nH)	0.12 to 13	
TaN Resistor	Sheet Resistance (Ω/□)	30	
TiWSi Resistor	Sheet Resistance (Ω/□)	1000	
Wafer thickness	(µm)	100	

Examples of microwave performance achieved by UMS catalogue products designed with ULRC-20 process (in combination with GaN devices):

Part Number	Freq (GHz)	Gain (dB)	Power Pulsed (W)	PAE (%) Pulsed	Bias A / V
CHZ015AaQEG	1.2-1.4	17,2	15	>55	0.1 / 45
CHZ180AaSEB	1.2-1.4	20	200	52	1.3 / 45

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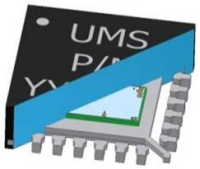
By choosing standard MMIC dimensions which are compatible with QFN high volume packaging capability, your project is on track for future industrial success.



How to participate to this shared foundry run?

So to start designing, please apply on-line for process Design Kit. Before the deadline, please send your layout to: foundry@ums-rf.com

INFORMATION	For engineering purpose only Simply provide your GDS file before July 21, 2023
DELIVERY	16 Engineering chips, from a PCM tested wafer
CONDITIONING	Gel-Pak® box

AVAILABLE DIE SIZE (mm)	1	2	3	4
MAX RATIO	1:4			

Die size include 100µm dicing street - No inspection, not test on MMIC
Launching date flexibility is +/- 2 weeks
Minimum order is 4mm² - Price is valid until July 21, 2023
Order to be placed before July 7, 2023
Important Notes:

- UMS may cancel the run in case of insufficient number of participants.
- For some countries a specific dedicated export license may be required before deliv

	1.4	2	2.4	3.4	4
1.4	2	2.8	3.4	4.8	5.6
2	2.8	4	4.8	6.8	8
2.4	3.4	4.8	5.8	8.2	9.6
3.4	4.8	6.8	8.2	11.6	13.6
4	5.6	8	9.6	13.6	16

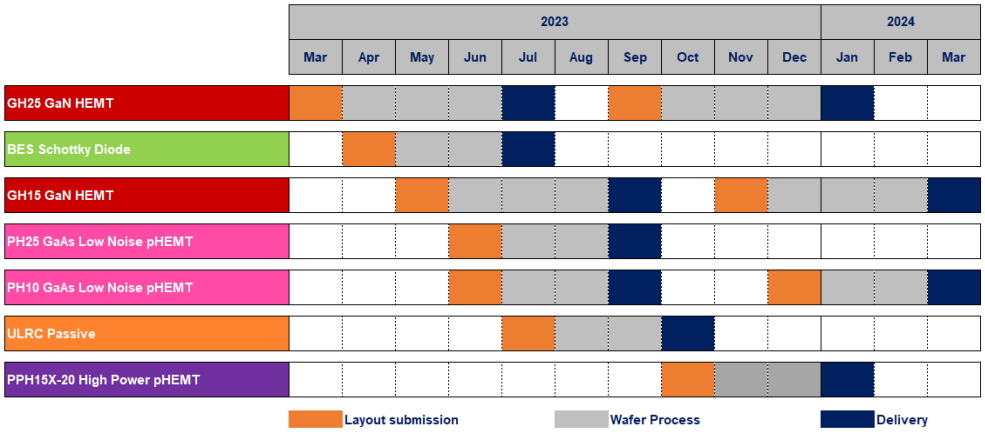
ULRC mask tile with available die size (mm)

How many dies will I receive and how much does it cost?

You will receive 20 dies of your circuit in Gel-Pak® box from a ULRC PCM good wafer. The price is based on your circuit dimensions on the mask tile multiplied by the mm² unit price.

For example, if your circuit is 2 x 3.4 mm², the price is 2 x 3.4 x 1 400€ = 9 520€.

Which processes are regularly offered in shared foundry?



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