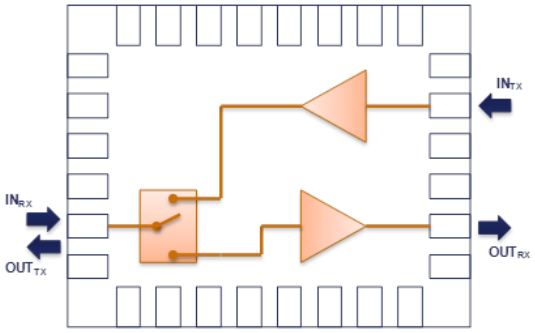
Advanced Information: AI2016

24.25-30.5GHz High Power Front End

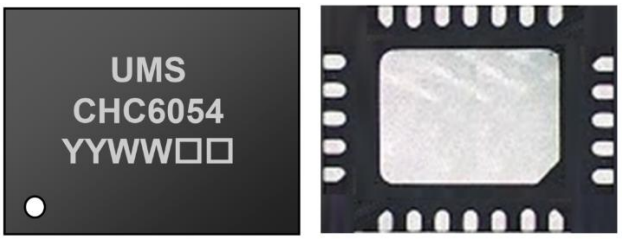
GaN & GaAs Monolithic Microwave IC SMD leadless package



UMS develops a High Power Frond-End (HPFE) featuring Transmit and Receive paths combined with In/Out Switch. This circuit operates in the 24.25-30.5GHz bandwidth. It is specially designed for telecommunication radio links. It typically exhibits a Receiver gain of 18dB with a low noise figure of 3.2dB, a Transmit gain of 28dB with 31dBm saturated output power. It features good linearity with an ACPR of 36dBc @23dBm average Pout with 56MHz modulation bandwidth and 4QAM.

This HPFE is realized on mixed technologies 150nm Gallium Nitride on Silicon Carbide (AlGaN/GaN on SiC) and 150nm Gallium Arsenide (GaAs) - UMS proprietary technologies - and provided in a cost effective plastic package
It is well suited for :

- 5G mmw Mobile & Fixed Wireless Access
  24.25-27.5GHz,
  26.5-29.5 GHz,
  27.5-28.35 GHz
- M-MIMO / Phased array antennas
- Time Division Duplex systems



United Monolithic Semiconductors S.A.S.
Bât. Charmille - Parc Mosaic - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34 - www.ums-rf.com

Electrical Characteristics – TX Mode

Tamb.= +25°C, Vd12 = 25V, Vg12 set in order to get Id12 = 40mA

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	24.25		30.5	GHz
Gain	Linear Gain		28		dB
RL_{in}	Input return loss		12		dB
RL_{out}	Output return loss		10		dB
Pdiss	Dissipated Power at Output power average ≈23dBm		3		W
P_{5dB}	Output power at 5dB gain compression		31		dBm

These values are representative of onboard measurements as defined on the drawing in paragraph "Evaluation mother board"

Electrical Characteristics – RX Mode

Tamb.= +25°C, VdL=VgL = 4V @ IdL = 60mA

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	24.25		30.5	GHz
Gain	Linear Gain		18		dB
NF	Noise Figure		3.25		dB
RL in	Input return loss		12		dB
RL out	Output return loss		17		dB
P1dB	Input power at 1dB gain comp		-7		dBm

These values are representative of onboard measurements as defined on the drawing in paragraph "Evaluation mother board".

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Typical Bias Conditions

Symbol	Parameter	Tx mode	Rx mode	Unit
SW	Switch control voltage	0	20	V
Vg1L	LNA 1st stage gate voltage	0	4	V
VdL	LNA drain voltage	0	4	V
Vg1d	Driver 1st stage gate voltage	4	0	V
Vd1d	Driver 1st stage drain voltage	4	0	V
Vg2d	Driver 2nd stage gate voltage	4	0	V
Vd2d	Driver 2nd stage drain voltage	4	0	V
Vg12	HPA gate voltage (quiescent biasing)	-3.1	0	V
Vd12	HPA drain voltage	25	0	V
Is	DC Switch control current Max. Switch control current vs. Pin max.	0 1	0 1	mA
IgL	DC LNA gate current (quiescent biasing) Max. Driver gate current vs. Pin max.	0 0	8 8	mA
IdL	DC LNA drain current (quiescent biasing) Max. Driver drain current vs. Pin max.	0 0	60 70	mA
Igd	DC Driver gate current (quiescent biasing) Max. Driver gate current vs. Pin max.	5 5	0 0	mA
Idd	DC Driver drain current (quiescent biasing) Max. Driver drain current vs. Pin max.	130 175	0 0	mA
Ig12	DC HPA gate current (quiescent biasing) Max. HPA gate current vs. Pin max.	0.001 0.1	0 0	mA
Id12	DC HPA drain current (quiescent biasing) Max. HPA drain current vs. Pin max.	40 500	0 0	mA

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Absolute Maximum Ratings – TX Mode (1)

Tamb.= +25°C

Symbol	Parameter	Values	Unit
Vd12	HPA Drain bias voltage	27	V
Vg12	HPA Gate bias voltage	-9 , -2	V
Id12	HPA drain current at saturated power	700	mA
Vd1d/Vd2d	Driver 1st /2nd stage drain voltage	4.5	V
Vg1d/Vg2d	Driver 1st /2nd stage gate voltage	4.5	V
Idd	Driver drain current at saturated power	200	mA
SW	Switch Control voltage	0	V
Pin	Maximum Input power	+10	dBm
Tc	Operating temperature range	-40 to +95	°C
Tstg	Storage temperature range	-55 to +125	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.

Absolute Maximum Ratings – RX Mode (2)

Tamb.= +25°C

Symbol	Parameter	Values	Unit
VdL	Drain bias voltage	4.5	V
VgL	Gate bias voltage	4.5	V
IdL	LNA drain current at saturated power	100	mA
SW	Switch Control voltage	20	V
Pin	Maximum Input power	-3	dBm
Tc	Operating temperature range	-40 to +95	°C
Tstg	Storage temperature range	-55 to +150	°C

(2) Operation of this device above anyone of these parameters may cause permanent damage.

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Recommended Operating – TX Mode [3] [4]

Tamb.= +25°C

Symbol	Parameter	Values	Unit
Vd12	HPA Drain bias voltage	18 to 25	V
Vg12	HPA Gate bias voltage (quiescent biasing)	-3.1	V
Id12	HPA drain quiescent bias current	40	mA
Vd1d/Vd2d	Driver 1st /2nd stage drain voltage	4	V
Vg1d/Vg2d	Driver 1st /2nd stage gate voltage	4	V
Idd	Driver drain quiescent bias current	130	mA
SW	Switch Control voltage	0	V
Pin	Maximum Input power	+8	dBm

[3] Electrical performances are defined for specified test conditions
[4] Electrical performances are not guaranteed over all recommended operating conditions

Recommended Operating – RX Mode [5] [6]

Tamb.= +25°C

Symbol	Parameter	Values	Unit
Vd12	HPA Drain bias voltage	18 to 25	V
Vg12	HPA Gate bias voltage	-5.0	V
VdL	Drain bias voltage	4	V
VgL	Gate bias voltage	4	V
IdL	LNA drain quiescent bias current	60	mA
SW	Switch Control voltage	20	V
Pin	Maximum Input power	-3	dBm

[5] Electrical performances are defined for specified test conditions
[6] Electrical performances are not guaranteed over all recommended operation conditions

Temperature Range

Tc	Operating temperature range (QFN backside)	-40 to +85	°C
Tstg	Storage temperature range	-55 to +150	°C

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Biasing procedure

Mode 1 – Tx mode

Device Power Up instructions:

HPA & Switch

1. Ground the device: I_{D12}= 0A
2. Set Vg12 to -5.0V: I_{D12}= 0A
3. Set Vd12 to 0V *(pinch off test)* : I_{D12}= 0A
4. Set Vd12 to 25V *(nominal bias voltage)* : I_{D12}= 0A
5. Set SW to 0V

Driver

1. Set Vg1d & Vd1d & Vg2d & Vd2d to 0V *(pinch off test):* I_{dd}= 0A/ I_{gd}= 0A
2. Set Vg1d & Vd1d & Vg2d & Vd2d to 4V *(nominal bias voltage):* I_{dd}=130mA/ I_{gd}= 8mA
   N.B: in order to protect the product, please to bias:
   - at the same time the 4 accesses,
   - or, in first, the drain accesses, then to increase slowly Vg1d & Vg2d up to 4V
3. Increase slowly Vg12 up to quiescent bias drain current I_{D12} = 40mA
4. Apply RF input power

Device Power Down instructions:

1. Remove RF input power
2. Decrease Vg12 down to -5.0V
3. Decrease Vg1d & Vd1d & Vg2d & Vd2d down to 0V
   N.B: in order to protect the product, please to bias:
   - at the same time the 4 accesses,
   - or, in first, the drain accesses, then to decrease slowly Vg1d & Vg2d down to 0V
4. Remove SW
5. Decrease Vd12 down to 0V

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Biasing procedure

Mode 2 – Rx mode

Device Power Up instructions:

HPA & Switch

1. Ground the device
2. Set SW to 20V
3. Set Vg12 to -5V: I_{D12}= 0A
   Vd12 = 25V

LNA

1. Set Vg1L & VdL to 0V *(pinch off test)*
2. Set Vg1L &VdL to 4V *(nominal bias voltage)*
   N.B: in order to protect the product, please to bias:
   - at the same time the 2 accesses,
   - or, in first, VdL, then to increase slowly Vg1L up to 4V
3. Apply RF input power

Device Power Down instructions:

1. Remove RF input power
2. Decrease Vg1L & VdL down to 0V
   N.B: in order to protect the product, please to bias:
   - at the same time the 2 accesses,
   - or, in first, the drain accesses, then to decrease slowly Vg1L down to 0V
3. Remove SW

Notes:

It is possible to begin the test measurement with Mode 1 or Mode 2.
In order to reduce DC biasing, be sure to
- in case of Mode 2 / Rx mode use:
  set HPA Vg12 to -5V, decrease Vd12 to 0V and set Vg12 to 0V
  set Driver Vg1d, Vg2d & Vd1d, Vd2d to 0V
- in case of Mode 1 / Tx mode use:
  set LNA Vg1L & VdL to 0V

CHC6054-QQA could be used on only one mode in the same time

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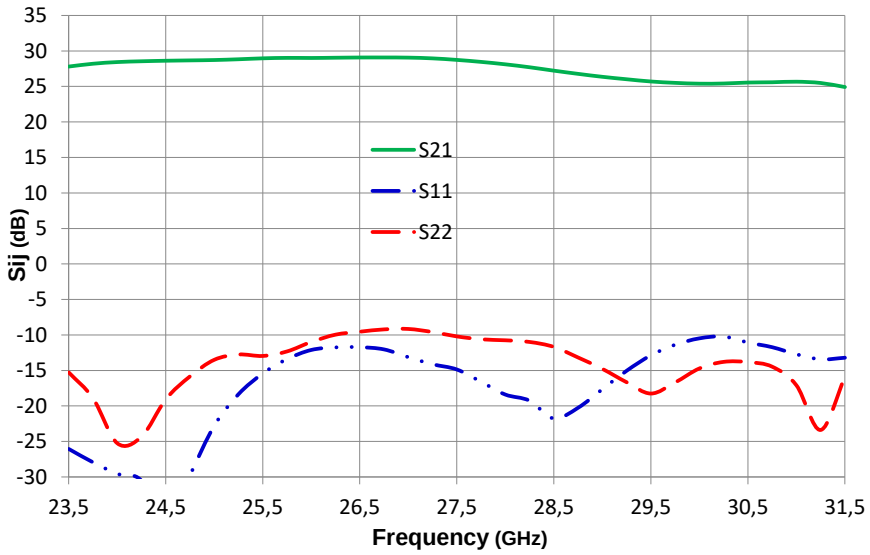
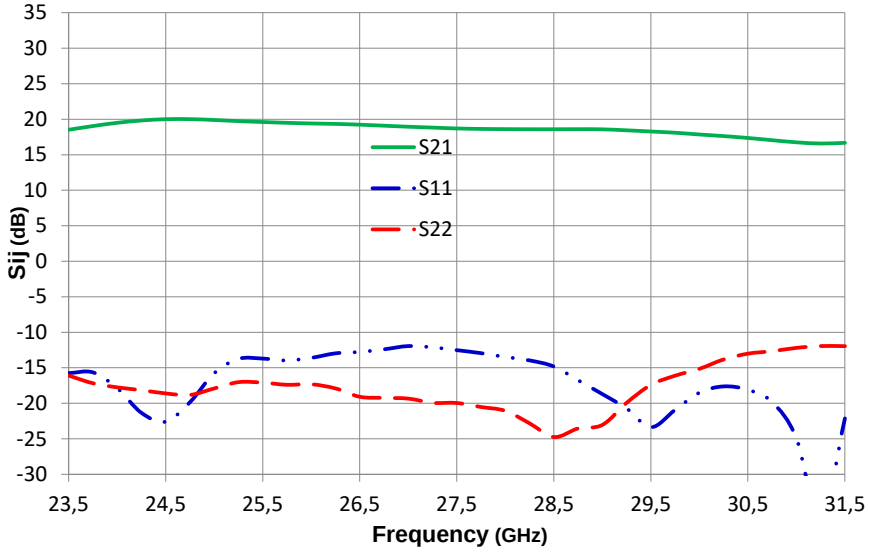
Typical Board Measurements

Tamb.= +25°C
Losses due to board are de-embedded. Measurements are given in the QFN access plan

Gain & Return Losses versus Frequency – TX Mode
Vd12 = +25V, Vg12 set in order to get Id12 = 40mA
SW = 0V, VdL=Vg1L=0V, Vd1d = Vd2d = Vg1d = Vg2d = 4V



Gain & Return Losses versus Frequency – RX Mode
Vd12 = +25V, Vg12 = -5V in order to ged Id12 = 0mA
SW = 20V, VdL=Vg1L=4V, Vd1d = Vd2d = Vg1d = Vg2d = 0V



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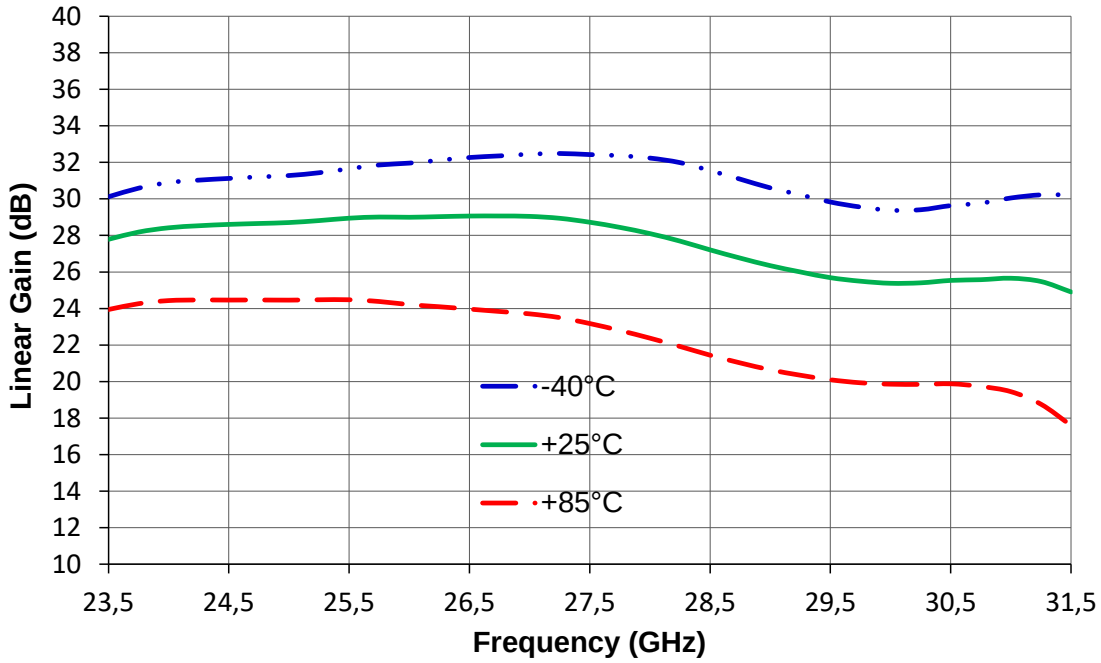
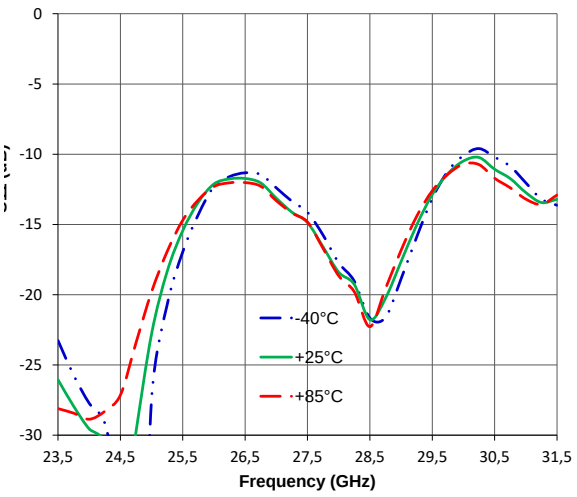
Typical Board Measurements – TX MODE

Tamb.= +25°C, SW = 0V, Vd12 = 25V, Vg12 set in order to get Id12 = 40mA
Vd1d = Vd2d = Vg1d = Vg2d = 4V, VdL=Vg1L=0V
Losses due to board are de-embedded. Measurements are given in the QFN access plan

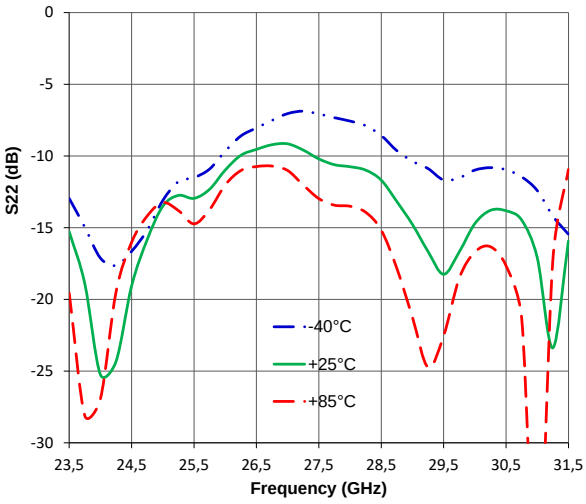
Gain versus Frequency in Temperature



Input Return Losses versus Frequency in Temperature



Output Return Losses versus Frequency In Temperature



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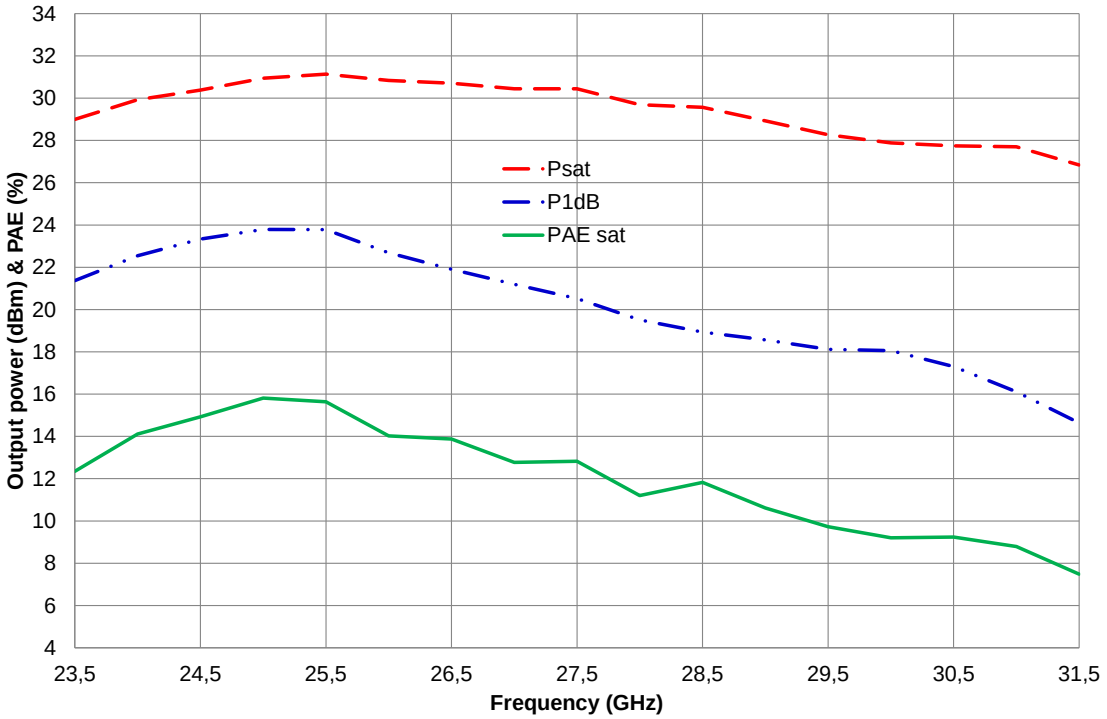
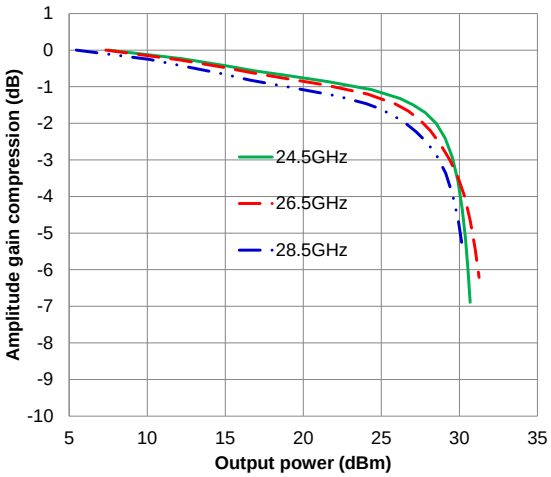
Typical Board Measurements – TX MODE

Tamb.= +25°C, SW = 0V, Vd12 = 25V, Vg12 set in order to get Id12 = 40mA
Vd1d = Vd2d = Vg1d = Vg2d = 4V, VdL=Vg1L=0V
Losses due to board are de-embedded. Measurements are given in the QFN access plan

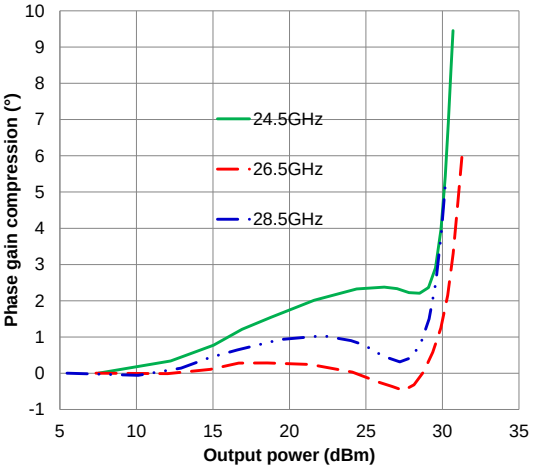
Output Power & PAE versus Frequency



Gain Amplitude versus Output Power



Gain Phase versus Output Power



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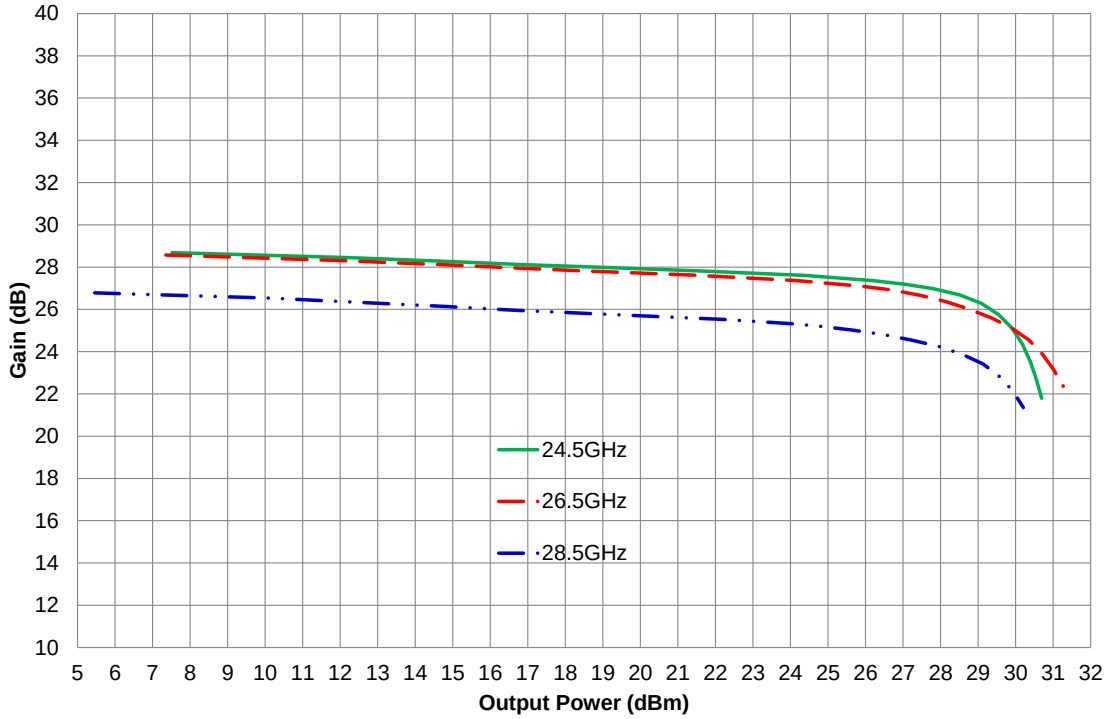
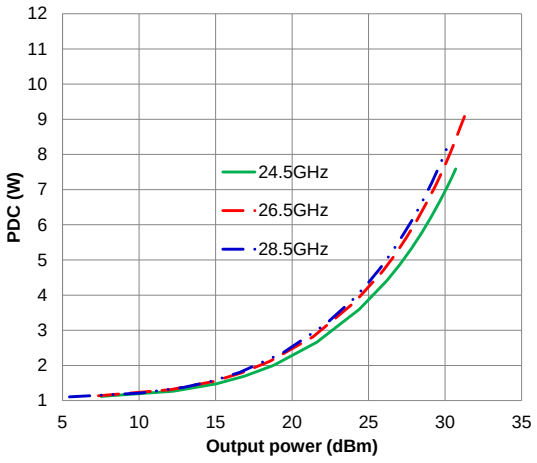
Typical Board Measurements – TX MODE

Tamb.= +25°C, SW = 0V, Vd12 = 25V, Vg12 set in order to get Id12 = 40mA
Vd1d = Vd2d = Vg1d = Vg2d = 4V, VdL=Vg1L=0V
Losses due to board are de-embedded. Measurements are given in the QFN access plan

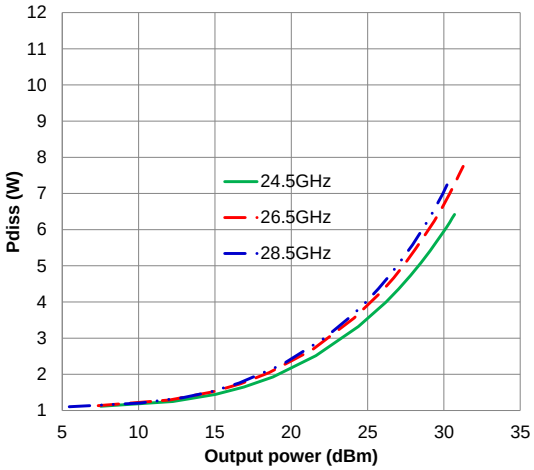
Gain versus Output Power



DC Power Consumption versus Output Power



Dissipated Power versus Output Power



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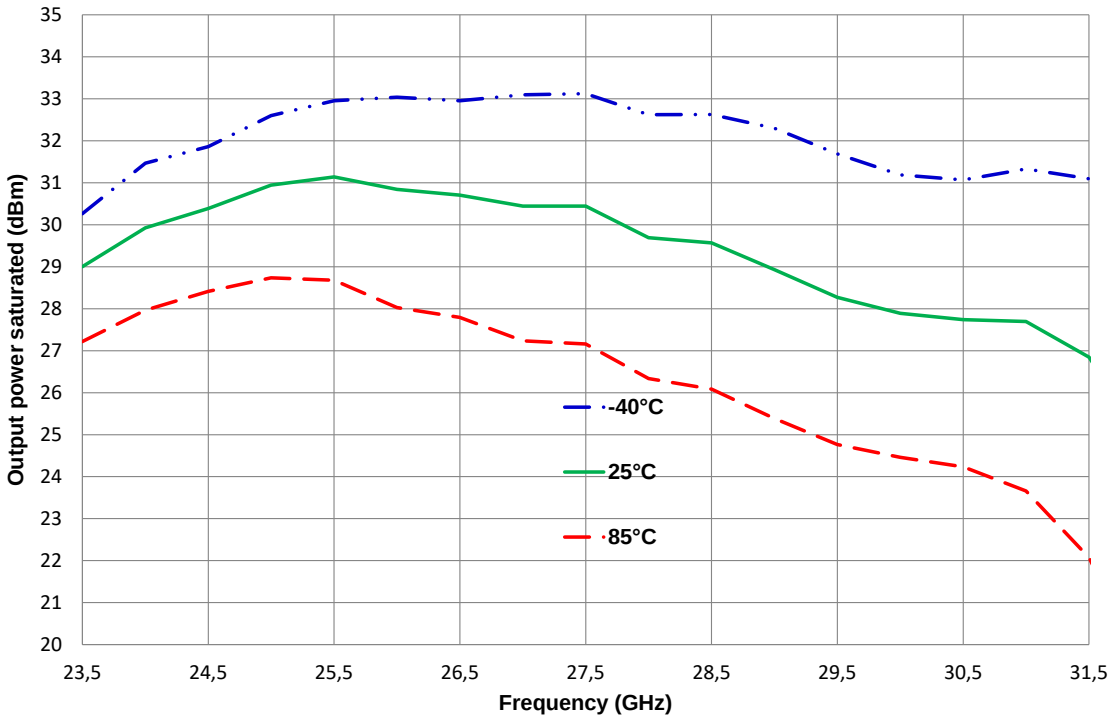
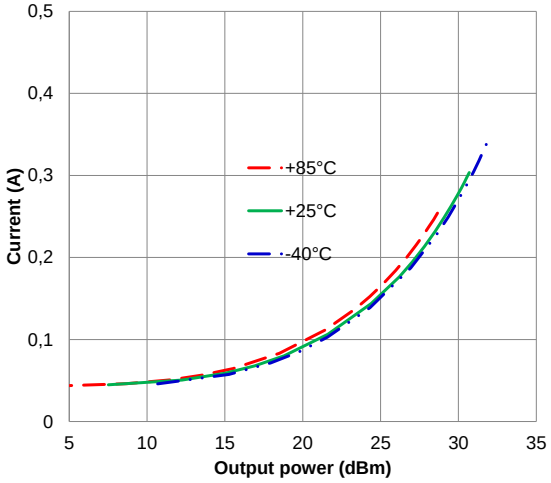
Typical Board Measurements – TX MODE

SW = 0V, Vd12 = 25V, Vg12 set in order to get Id12 = 40mA
Vd1d = Vd2d = Vg1d = Vg2d = 4V, VdL=Vg1L=0V
Losses due to board are de-embedded. Measurements are given in the QFN access plan

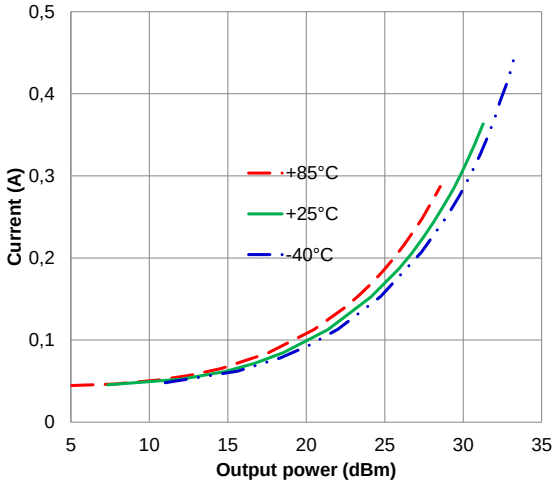
Output Power saturated versus Frequency in Temperature



HPA Drain Current versus Output Power @24.5GHz



HPA Drain Current versus Output Power @26.5GHz



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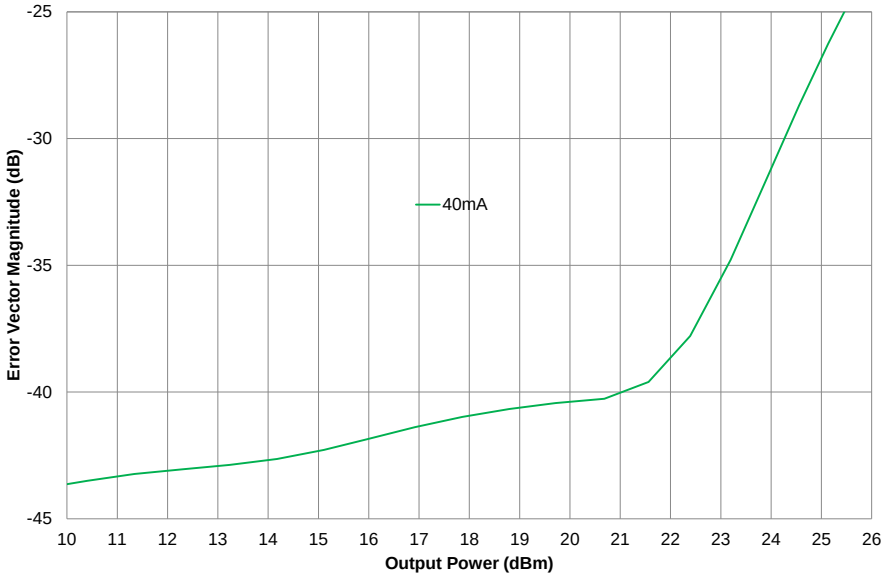
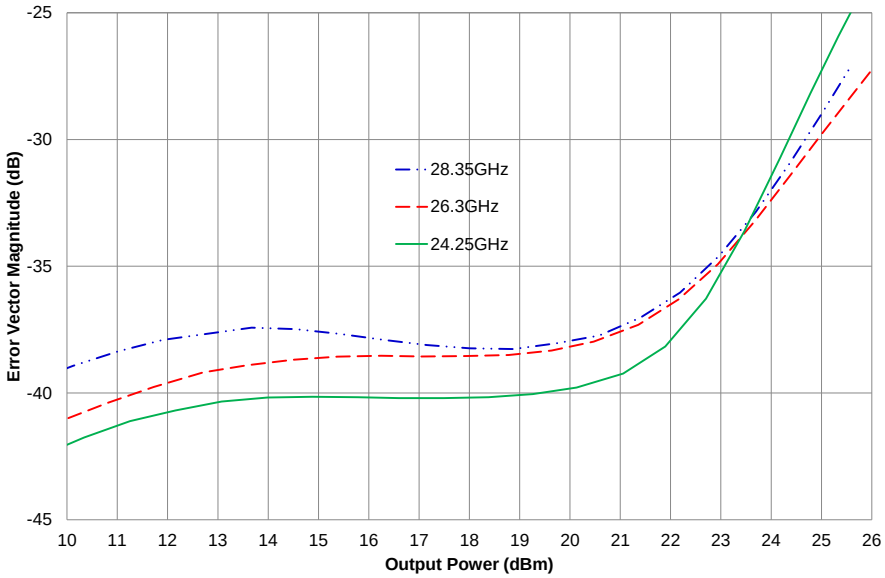
Typical Board Measurements – TX MODE

Tamb.= +25°C, SW = 0V, Vd12 = 25V, Vg12 set in order to get Id12
Vd1d = Vd2d = Vg1d = Vg2d = 4V, VdL=Vg1L=0V ; QAM Modulation **without DPD**
Losses due to board are de-embedded. Measurements are given in the QFN access plan

Error Vector Magnitude versus Output Power and Idq
RF_Freq = 24.25GHz ; Channel Spacing =56MHz, 4QAM



Error Vector Magnitude versus Output Power and RF Frequency
Idq = 40mA ; Channel Spacing =56MHz, 4QAM



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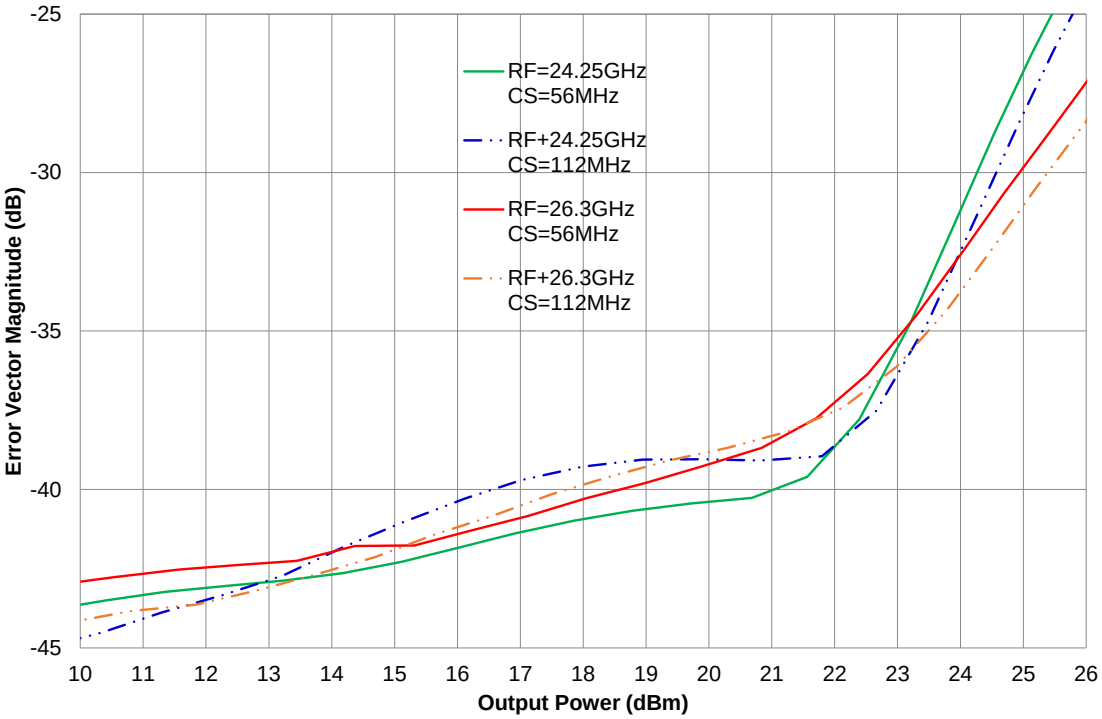
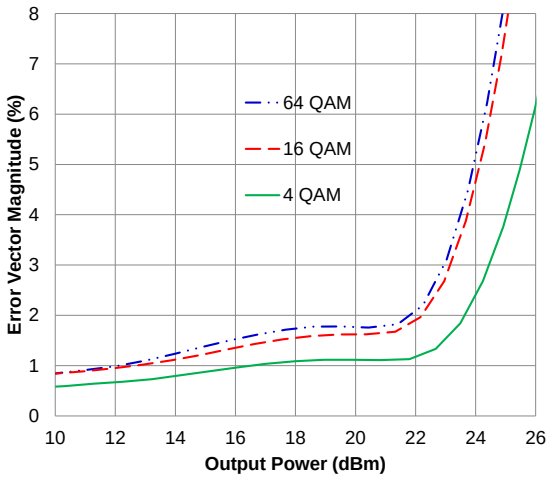
Typical Board Measurements – TX MODE

Tamb.= +25°C, SW = 0V, Vd12 = 25V, Vg12 set in order to get Id12 = 40mA
Vd1d = Vd2d = Vg1d = Vg2d = 4V, VdL=Vg1L=0V ; QAM Modulation **without DPD**
Losses due to board are de-embedded. Measurements are given in the QFN access plan

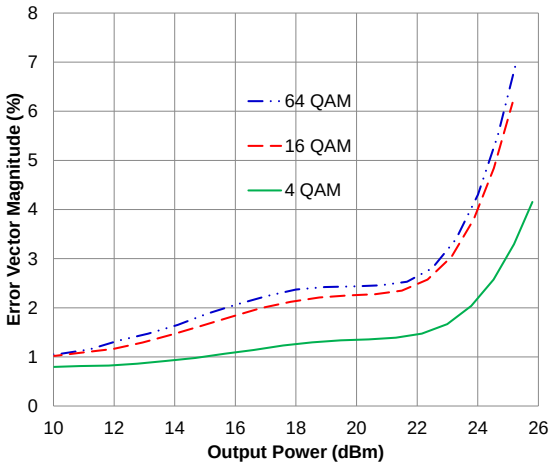
Error Vector Magnitude versus Output Power
RF_Freq = 24.25 & 26.3GHz ; Channel Spacing =56 & 112MHz, 4QAM



Error Vector Magnitude (%) versus Output Power @24.25GHz
Channel Spacing =112MHz



Error Vector Magnitude (%) versus Output Power @28.35GHz
Channel Spacing =112MHz



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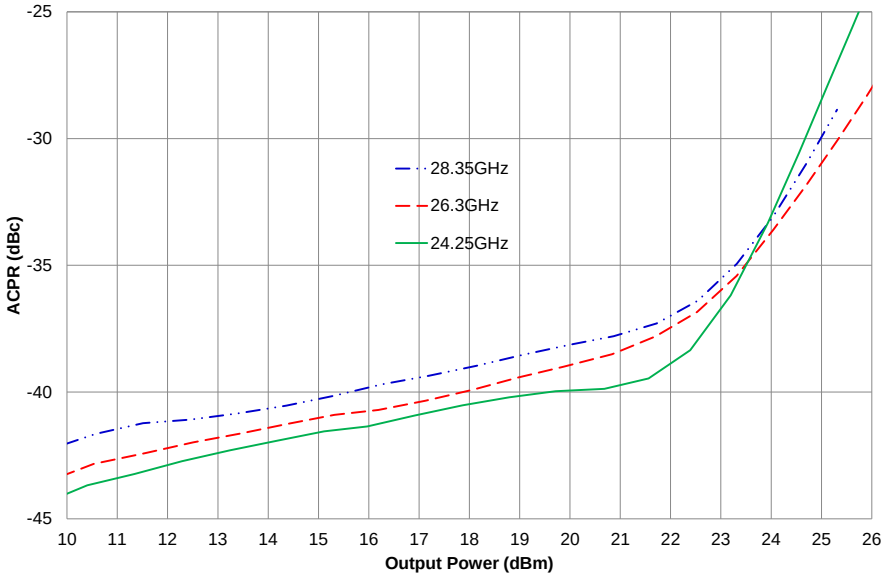
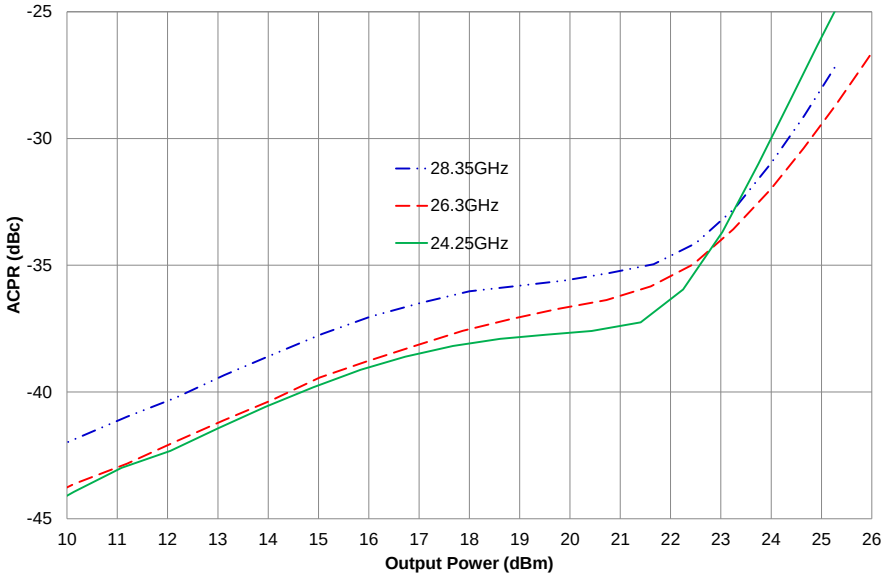
Typical Board Measurements – TX MODE

Tamb.= +25°C, SW = 0V, Vd12 = 25V, Vg12 set in order to get Id12 = 40mA
Vd1d = Vd2d = Vg1d = Vg2d = 4V, VdL=Vg1L=0V ; QAM Modulation **without DPD**
Losses due to board are de-embedded. Measurements are given in the QFN access plan

ACPR versus Output Power and RF Frequency
Channel Spacing =56MHz, 4QAM



ACPR versus Output Power and RF Frequency
Channel Spacing =112MHz, 64QAM



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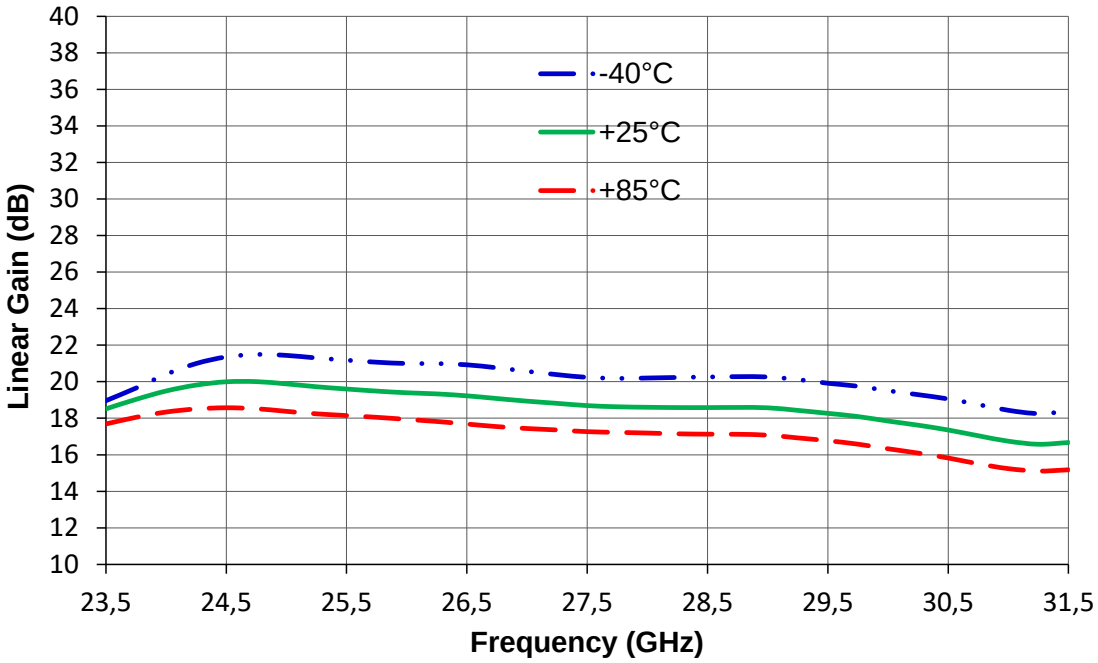
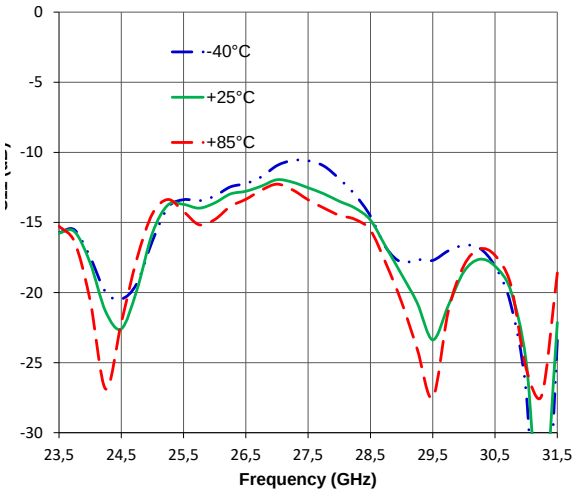
Typical Board Measurements – RX MODE

SW = +20V, Vd12 = 25V, Vg12 = -5V in order to get Id12 = 0mA
Vd1d = Vd2d = Vg1d = Vg2d = 0V, VdL=Vg1L=4V
Losses due to board are de-embedded. Measurements are given in the QFN access plan

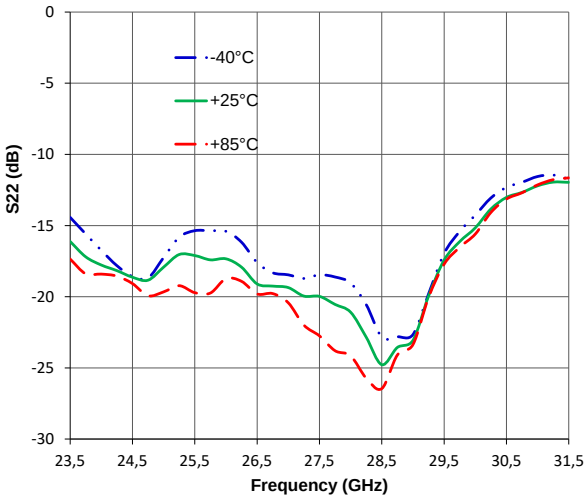
Gain versus Frequency in Temperature



Input Return Losses versus Frequency In Temperature



Output Return Losses versus Frequency In Temperature



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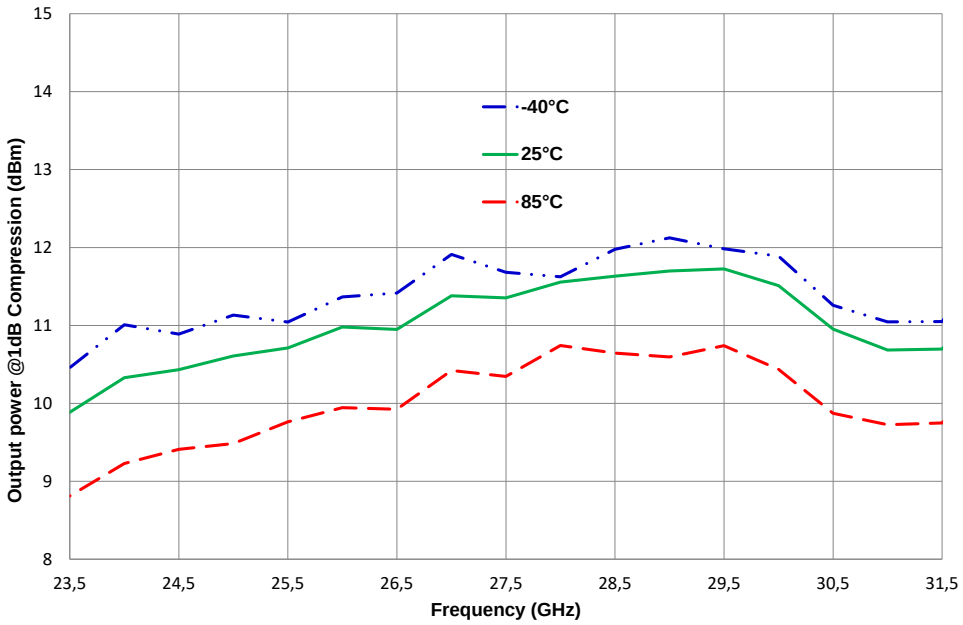
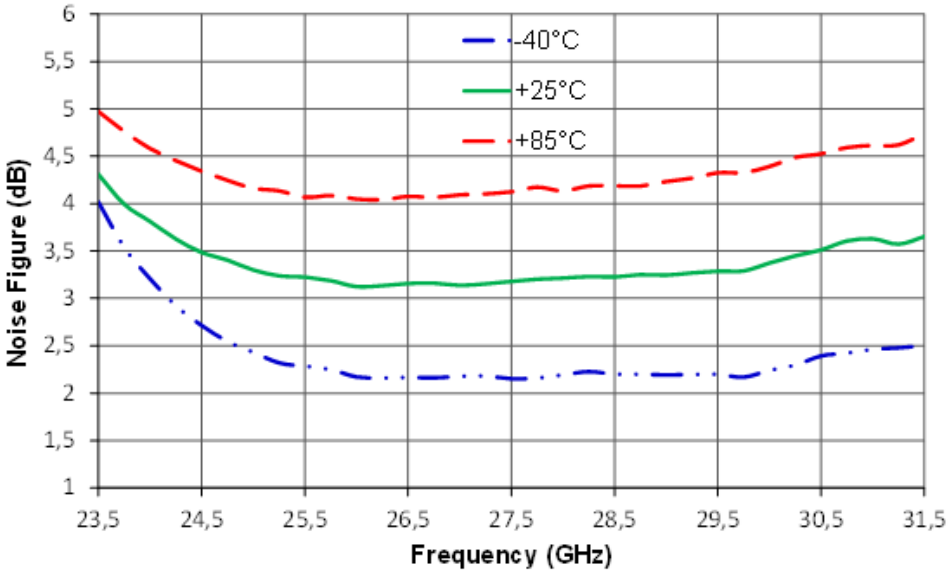
Losses due to board are de-embedded. Measurements are given in the QFN access plan

Output Power at 1dB compression versus Frequency in Temperature



Noise Figure versus Frequency in Temperature



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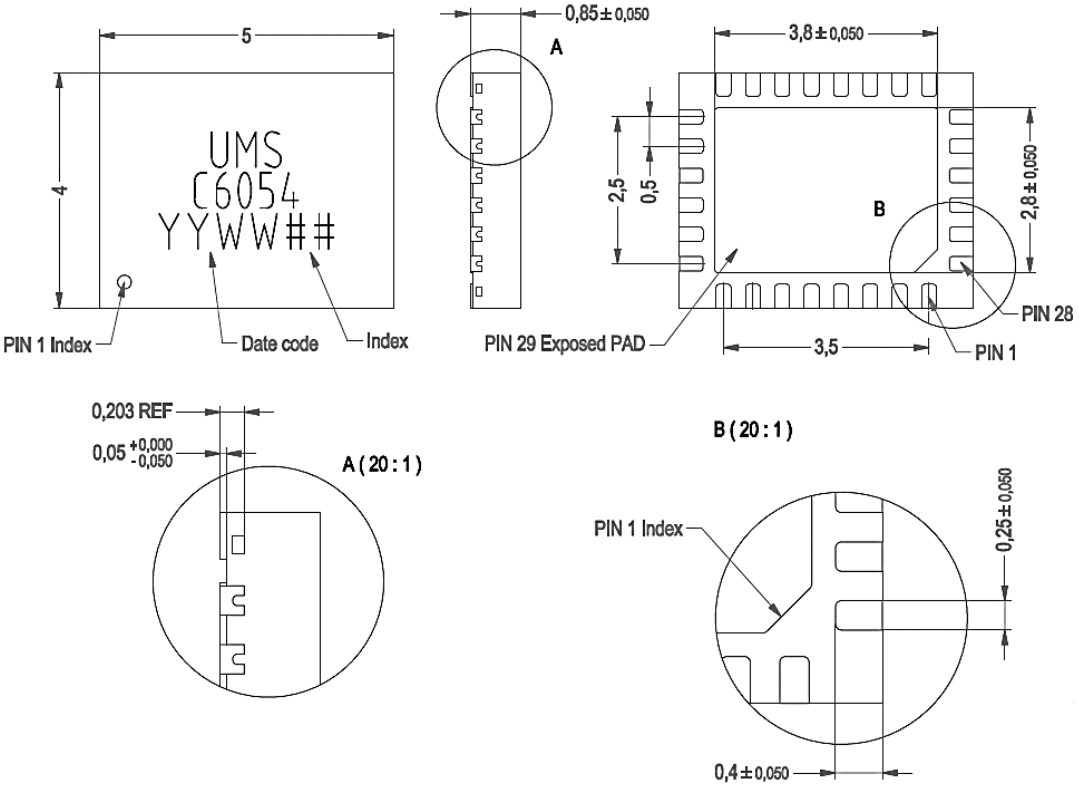
Package outline (1)



Matte tin, Lead Free (Green)	1- GND(2)	11- GND(2)	21- Vg12
Units : mm	2- Nc	12- GND(2)	22- Vd12
From the standard : JEDEC	3- SW	13- Input TX	23- GND(2)
MO-220	4- GND(2)	14- GND(2)	24- Nc
(VGGD)	5- Vg1L	15- Vg1d	25- GND(2)
29- GND	6- VdL	16- Vd1d	26- GND(2)
	7- GND(2)	17- Vg2d	27- Common
	8- Nc	18- Vd2d	28- GND(2)
	9- GND(2)	19- GND(2)	
	10- Output RX	20- GND(2)	

(1) The package outline drawing included to this document is given for indication. Refer to the application note AN0017 (https://www.ums-rf.com) for exact package dimensions.

(2) It is strongly recommended to ground all pins marked “GND” through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

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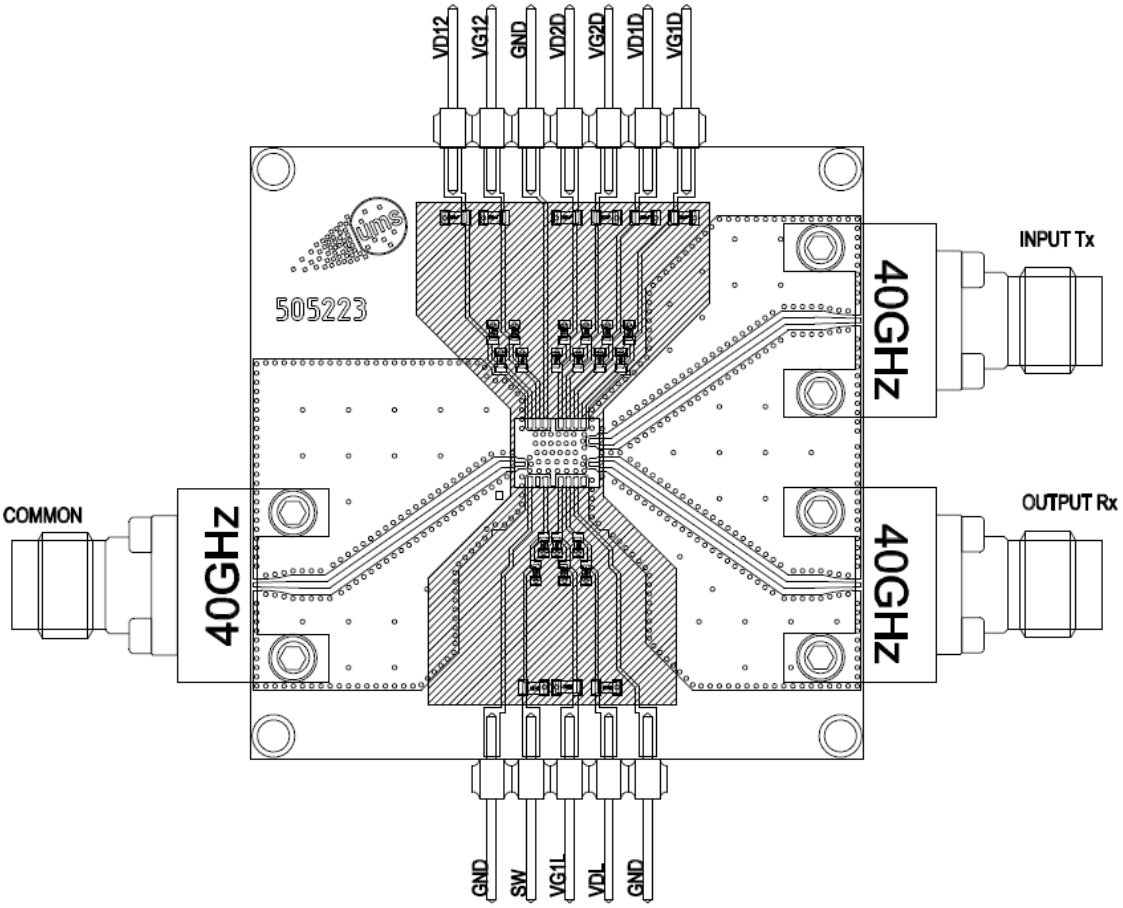
Evaluation mother board

Compatible with the proposed footprint.
■ Based on typically Ro4003 / 8mils or equivalent.
■ Using a micro-strip to coplanar transition to access the package.
■ Recommended for the implementation of this product on a module board.
■ Decoupling capacitors: 100pF ±5%, 10nF ±10% and 1µF ±10% are recommended for all DC accesses.
■ See application note AN0017 for details.



Note: All board measurements are performed using shielded cables, even for DC bias, to ensure safe operation.

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ESD Notes

ESD – Human Body Model (HBM)
Class 1A / 250 volts to < 500 volts (1) (2)

ESD – Machine Model (MM)
Class M1 / < 100 volts (1)
Class M2 / 100 volts up to 200 volts (2)

(1) from pin #22 (Vd12) ESDA / JEDEC JESD22-A114
(2) from pin #10 (Output_RX) ESDA / JEDEC JESD22-A115

The DC connections do not include any decoupling capacitor in package, therefore it is mandatory to provide a good external DC decoupling (100pF mandatory and 10nF & 1µF if possible) on the PC board, as close as possible to the package.

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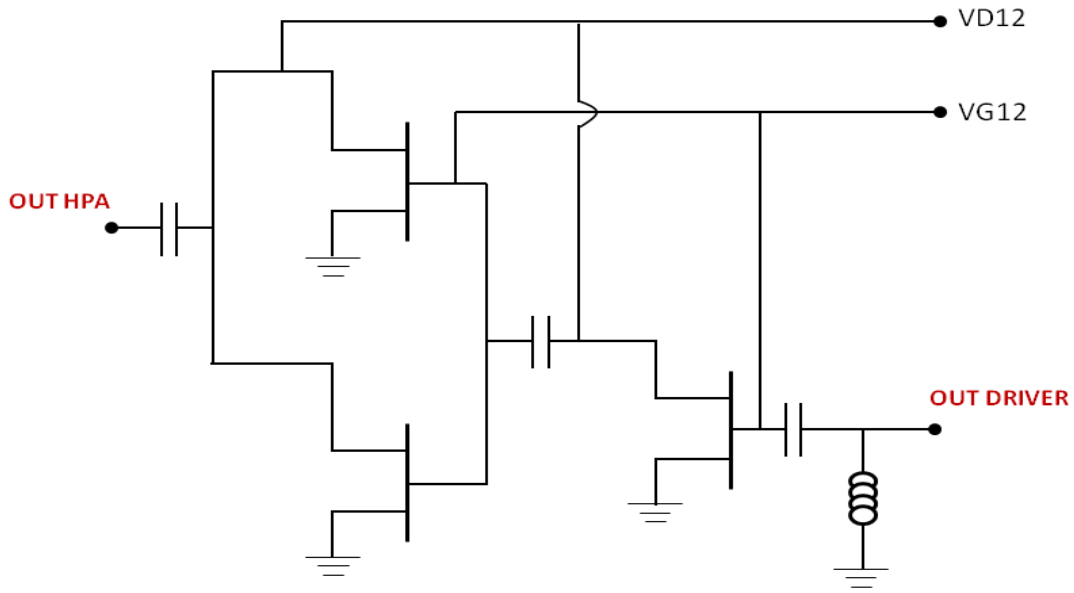
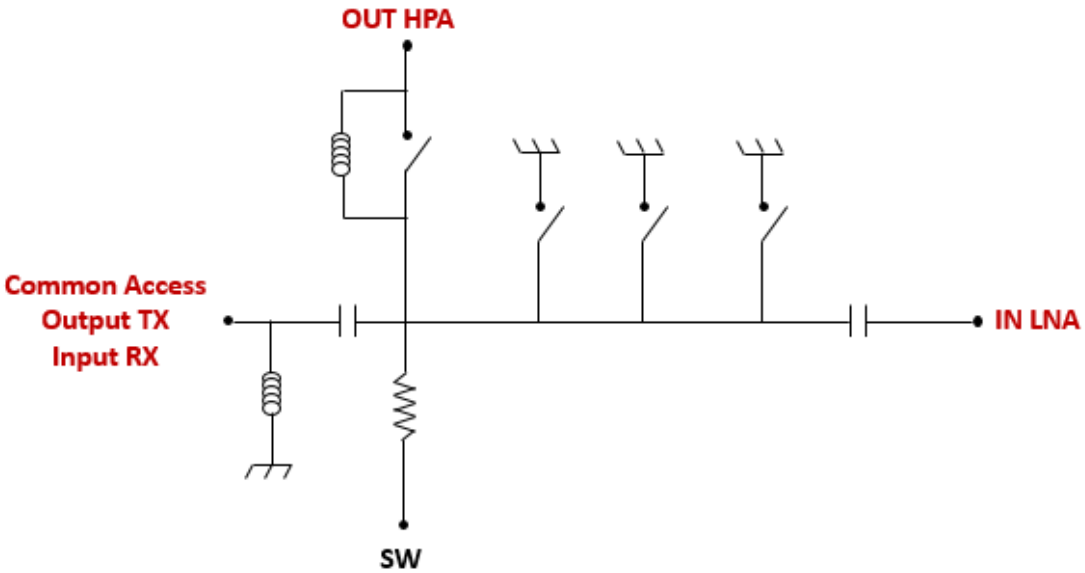
HPA DC Schematic



Vg12 # -3.1V, Vd12 = 25V, Id12 = 40mA

Switch DC Schematic



TX mode: SW = 0V
RX mode: SW = +20V

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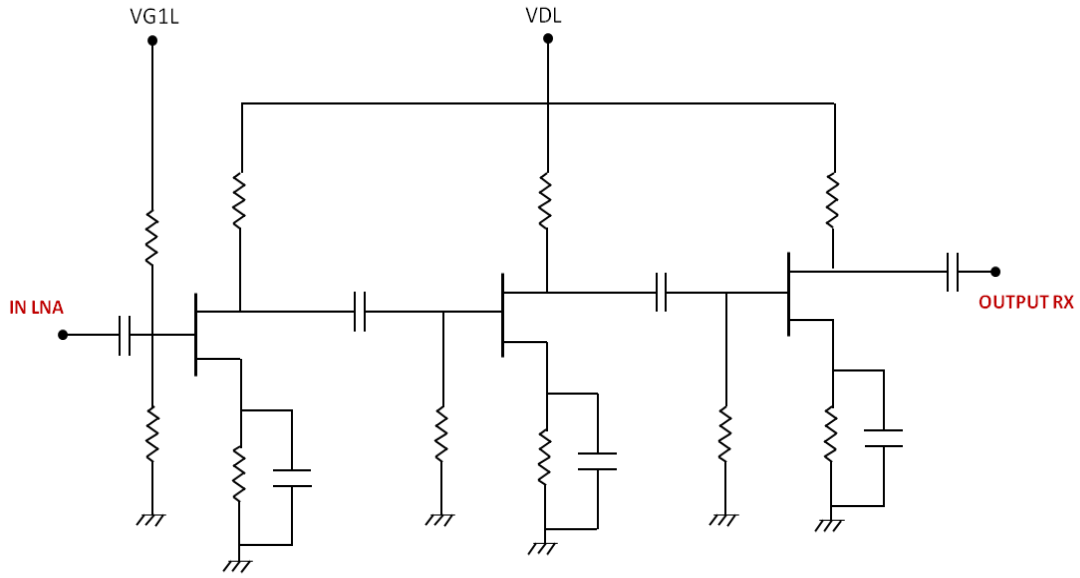
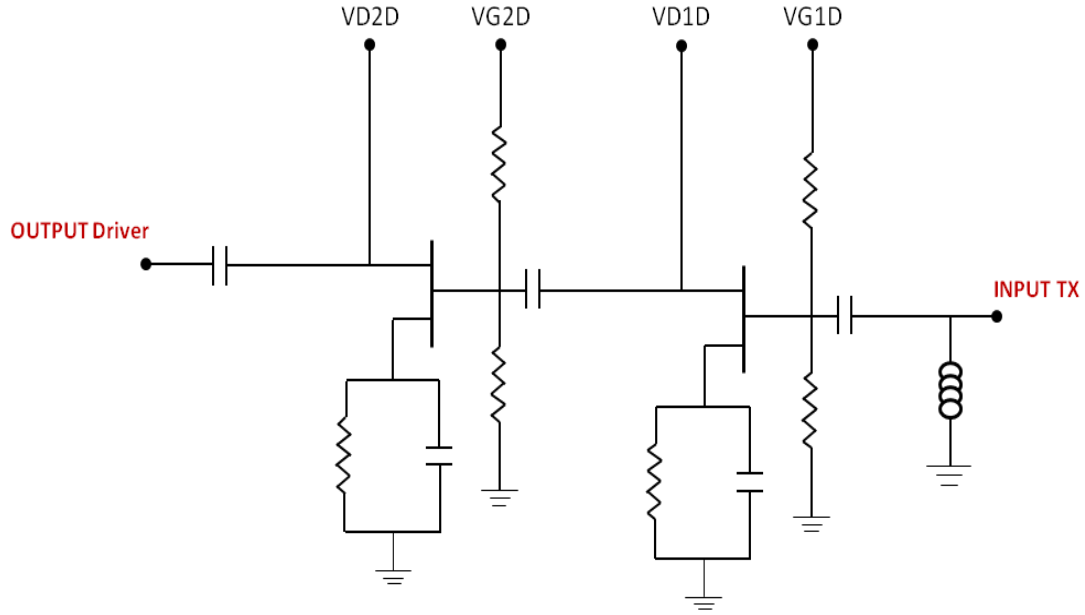
LNA DC Schematic



Vg1L = 4V, VdL = 4V, IdL = 60mA

Driver DC Schematic



Vd1d = Vd2d = 4V, Vg1d = Vg2d = 4V, Id12d = 130mA

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