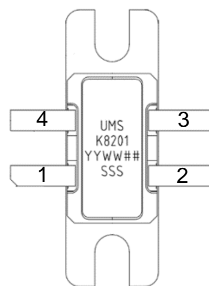
United Monolithic Semiconductors

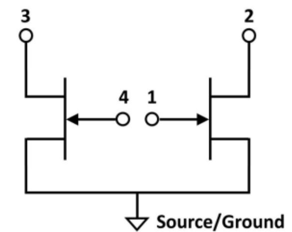
AI2010

Advanced Information: AI2010

45W GaN packaged power bar

GaN HEMT Microwave Transistor





Description

UMS developed an unmatched power bar microwave transistor, dedicated to RF power applications up to 4 GHz. It consists of two CHK8101a99F power bars packaged together with individual access possible.

The applied GaN on SiC process is a space evaluated HEMT process with 0.50 µm gate length.

It is supplied in a hermetic ceramic-metal flange power package, compliant with the RoHs N°2011/65 and REACH N°1907/2006 directives.

Main Electrical Characteristics

Tamb.= +25°C, V_D = +50V, I_{D_Q} = 200mA, freq. = 1.3 GHz, Pulsed mode

Symbol	Parameter	Min	Typ	Max	Unit
G_{SS}	Small signal gain		21		dB
P_{SAT}	Saturated output power		45		W
PAE	Power Added Efficiency		55		%
G_{PAE_MAX}	Associated Gain at Max PAE		14		dB

These values are representative of board measurements made in the connector's access planes.

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Recommended Operating Ratings (ROR)

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range			4	GHz
V_{DS}	Drain source voltage		50	50	V
V_{GS}	Gate source voltage		-1.9		V
I_{D_Q}	Quiescent drain current		200	640	mA
I_{G_MAX}	Gate Current (forward mode)		0	32	mA
T_{OP_CASE}	Case operating temperature range(1)	-40		85	°C
T_{j_MAX}	Junction temperature			200	°C

(1) Max junction temperature must be considered

Absolute Maximum Ratings (1,2) (AMR)

Tamb.= +25°C

Symbol	Parameter	Values	Unit
V_{DS}	Drain source biasing voltage	60	V
V_{GS}	Gate source biasing voltage (3)	-10 to +2	V
V_{GS}	Gate bias voltage	-2 to +0.4	V
I_{G_MAX}	Maximum Gate Current in Forward Mode	+64	mA
I_{G_MIN}	Maximum Gate Current in Reverse Mode	-4	mA
I_{D_MAX}	Maximum drain current	(4)	mA
Tj	Junction temperature	230	°C
Ta	Operating temperature range	See note (4)	°C
Tstg	Storage temperature range	-55 to +150	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage
(2) Duration < 1s
(3) Linked to and limited by I_{G_MAX} and I_{G_MIN} values. Maximum input power depends on frequency and should not exceed 2dB above PAE_{MAX}
(4) Max junction temperature must be considered

Biasing procedure

1. Bias power bar gate voltage at V_{GS} close to V_p (Typically: $V_{GS} \approx -5V$)
2. Apply V_{DS} bias voltage (Typically: $V_{DS} = 50V$)
3. Increase V_{GS} up to quiescent bias drain current I_{D_Q}

The quiescent current steady state must be carefully controlled as it is influenced by the operating mode, the temperature and the overall thermal resistance.
A drain current control is recommended on the biasing network.

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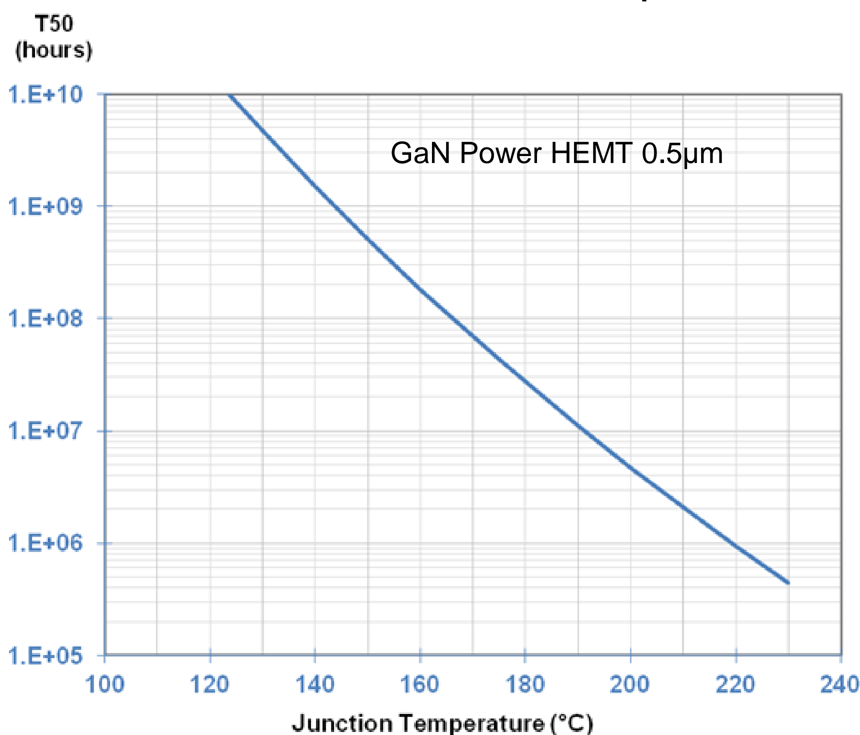
Device thermal information

The thermal performances of the device are based on UMS rules to evaluate the junction temperature (Tj). This temperature is defined as the peak temperature in the channel area. This same procedure is the basis for junction temperature evaluation of the samples used to derive the Median lifetime and activation energy for the particular technology on which the power bar is fabricated (GaN Power HEMT 0.5µm).
The temperature Tb is defined as the chip back side temperature
The thermal resistance (Rth) is given for the full power bar, in "equivalent" CW operating mode and in two different configurations as given in the table. The device assembly must be adapted to the operating mode. Thermal analysis is recommended. More information is available on request.

Parameters	Symbol	Conditions	Value	Unit
Typical Thermal Resistance	Rth	Bare die on carrier characteristic Tc = 100°C, Pdiss* = 25W , CW	2.88	°C/W
Junction Temperature	Tj		160	°C

The reference temperature (Tc) is defined on the carrier back side.
The power bar is mounted on package carrier plate (20µm Au/Sn soldering + 1.5mm Cu/Mo/Cu).

Median Life Time versus Junction Temperature



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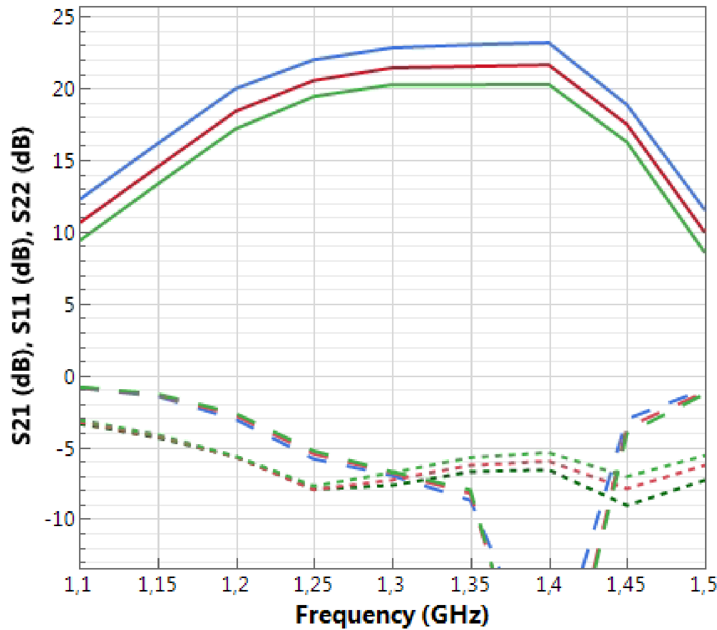
Typical Board Measurements

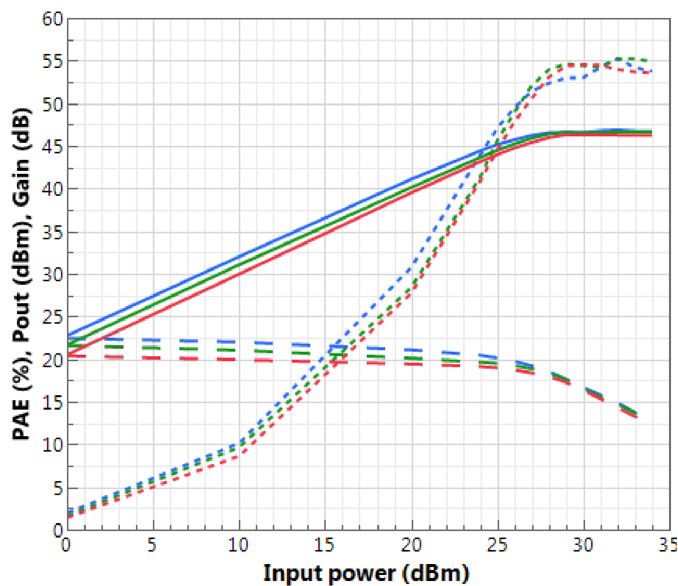
Vd = +50V, I_{D_Q} = 200mA

Gain (dB, – S_{21}), input (dB, – – S_{11}) & output (dB, - - S_{22}) return losses against frequency
(I_{D_Q} = 200 mA at 25°C)



Tcase ≈ -40°, +25; +85°C

PAE (%, --), Pout (dBm, –), and Gain (dB, – –) against input power
(f = 1.3GHz, I_{D_Q} = 200mA at 25°C)



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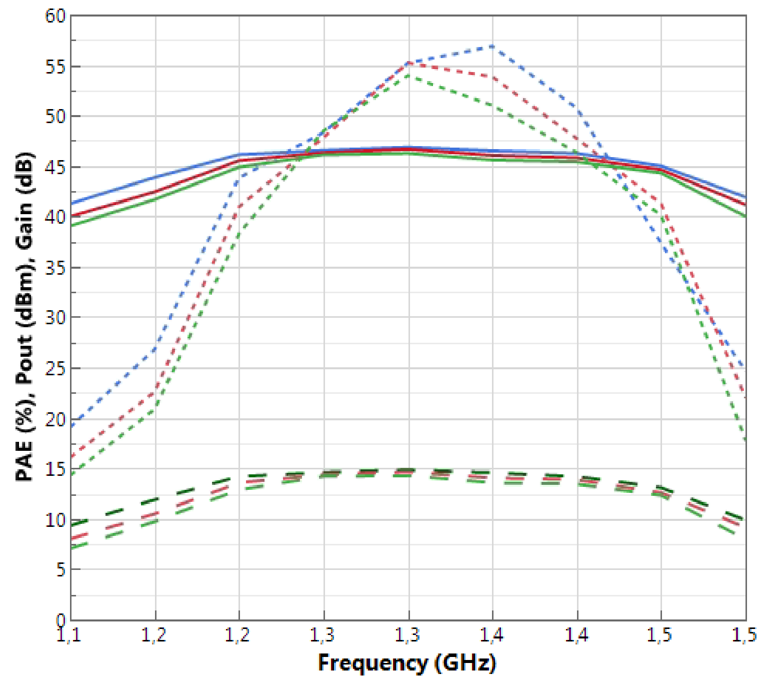
Typical Board Measurements

Vd = +50V, I_{D_Q} = 200mA

PAE (%, --), Pout (dBm, –), and Gain (dB, – –) against frequency
(Pin = 32 dBm, I_{D_Q} = 200 mA at 25°C)



Tcase ≈ -40°, +25; +85°C

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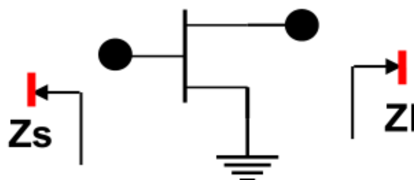
Simulated Source and Load Impedances

V_{DS} = +50V, I_{D_Q} = 200 mA, Tcase= +25°C



These values are given in the reference plane defined by the connection between the transistor leads and the PCB. The impedances are simulated in the package access planes, the two flanges of each package side being connected. A gap of 200µm is considered between the edge of the package and the PCB.

Frequency (MHz)	Zs (Ω)	Zl (Ω)	Pout (dBm)	PAE (%)
1000	2-j	6.4+j*15	46	77
2500	1.3-j*6.8	2.6+j*2.6	46	68.6
4000	5-j*16	1.5-j*3.2	45.9	43

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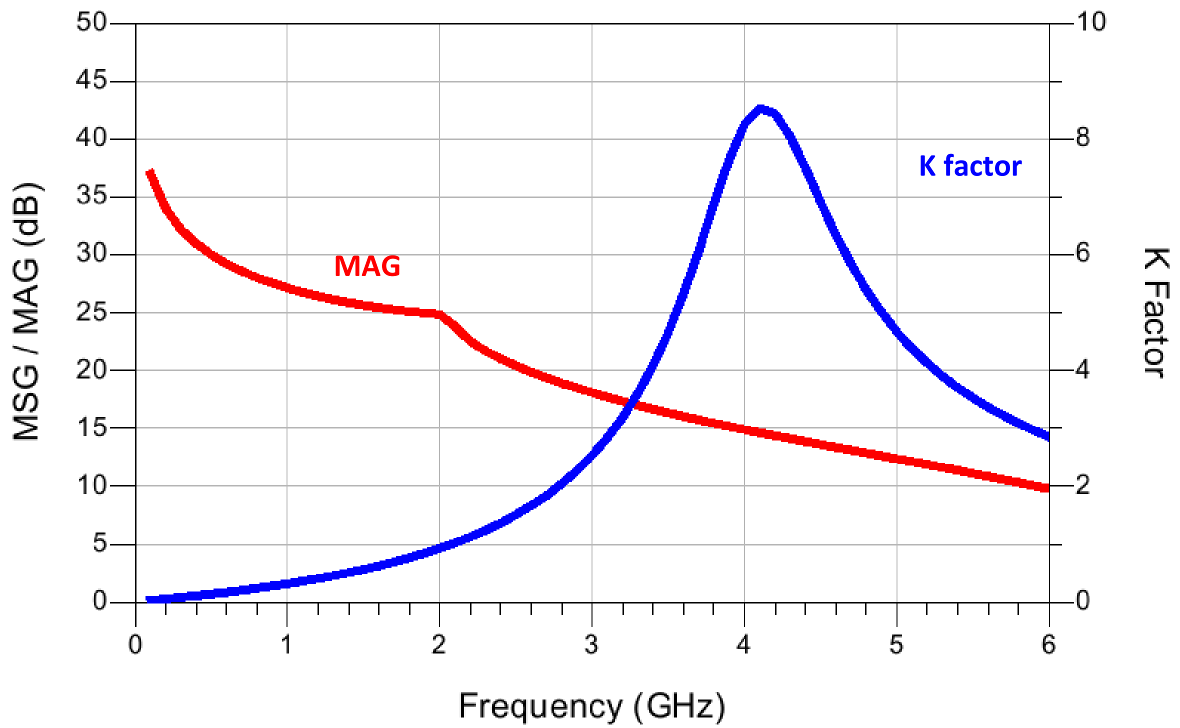
Simulated Maximum Gain & Stability Characteristics

V_{DS} = +50V, I_{D_Q} = 640mA, Tcase= +25°C



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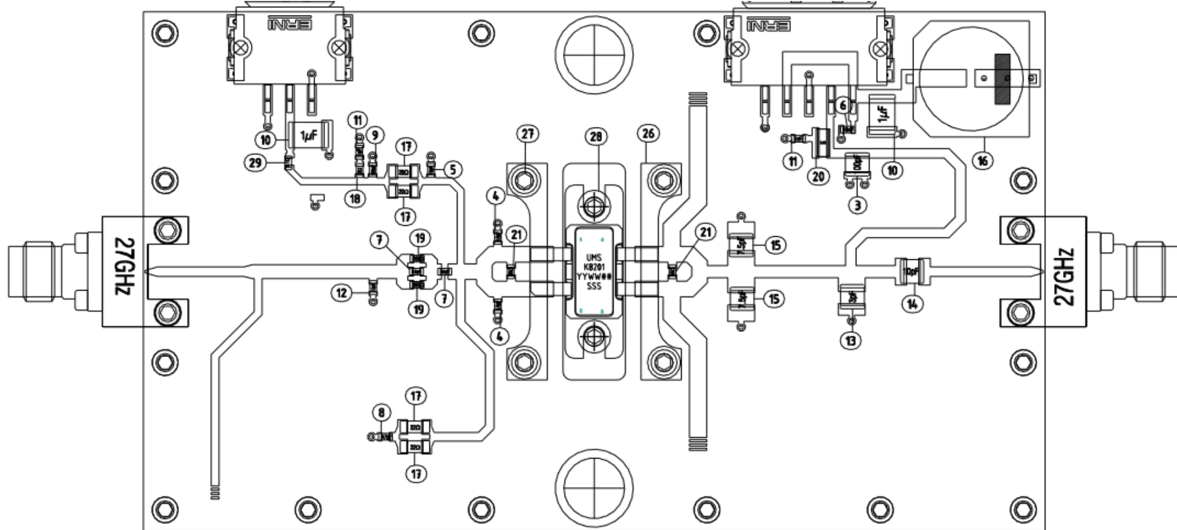
Demonstration board

The measurements of the component are performed on an evaluation board whose description can be found below. It is optimized for operation around 1.3 GHz.



Drawing reference	Quantity	SAP reference	Designation
1	1	61503717	Semelle Alu 104X60X7
2	1	61505027	Circuit EDG CHK8201-SYA
3	1	47003098	ATC100B 100pF 1111 500V 175°C
4	2	47002069	Condo 0603 3.9pF± 0.25pF 250V
5	1	47002075	Condo 0603 10pF± 5% 250V
6	1	47002501	Condo 0603 X7R 10nF ±10% 100V
7	2	47002077	Condo 0603 15pF± 5% 250V
8	1	47002086	Condo 0603 47pF± 5% 250V
9	1	47002090	Condo 0603 100pF± 5% 250V
10	2	47002101	Condo 1812 1µF±10% 100V
11	2	47002500	Condo 0603 COG 1nF ±5% 100V
12	1	47002076	Condo 0603 12pF± 5% 250V
13	1	47003102	Condo 1111 3pF± 10% 500V
14	1	47003096	ATC100B 10pF 1111 500V 175°C
15	2	47003094	ATC100B 7.5pF 1111 500V 175°C
16	1	47002274	Condo H13 68µF±20% 100V
17	4	47002246	RESIS MMA0204 22ohms ±1% 250mW
18	1	47002115	Resis 0603 3 Ohms±1% 0.1W
19	2	47002349	Resis 0603 200ohms ±1% 0.1W
20	1	47003035	RESIS 0612 3.3Ω ±1% 1W
21	2	47002119	Resis 0603 10 Ohms±1% 0.1W
22	1	47000882	Connect CMS angle male 3 cts
23	1	47000884	Connect CMS angle male 5 cts
24	2	47000875	Connecteur RF SMA (DC-27 GHz)
25	13	47000895	Vis CHc M1.6X6 A2
26	2	61498873	Presseur boitier
27	4	47002329	Vis CHc M2x10 A2
28	2	47000926	Vis CHc M2x6 A2
29	1	47002117	Resis 0603 5.1ohm ±1% 100mW

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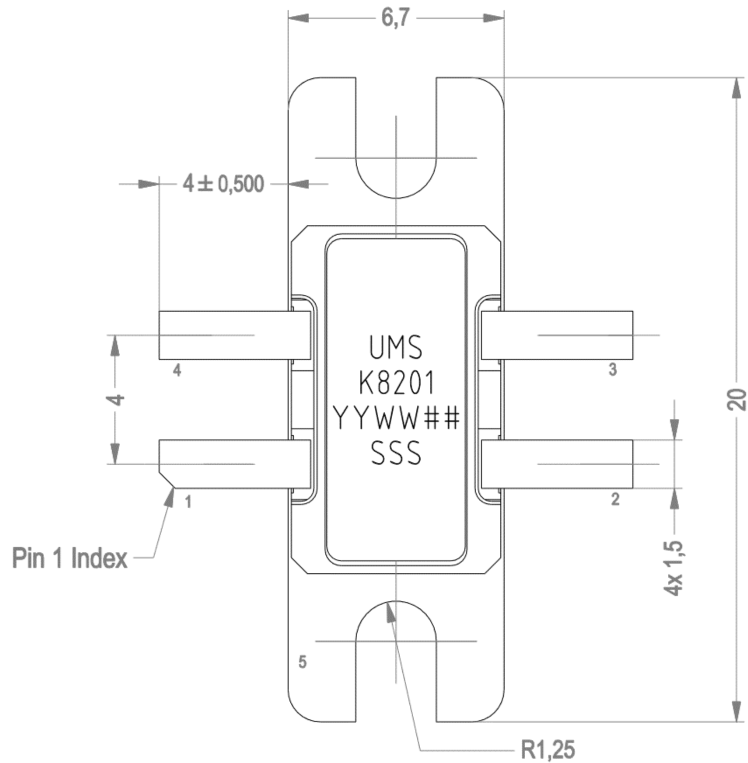
Package outline



Ni/Au finish on leads	1- Gate
Units : mm	2- Drain
	3- Drain
Ni/Au finish on leads	4- Gate
Ni/Au finish on Cu/Mo/Cu package	5- Gnd

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