United Monolithic Semiconductors

CHA4253-FAB

17- 21GHz Medium Power Amplifier

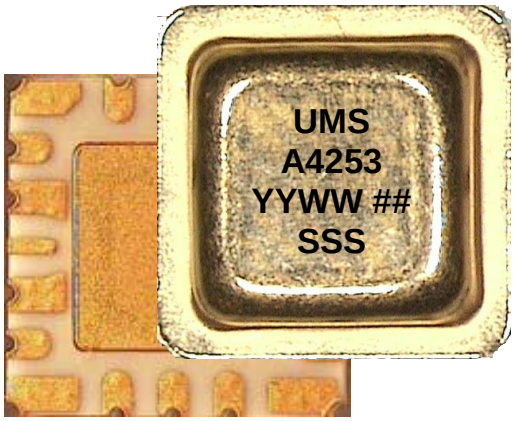
GaAs Monolithic Microwave IC in SMD Hermetic package

Description

The CHA4253-FAB is a four stage monolithic GaAs Medium Power Amplifier circuit delivering 23.5dBm output power at 1dB compression point.

It is designed for a wide range of applications, commercial space, military and commercial communication systems. The circuit is manufactured with an internal robust space evaluated 0.15µm gate length pHEMT process.

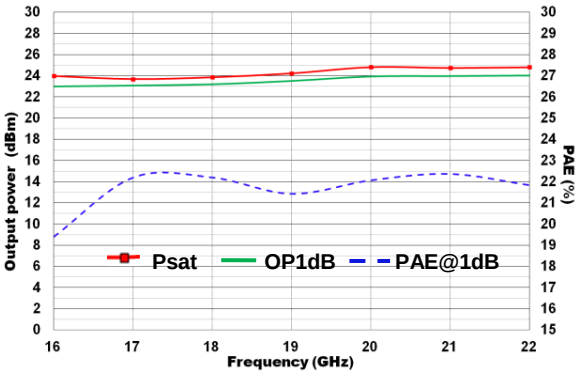
It is supplied in a hermetic package.



Main Features

- Broadband performances: 17- 21GHz
- 23.5dBm Pout for 1dB gain compression
- 26dB Linear Gain
- 33dBm Output IP3
- DC bias: Vd= 4.0V, Id= 230mA
- 20Leads-SMD
- 6x6mm² metal ceramic hermetic package

Output power & PAE versus Frequency



Main Electrical Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	17.0		21.0	GHz
Gain	Linear Gain		26		dB
P-1dB	Output Power @1dB comp.		23.5		dBm
OIP3	3rd order Intercept point		33		dBm

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Electrical Characteristics

Tamb.= +25°C, Vd = +4.0V

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	17.0		21.0	GHz
Gain	Linear Gain		26		dB
ΔG	Gain variation in temperature		0.05		dB/°C
OIP3	3rd order Intercept point		33		dBm
P_{-1dB}	Output power @ 1dB compression		23.5		dBm
Psat	Saturated Output Power		24.5		dBm
RLin	Input Return Loss		15		dB
RLout	Output Return Loss		12		dB
Id	Quiescent Drain current		230		mA
Vg	Gate voltage		-0.7		V
Tj	Junction temperature (1)			175	°C

These values are representative of onboard measurements as defined on the drawing in paragraph "Evaluation mother board".

(1) Duration < 1s.

Absolute Maximum Ratings (1)

Tamb.= +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	6	V
Id	Drain bias quiescent current	300	mA
Vg	Gate bias voltage	-2 to +0.4	V
Pin	Maximum input power	+10	dBm
Ta	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +150	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.

Typical Bias Conditions

Tamb.= +25°C

Symbol	Pad Nº	Parameter	Values	Unit
Vd12	2	DC Drain voltage 1st, 2nd stage	4	V
Vd34	4	DC Drain voltage 3rd, 4th stage	4	V
Vg12	14	DC Gate voltage 1st & 2nd stage	-0.7	V
Vg34	13	DC Gate voltage 3rd & 4th stage	-0.7	V

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Device thermal information

The device thermal performances below are based on UMS rules to evaluate the junction temperature.
This same procedure is the basis for junction temperature evaluation of the samples used to derive the Median lifetime and activation energy for the particular technology on which the CHA4253-FAB is manufactured (GaAs Power HEMT 0.15µm).
The temperature T_{case} is defined as the case back side. The thermal resistance (Rth_eq) is given for the full circuit, and assumes CW and pulsed operation mode are given in the table.

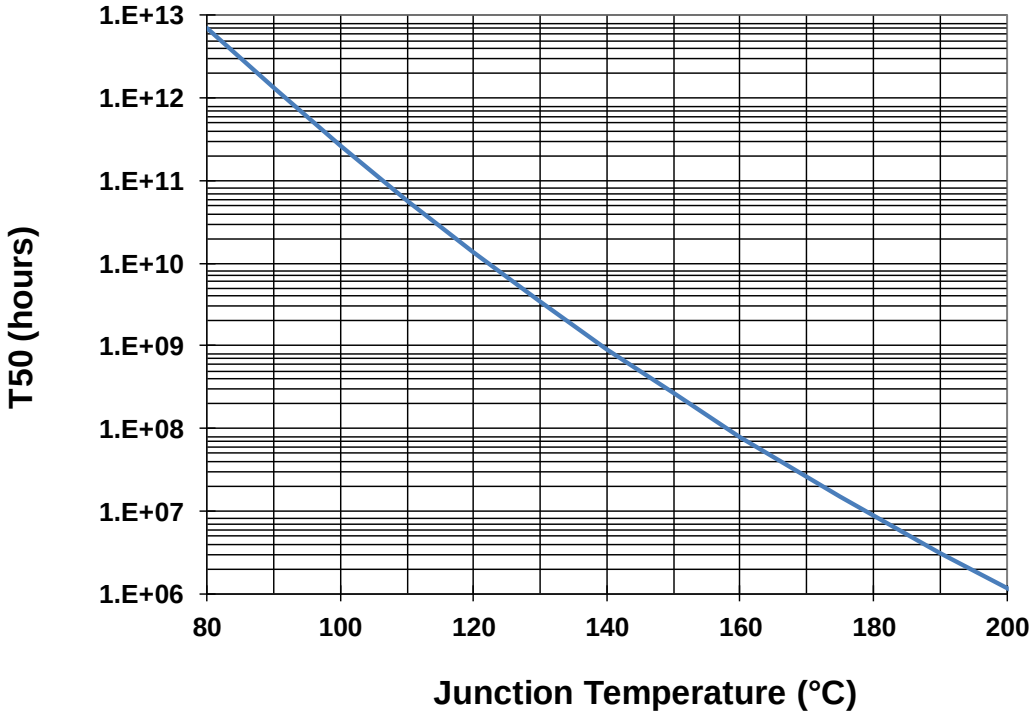
Thermal Resistance(1)	Rth_eq	Tb_{case} =85°C, Vd=4V, Id_drive=0.2A Pin=3dBm Pout=24dBm Pdiss=0.81W CW	40	°C/W
Junction Temperature	Tj		118	°C
Median Life	T50		$1.35x10^{10}$	Hrs

(1) Thermal resistance measured to back side of the package

Thermal Resistance(1)	Rth_eq	Tb_{case} =85°C, Vd=4V, Id_drive=0.23A Pin=7dBm Pout=24.4dBm Pdiss=0.9W CW	40	°C/W
Junction Temperature	Tj		122	°C
Median Life	T50		$1.35x10^{10}$	Hrs

(1) Thermal resistance measured to back side of the package

Median Life Time versus Junction Temperature



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Typical Package Sij parameters

Tamb.= +25°C, Vd = +4.0V, Idq = 230mA

Freq (GHz)	S11 (dB)	PhS11 (°)	S12 (dB)	PhS12 (°)	S21 (dB)	PhS21 (°)	S22 (dB)	PhS22 (°)
1	-0.61	144.35	-79.12	37.33	-75.75	55.63	-0.6	148.61
2	-0.75	108.35	-73.88	20.49	-72.01	14.68	-0.72	117.1
3	-0.92	71.87	-73.41	-13.71	-75.29	-48.81	-0.85	84.82
3.5	-1.01	53.16	-75.16	-2.23	-78.33	-51.23	-0.92	68.04
4	-1.12	34.08	-73.48	-28.91	-71.66	-175.38	-0.98	50.97
4.5	-1.3	14.57	-74.8	-51.86	-67.56	108.81	-1.05	33.43
5	-1.57	-4.96	-76.81	-65.63	-51.42	166.42	-1.1	15.49
5.5	-1.91	-23.62	-79.94	-77.69	-34.26	76.96	-1.15	-2.99
6	-2.11	-41.25	-77.03	-106.46	-27.2	-12.82	-1.2	-21.91
6.5	-2.25	-60.94	-82.67	-137.54	-23.3	-80.62	-1.23	-41.95
7	-2.32	-80.52	-92.75	-121.52	-20.02	-134.72	-1.27	-62.25
7.5	-2.42	-100.49	-83.61	-141.84	-16.84	177.08	-1.34	-83.31
8	-2.6	-120.68	-75.4	-135.15	-13.77	131.89	-1.5	-105.16
8.5	-2.83	-140.93	-66.67	-156.94	-10.81	88.47	-1.76	-128.08
9	-3.15	-161.27	-61.24	166.03	-8	46.02	-2.21	-152.24
9.5	-3.53	178.45	-59.32	116.75	-5.41	3.96	-2.9	-177.74
10	-4	157.97	-56.46	80.8	-3.17	-35.84	-3.74	155.01
10.5	-4.53	137.51	-61.13	38.87	-0.73	-75.81	-4.99	125.51
11	-5.15	116.93	-60.59	27.83	1.35	-115.27	-6.34	94.32
11.5	-5.85	95.76	-62.62	5.66	3.27	-153.78	-7.69	60.95
12	-6.66	74.46	-66.32	-18.92	5.08	169.14	-8.78	27.26
12.5	-7.57	52.72	-74.83	10.16	6.87	133.19	-9.47	-5.27
13	-8.62	30.54	-71.99	76.55	8.73	98.42	-9.79	-34.88
13.5	-9.79	7.8	-64.52	97.68	10.74	64.4	-9.91	-60.53
14	-11.13	-15.81	-56.96	84.48	12.99	30.21	-9.97	-83.6
14.5	-12.71	-39.7	-57.81	64.95	15.44	-5.08	-10.34	-106
15	-14.59	-63.57	-52.68	42.89	18.04	-41.93	-11.39	-128.08
15.5	-17.03	-84.95	-50.94	18.52	20.85	-80.98	-13.53	-148.14
16	-20.33	-98.91	-51.43	-3.31	23.82	-124.08	-18.12	-158.74
16.5	-19.58	-86.88	-50.59	-27.34	26.31	-171.68	-25.66	-89.92
17	-15.32	-102.15	-54.47	-33.56	28.22	137.56	-14.19	-77.31
17.5	-14.05	-143.96	-53.95	-26.21	29.61	82.07	-10	-110
18	-15.49	177.06	-49.91	-35.99	29.27	27.55	-9.59	-137.79
18.5	-18.61	154.01	-48.35	-52.82	28.29	-17.87	-11.03	-154.83
19	-22.88	161.01	-48.11	-81.7	27.55	-57.89	-13.44	-155.89
19.5	-19.93	171.37	-51.44	-96.78	27.23	-96.12	-13.5	-150.3
20	-16.93	154.97	-51.23	-117.4	27.34	-134.43	-11.93	-147.78
20.5	-17.09	135.91	-58.08	-135.02	27.21	-172.86	-11.77	-160.68
21	-16.25	125.97	-68.78	-44.57	27.49	149.37	-11.89	-159.27
21.5	-13.23	112.95	-50.53	-69.03	28.11	109.35	-9.86	-154.73
22	-12.24	85.3	-49.71	-98.32	28.18	66.17	-8.71	-172.06
22.5	-12.84	51.15	-51.93	-125.58	27.5	24.5	-9.39	171.13
23	-14.26	22.12	-55	-106.28	27.29	-13.42	-10.53	165.12
23.5	-16.98	-10.15	-53.06	-103.66	27.32	-51.06	-11.95	158.77
24	-20.23	-47.02	-51.66	-88.48	27.96	-91.82	-12.66	159.38
24.5	-21.57	-131.28	-49.36	-113.86	28.73	-136.57	-14.51	164.84
25	-16.37	162.45	-47.1	-107.05	29.22	174.26	-17.65	-177.8
25.5	-13.87	115.17	-46.43	-132.8	28.64	115.78	-15.81	-160.82
26	-12.31	86.14	-44.77	-137.61	26.78	59.33	-10.68	-152.64

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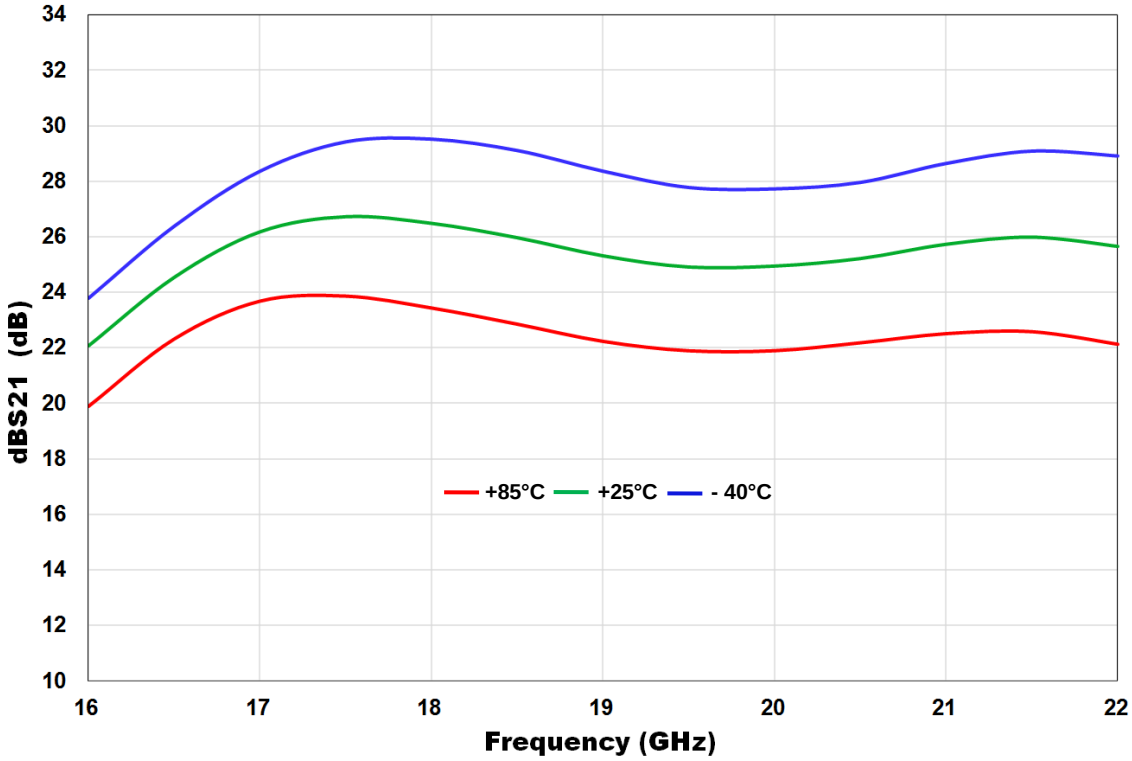
Typical Board Measurements

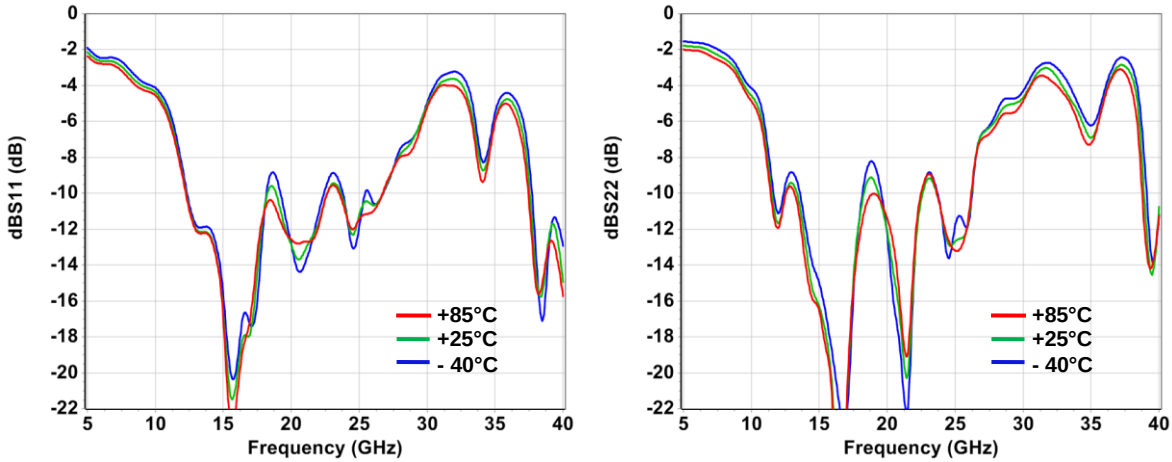
Vd = +4.0V. Idq = 230mA

These values are representative of onboard measurements as defined on the drawing in paragraph "Evaluation mother board". Measurements in the planes of the connectors. Board losses have been taken into account to plot the following measurements below.

Linear Gain versus Frequency in Temperature



Return losses versus Frequency in Temperature



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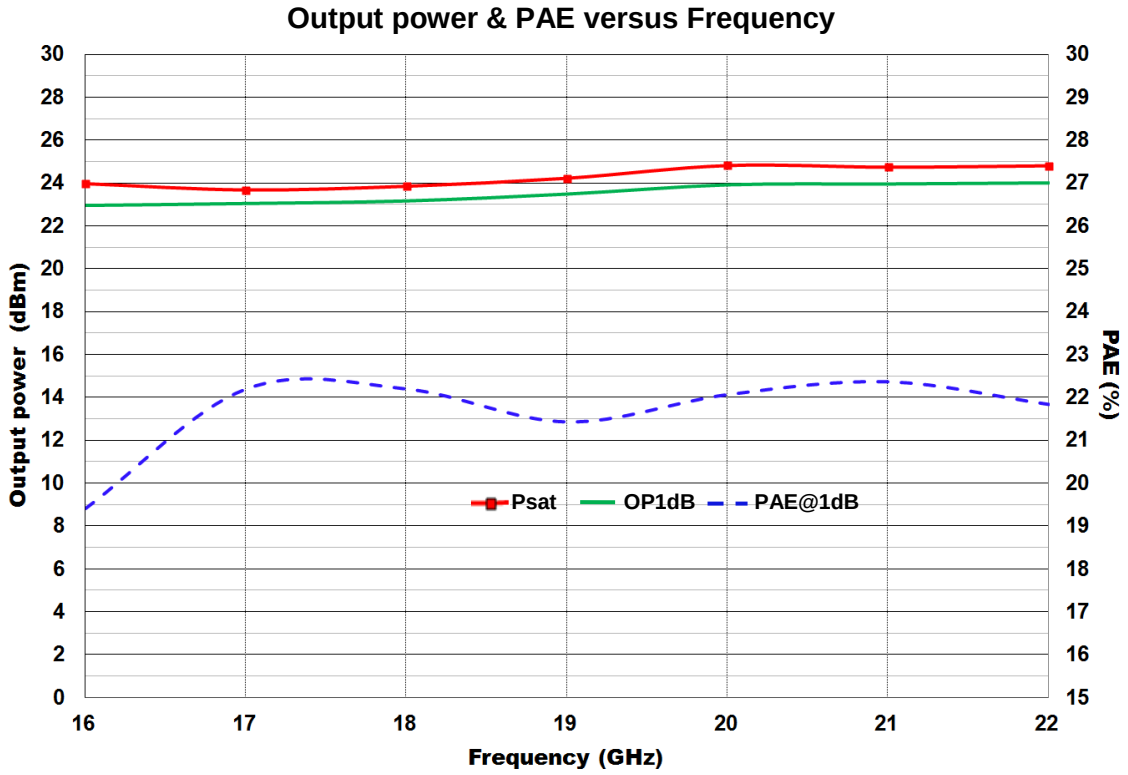
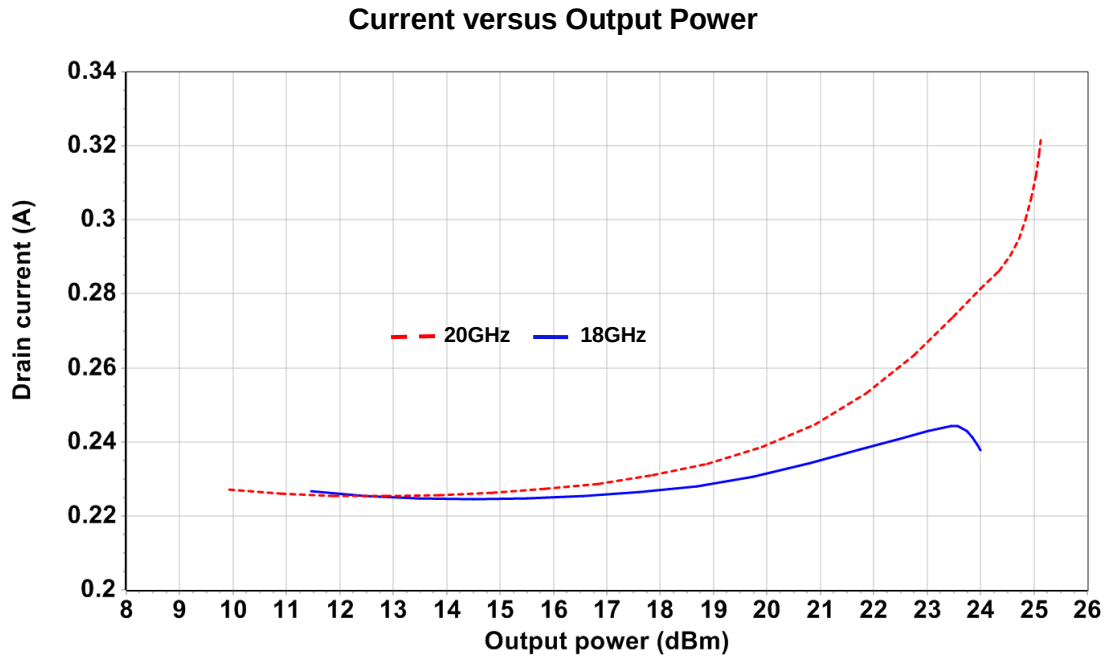
Typical Board Measurements

Tamb.= +25°C. Vd = +4.0V. Idq = 230mA. Measurements in packaging planes.





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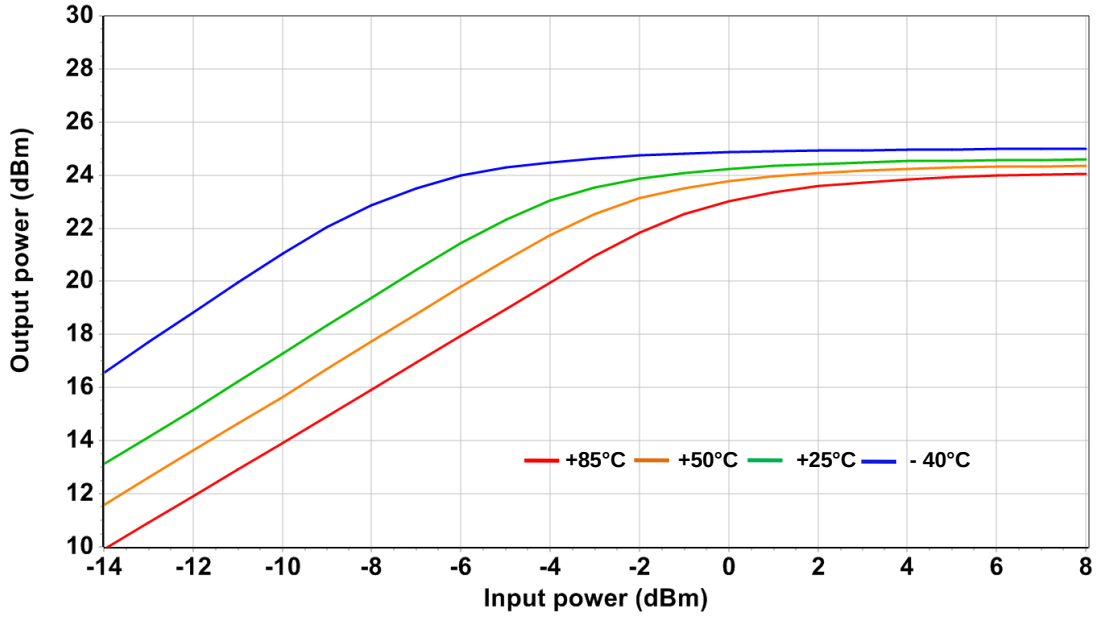
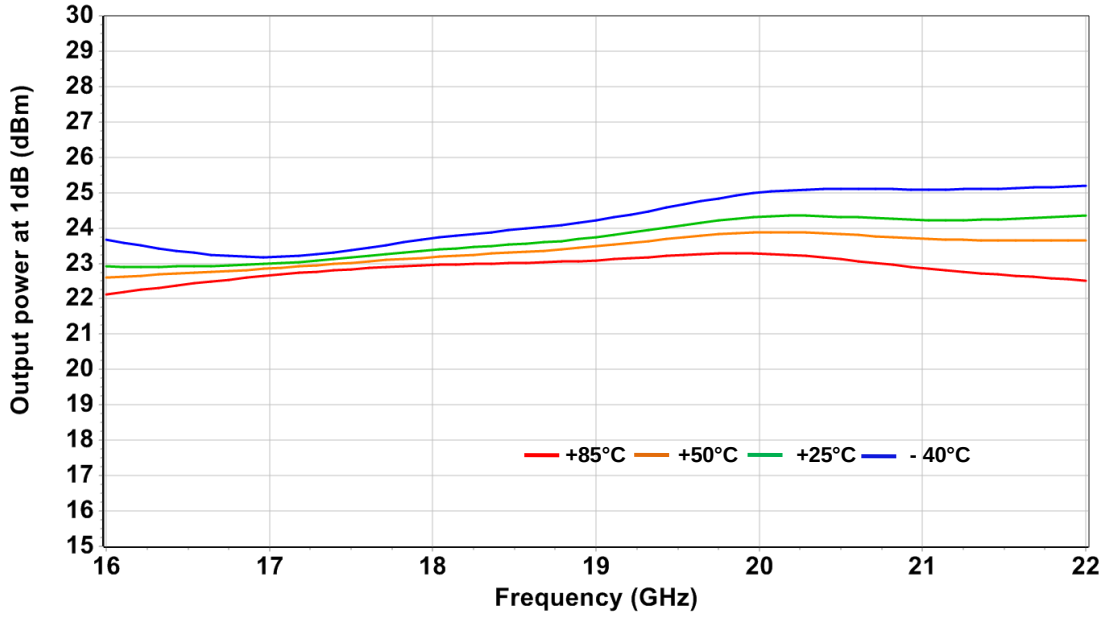
Typical Board Measurements

Vd = +4.0V. Idq = 230mA. Measurements in packaging planes.

Output power versus Input power and Temperature at 19GHz



Output power at 1dB compression versus Temperature and Frequency



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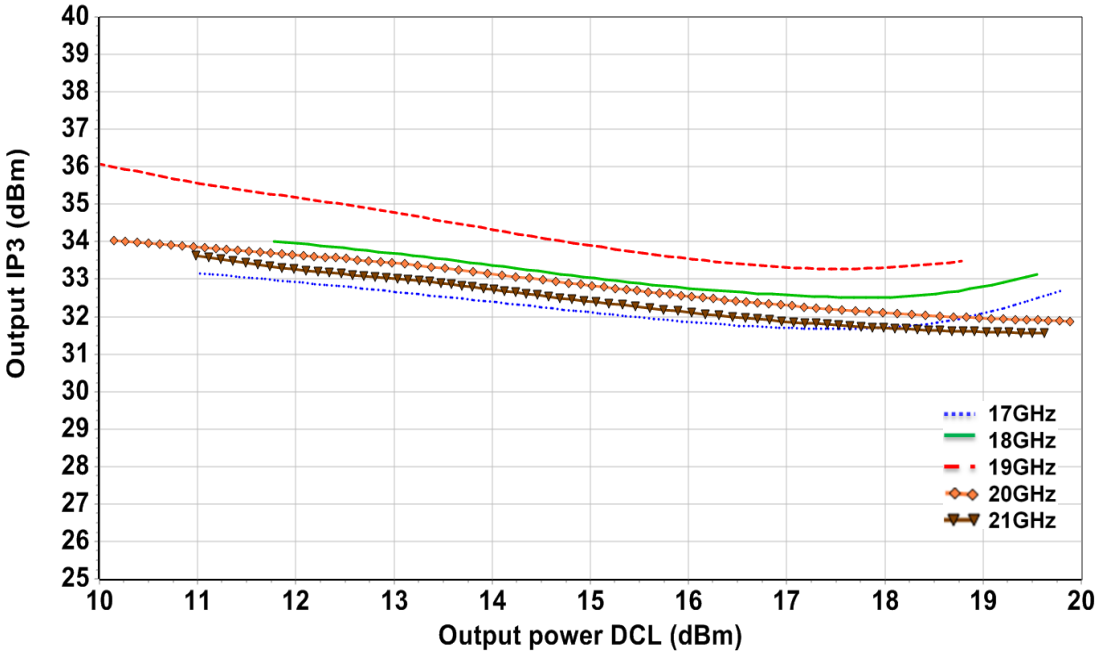
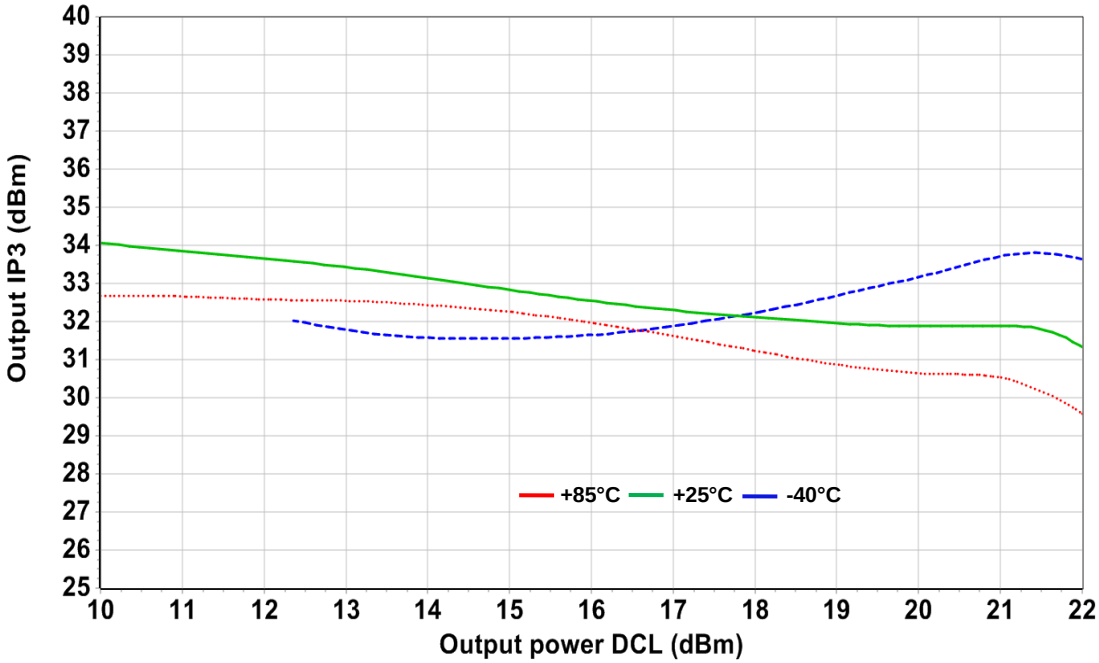
Typical Board Measurements

Tamb.= +25°C. Vd = +4.0V. Idq = 230mA. Measurements in packaging planes.

Output IP3 versus Output Power DCL & Frequency



Output IP3 versus Output Power DCL in Temperature at 20GHz



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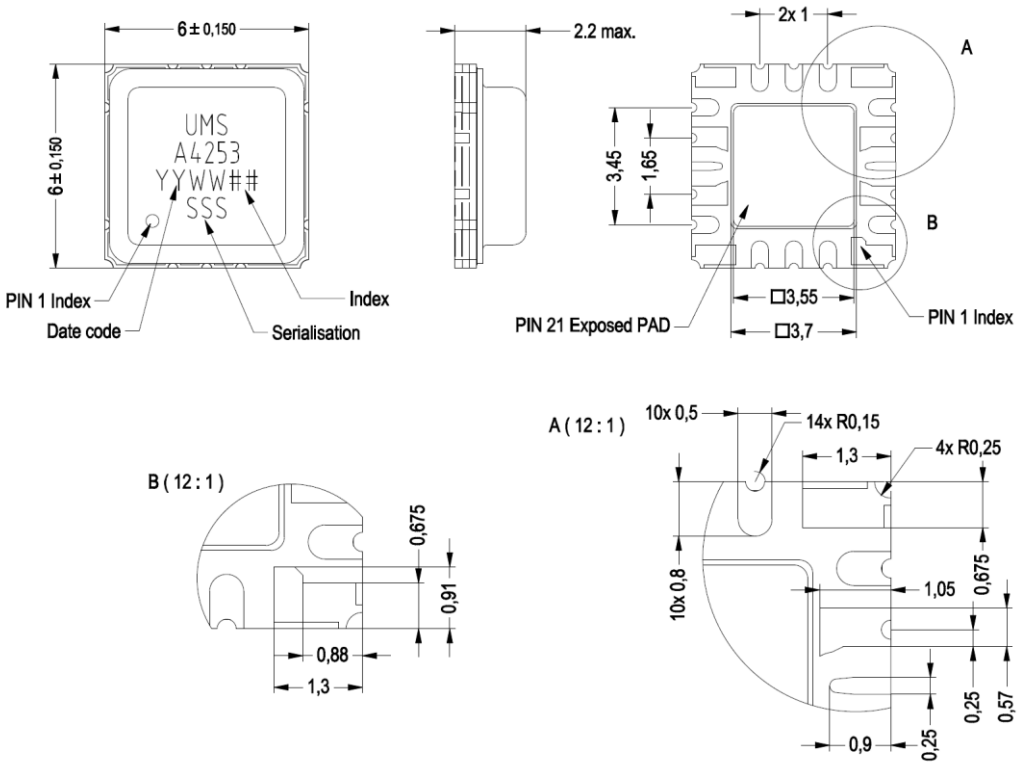
Package outline (1)



1- GND	8- RF OUT	15- GND
2- VD12	9- GND	16- Nc
3- Nc	10- Nc	17- GND
4- VD34	11- GND	18- RF IN
5- GND	12- Nc	19- GND
6- Nc	13- VG34	20- GND
7- GND	14- VG12	21- GND

Units : mm

(1) The package outline drawing included to this data-sheet is given for indication. Refer to the application note AN0024 (https://www.ums-rf.com) for exact package dimensions.

It is strongly recommended to ground all pins marked “Gnd” through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

Package Information

Parameter	Value
Package body material	RoHS-compliant
Lead finish	Gold
Hermetic sealing (fine leak compliant Mil-Std-883 Method 1014.10 Condition A4, tracer gas He at 1atm)	$1x10^{-8}$ccHe/s/atm

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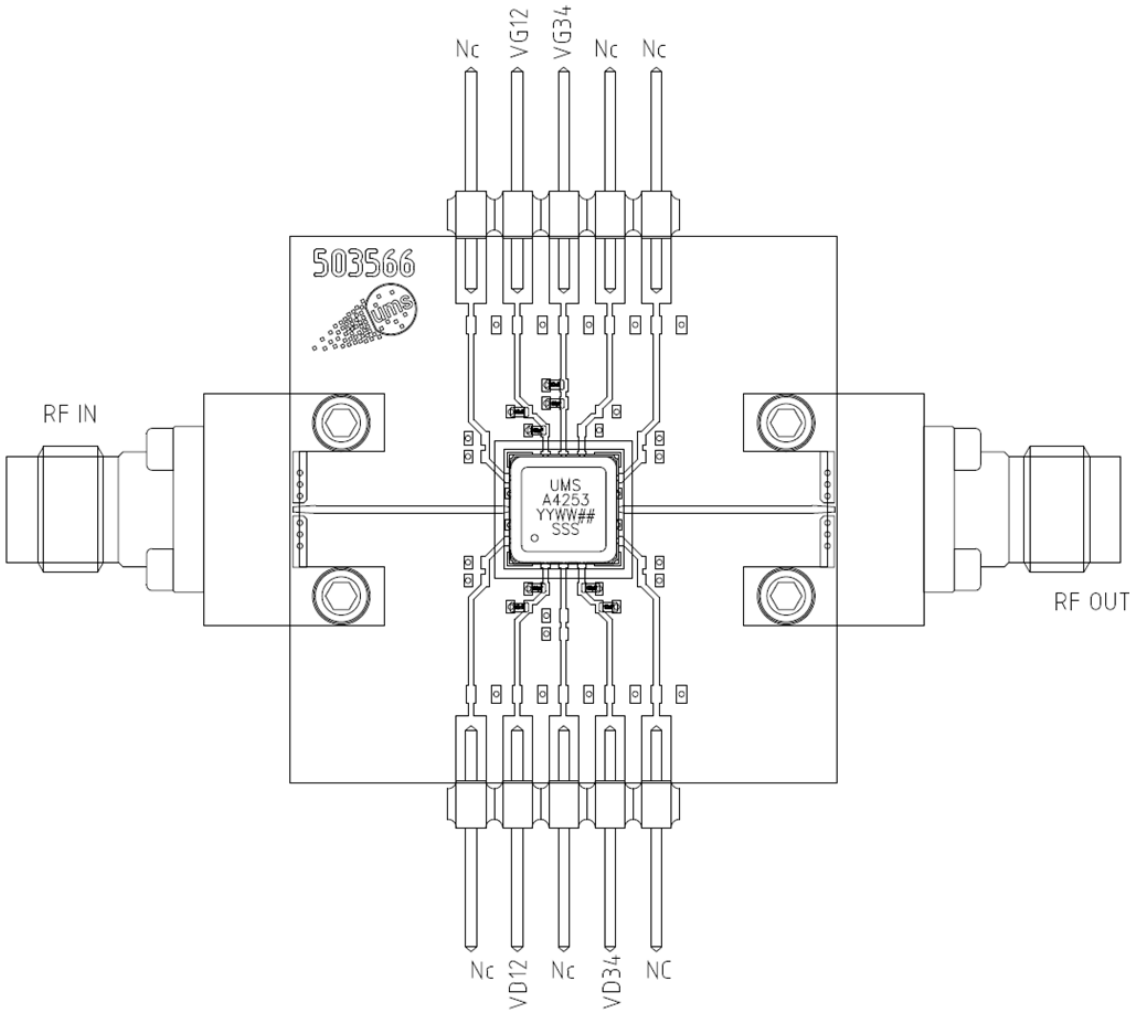
Evaluation mother board

- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a micro-strip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 100pF ±5% & 10nF ±10% are recommended for all DC accesses.
- See application note AN0024 for details.



Note: All board measurements are performed using shielded cables, even for DC bias, to ensure safe operation.

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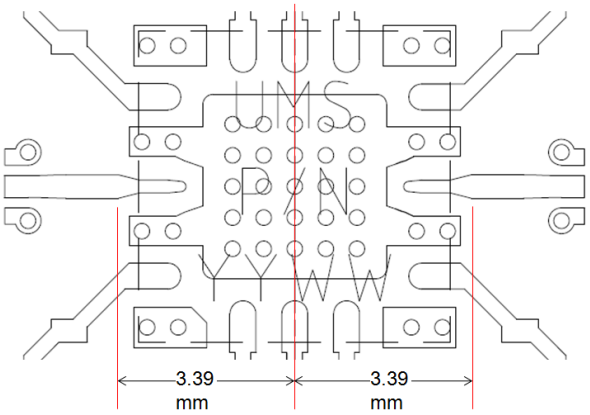
Definition of the Sij reference planes

The reference planes used for Sij measurements given above are symmetrical from the symmetrical axis of the package (see drawing beside). The input and output reference planes are located at 3.39mm offset (input wise and output wise respectively) from this axis. Then, the given Sij parameters incorporate the land pattern of the evaluation motherboard recommended in paragraph "Evaluation mother board".



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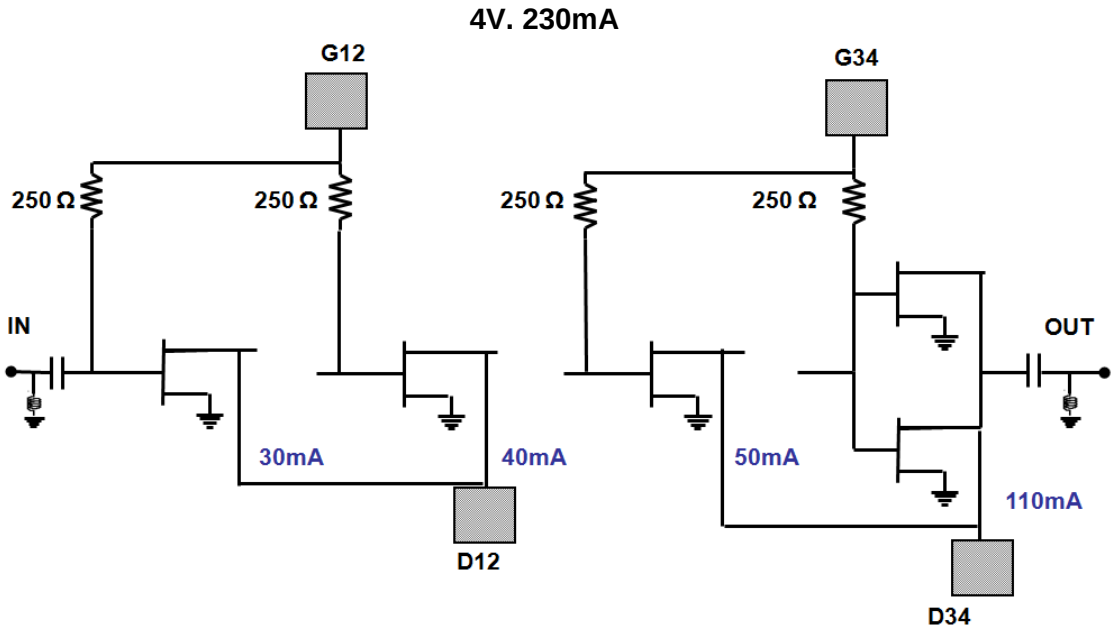
DC Schematic



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Notes

Due to ESD protection circuits on RF input and output an external capacitance might be requested to isolate the product from external voltage that could be present on the RF accesses.

The DC connections do not include any decoupling capacitor in package. Therefore it is mandatory to provide a good external DC decoupling (100pF. 10nF) on the PC board as close as possible to the package.

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Recommended package footprint for FAB Package

Refer to the application note AN0024 available at https://www.ums-rf.com for package foot print recommendations and exact package dimensions.

SMD mounting procedure for FAB Package

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details see application note AN0024 available at https://www.ums-rf.com.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at https://www.ums-rf.com.

Recommended ESD management

Refer to the application note AN0020 available at https://www.ums-rf.com for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

Leadless hermetic package:	CHA4253-FAB/XY Waffle pack: XY = 24

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