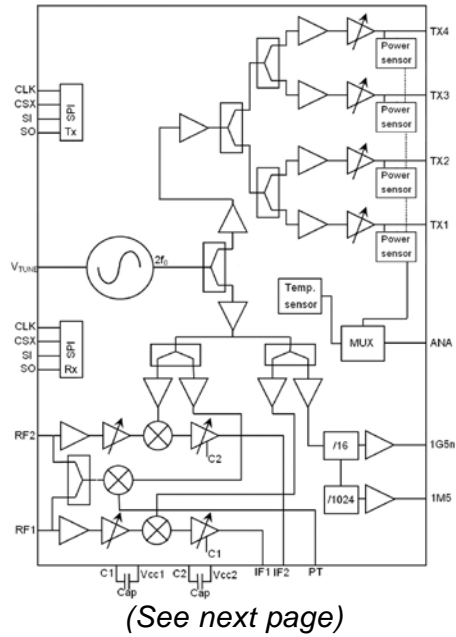


Advanced Information: AI2017

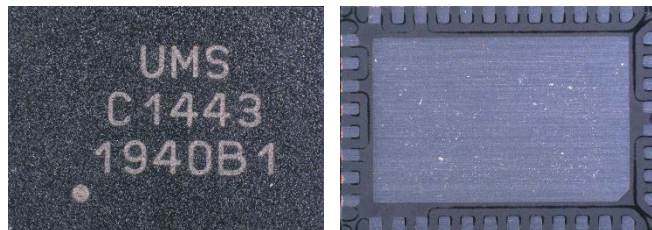
24GHz 4TX/2RX
Microwave IC in SMD Leadless package



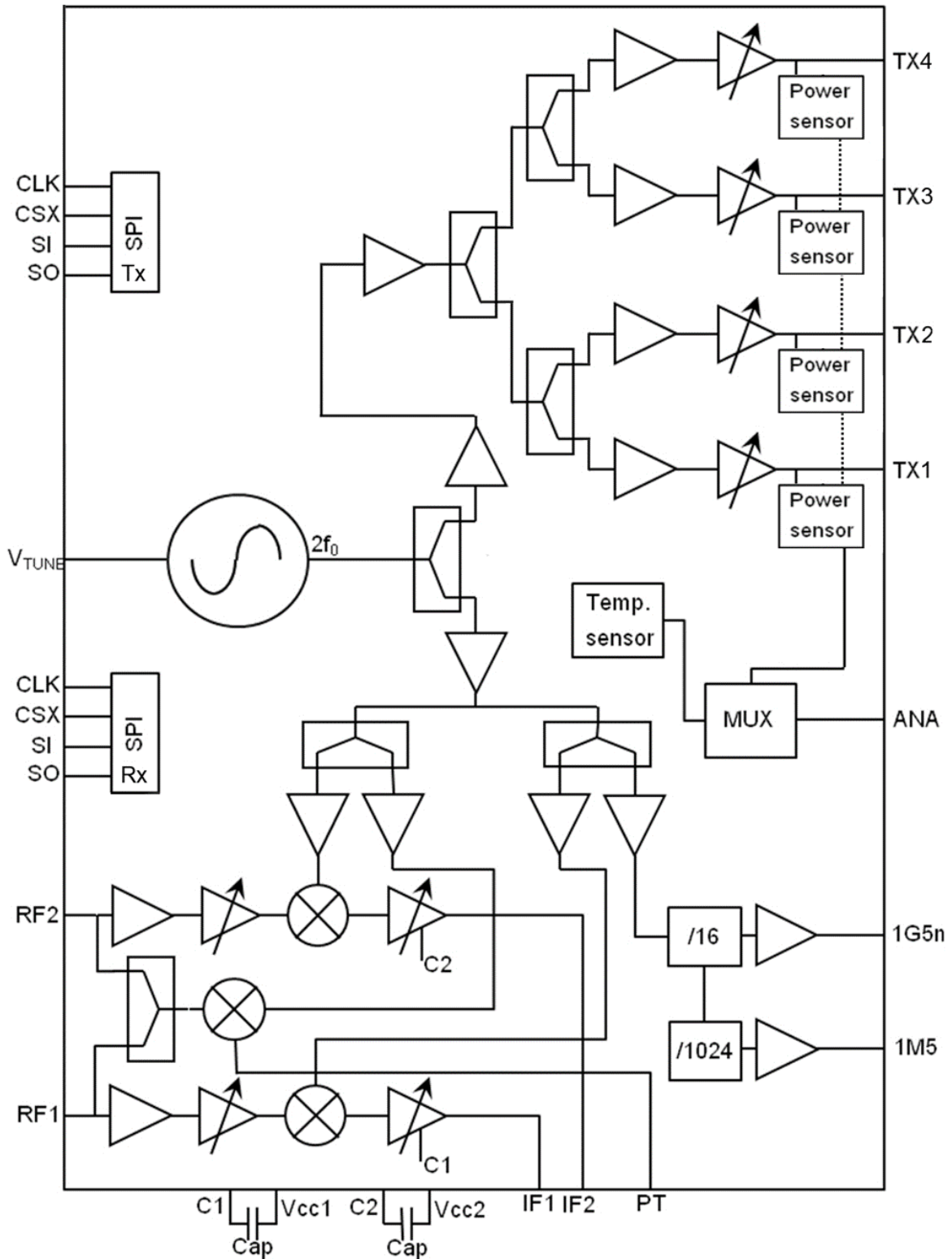
Description

UMS proposes a multifunction chip which integrates a low phase noise core VCO, four Tx MPA, two Gilbert based heterodyne Rx and, frequency calibration & loop prescalers. The circuit is fully SPI controlled and monitored with power and temperature sensors.

It is designed for signal generation and reception for 24GHz radar applications.



BLOCK DIAGRAM



Advanced Information



24 GHz 4TX2RX

Main Features

- Frequency Band: 24-24.25GHz
- 5dBm Nominal Tx Power
- Tx Power SPI controlled
- 37dB Rx gain
- 24dB Rx gain SPI controlled range
- 11dB Rx SSB NF @ IF \geq 100kHz, max RF gain
- -16dBm IP1dB RF power @ min RF VGA gain
- Temperature range from -40°C to +125°C
- DC bias: 3.3V / 250mA @ Tx 5dBm Nom./BR17='0'

Main Electrical Characteristics

TC_{Case}. = +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	24		24.25	GHz
GCv	Voltage Conversion Gain (Nom RF/IF gain)		37		dB
NF	Noise Figure SSB (Nom RF & IF gain)		11.5		dB
Pout	Output Power (Nom setting)		5		dBm
CP1dB	IP1dB compression point (Nom RF gain)		-18		dBm

Advanced Information

Ref. : AI20171025 - 25 Jan 21

3/24

Subject to change without notice

POWER/TEMPERATURE

Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Supply Voltage	3.2	3.3	3.4	V
I _{tot}	Total DC Current (@ 1 TX Pout Nom / BR17='0')		250	345	mA
I _{CC1} , I _{CC2}	Supply Current (BR17='0')			80	mA
I _{DD1}	Supply Current (BR17='0')			28	mA
I _{DD2}	Supply Current			2	mA
I _{VCO}	Supply Current			55	mA
I _{LO, TX}	Supply Current (@ 1 TX Pout Nom)			100	mA
T _{Case}	Operating Temperature (lead frame slug)	-40		+125	°C
T _S	Storage Temperature	-40		+150	°C

TX section

T_{Case}. = -40°C to +125°C, V_{cc} = +3.2 V to 3.4V

Symbol	Parameter	Min	Typ	Max	Unit
f _{VCO}	VCO Frequency Range	24.05		24.25	GHz
V _{tune}	VCO Tuning Voltage Range	0.3		4.5	V
f _{core}	Core VCO Frequency		f _{VCO}		GHz
Δf / ΔV _{tune}	VCO Tuning Sensitivity	350	600	1000	MHz/V
I _{_Tune}	DC Current into V_TUNE Pin		<0.001	0.5	mA
Δf / °C	VCO Frequency Drift over Temperature			6	MHz/°C
P _{N100kHz}	VCO Phase Noise @ 100kHz offset		-90	-80	dBc/Hz
Δf / ΔV _{CC}	VCO Pushing		50	200	MHz/V
Δf _{int1}	VCO Pulling vs. TX, LO, PT Buffer Adjust			8	MHz
Δf _{int2}	VCO Pulling vs. Prescaler (B12='1' & B13 alternate btw '0' & '1') (w/o thermal drift)		0.05	0.5	MHz
Δf _{int3}	VCO Pulling vs. low pulling Mute & 1Tx select		1	2	MHz
Δf _{ext}	TX Load Pulling into 3:1 VSWR @ Nominal Tx SPI power setting		0.25	1	MHz
Z _{TXLoad}	TX Load Impedance		50		Ω
ΔP _{O(f)}	TX Power Variation over Frequency			+/- 1	dB
ΔP _{O(f & temp)}	TX Power Variation range over Temperature @ Nominal Tx SPI power setting			<3.5	dB
PO, nom	TX Output Power @ fVCO @ Nominal Tx SPI power setting	1.20	5	7.5	dBm
PO,max	TX Maximum Output Power @ fVCO (with Tx SPI power control)	7.4	8	8.2	dBm
PO,min	TX Minimum Output Power @ fVCO (with Tx SPI power control)	-1.5	-1	0.5	dBm
N _{PO}	TX Output Power Steps (Tx SPI)		16		
Po_delta	TXi to TXj delta power (@ Nom power)	0	<0.5	<1	dB
TX_ iso	TXi to TXj isolation (1TX @ Nom power)	>28			dB

Advanced Information



24 GHz 4TX2RX

AI2017
January 2021

TX _{swt}	TX switching time (TX _i off to TX _j on) after CSX TX (50% command / 90% output)			<0.5	μs
TX _{rflon}	TX _i ON output Return losses on 50Ω load @ Nominal Tx SPI power setting		<-9	<-7	dB
P _{TX}	Total TX Power Sensors Voltage @ Nom TX power 5dBm (sensor voltage linear with power)		1.3		V
f _{TXPS}	TX Power Sensor Frequency Response	10	20		kHz
D _{Q1}	Prescaler 1 Division Ratio		16		
P1G5	Prescaler 1 Output Power on 1G5N / 50Ω AC (BR17='0' / Reduced DC power)	-14	-9.5	-5	dBm
D _{Q2}	Prescaler 2 Division Ratio		1024		
V _{Q2}	Prescaler 2 Output Voltage Adjust Range (BR21='0' / P1M5 Full swing)	0.1		V _{cc}	V
Z _{P1M5 Out}	Output Impedance of Prescaler 2 for P1M5 (BR21='1' / P1M5=100mVpp)		50		Ω
Z _{P1M5 Load}	Load of Prescaler 2 for P1M5	3.5k		20k	Ω
P _{O(mute)}	TX Power Disable (Mute)		-40	-25	dBm
H _{n_TX}	TX Harmonics (12, 36, 48 & 60GHz)		-30	-24	dBm
H _{n_SUPPLY}	Bias ports Harmonics (12, 36, 48 & 60GHz) w/o external decoupling		-18	-10	dBm
H _{pres}	Prescaler Harmonics rejection (BR17='1')		-27	-20	dBc
Sp _{TX}	Non-harmonic Spurious Rejection (prescaler OFF)		-80	-70	dBc

Advanced Information

Ref. : AI20171025 - 25 Jan 21

5/24

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RX section

T_{Case} = -40°C to +125°C, V_{cc} = +3.2 V to 3.4V

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	24.05		24.25	GHz
Z _{RXn}	RXn Port Impedance		50		Ω
RL _{RXn}	RXn Return Loss		-20	-10	dB
Z _{IFn Out}	Output Port Impedance of IF Amplifier			50	Ω
Z _{IFn Load}	Load of IF Amplifier BR17='1' / nominal DC power BR17='0' / reduced DC power	150 500			Ω
GC _{Vtotal}	Voltage Conversion Gain (Min VGA, Nom mixer, Nom IF gain / 500Ω IF load / BR17='0')	26	33	39	dB
	Voltage Conversion Gain (Nom VGA , Nom mixer, Nom IF gain / 500Ω IF load / BR17='0')	30	37 (no VIF change)	44	
	Voltage Conversion Gain (Max VGA , Nom mixer, Nom IF gain / 500Ω IF load / BR17='0')	32	40	47	
ΔGC _{VRF}	Gain Variation vs RXn Frequency			± 1	dB
ΔCG _{Vtotal_cp}	Conversion Gain over Temperature (With VGA gain settings)			±1	dB
ΔCG _{Vtotal}	Conversion Gain variation range over Temperature @ Nominal Gain (RF & IF)		±2.5	±3	dB
ΔG _{RF}	RF gain adjust range		10		dB
ΔG _{IF}	IF Gain adjust range		14		dB
I _{TX/RXn}	TX to RXn Isolation @ Nominal Tx SPI power setting	40	45		dB
I _{LO/RXn}	TX/LO to RXn leakage @ any Tx SPI power settings		-40	-34	dBm
I _{LO/IFn}	LO to IFn leakage		-35	-30	dBm
I _{RXi/IFj}	RXi to IFj Isolation	30	38		dB
I _{RXi/RXj}	RX1 to RX2 & RX2 to RX1 Isolation	30	35		dB
f _{IF HP}	HP Filter cut-off frequency of IF Amplifier		DC	10	kHz
f _{IF LP}	LP Filter cut-off frequency of IF Amplifier	10	25	40	MHz
FS _{if}	Roll-off factor of IF Amplifier			20	dB/dec
T _{IF}	IF Amplifier time constant τ			0.7	μs
N _{SSB(10kHz)}	Noise Figure SSB at IF=10kHz (HPF=OFF) nominal RF & IF gain		<15	18	dB
N _{SSB(≥100kHz)}	Noise Figure SSB at IF≥100kHz (HPF=OFF) nominal RF & IF gain		11.5	15	dB
IF _{noise}	IF Noise Power Density @ CG _{VRF} gain with 500 Ω IF load and IF=100kHz and HPF=OFF		-136	-130	dBm/Hz

Advanced Information



ΔI_{noise}	IF Noise Power Variation over Temperature (With VGA gain settings)			± 2.5	dB
f_{Cn}	IFn Noise Corner Frequency (HPF=OFF)		10		kHz
IP_{1dB}	RF Input Compression Point (Min VGA, Nom mixer, Min IF gain)	-19	-14		dBm
	RF Input Compression Point (Nom VGA, Nom mixer, Min IF gain)	-24	-18		
	RF Input Compression Point (Max VGA, Nom mixer, Min IF gain)	-28	-21		
IIP_3	3rd Order Input Intercept Point (Min VGA, Nom mixer, Min IF gain)	-9	-5		dBm
	3rd Order Input Intercept Point (Nom VGA, Nom mixer, Min IF gain)	-14	-9		
	3rd Order Input Intercept Point (Max VGA, Nom mixer, Min IF gain)	-18	-12		
$V_{IFn(1dB\ comp)}$	IFn Output Voltage at 1dB Compression Point (HPF ON / B10='0')	2	2.5	3	V_{p-p}
H_{pIF}	IFn Harmonics ($P_{RF} < IP_{1dB} - 3dB$)		-30	-20	dBc
Sp_{IF}	Mixing Products Spurious			-30	dBc
$\Delta\phi_{Diff}$	Phase Tracking between IF1, IF2 (calibrated)	-3		3	Deg
$\Delta\phi_{Diff, uncal}$	Phase Difference Variation ($\phi_{IF1} - \phi_{IF2}$) for equal phase RX input	0	± 1	± 15	deg
$\Delta\phi_{Diff, power, up}$	Phase Difference Variation ($\phi_{IF1} - \phi_{IF2}$) for equal phase RX input and power up with calibrated Frequency Range	0	± 1	± 2	deg
ΔP_{IF}	Amplitude Tracking between IF1, IF2 (calibrated)		± 0.25	± 1	dB
H2 & H3	RF & LO Harmonics (2nd & 3rd) at IF Ports			-30	dBm
V_{ANA}	ANA output voltage	0.2		3.1	V
R_{ANA}	ANA resistive load	9			k Ω
C_{ANA}	ANA capacitive load			15	nF
ΔV_{Temp}	Temperature Sensor Voltage Sensitivity	6.25	7	7.75	mV/ $^{\circ}C$
V_{Temp}	Temp. Sensor Voltage @ $T_{Case} = +25^{\circ}C$	0.7	1.65	2.33	V
	Temp. Sensor Voltage @ $T_{Case} = +125^{\circ}C$	1.47		3.1	
	Temp. Sensor Voltage @ $T_{Case} = -40^{\circ}C$	0.2		1.83	
$t_{TempSet}$	Temperature Sensor Settling Time			1	ms

These values are representative of PCB measurements as defined on the drawing in paragraph "Evaluation board".

Advanced Information



ABSOLUTE MAX RATINGS⁽¹⁾

Parameter	Min Rating	Max Rating	Unit
V _{CC} to GND (Any supply)	-0.3	3.8	V
Digital I/O Voltage to GND	-0.3	V _{dd} +0.3	V
Analog Voltage AMUX to GND	-0.3	V _{CC} +0.3	V
Analog I/O Voltage to GND	-0.3	V _{CC} +0.3	V
Analog Voltage V_TUNE to GND	-0.3	7.5	V
DC Current into IF1, IF2 Pin	0	12.5	mA
DC Current into ANA Pin	0	0.4	mA
DC Current into V_TUNE Pin (1)		9	mA
RF Power Input at RX1, RX2 Pin		0	dBm
DC Voltage at RF Output Tx Pin and RF Input RX1, RX2 Pin		0	V
Total DC Power Dissipation (BR17='0')		1.13	W
Absolute T _{Case} Operating Temperature (lead frame slug)	-40	+125	°C
Non-operating Temperature Range (Storage)	-40	+150	°C
Peak Soldering Temperature		+260	°C

Operation of this device above anyone of these parameters may cause permanent damage or reduce MTTF. All functions activated (max DC current SPI configuration)

⁽¹⁾ Voltage applied through external serial resistor to limit V_TUNE current below 9mA DC.

Recommended operating conditions ^{(2) (3)}

Parameter	Nominal	Unit
V_{TX} V_{CC1} V_{CC2}	3.3	V
Digital I/O Voltage	0 to 3.3	V
V_{DDx}	3.3	V
Analog Voltage V_{TUNE}	0 to 4.5	V
RF Power Input at RX1, RX2 Pin	0	dBm

² Electrical performances are defined for specified test conditions

³ Electrical performances are not guaranteed over all recommended operating conditions

Device thermal performances

All the figures given in this section are obtained assuming that the QFN device is cooled down only by conduction through the package thermal pad (no convection mode considered).

The temperature is monitored at the package back-side interface (T_{Case}) as shown below. The system maximum temperature must be adjusted in order to guarantee that T_{Case} remains below than the maximum value specified in the next table. So, the system PCB must be designed to comply with this requirement.

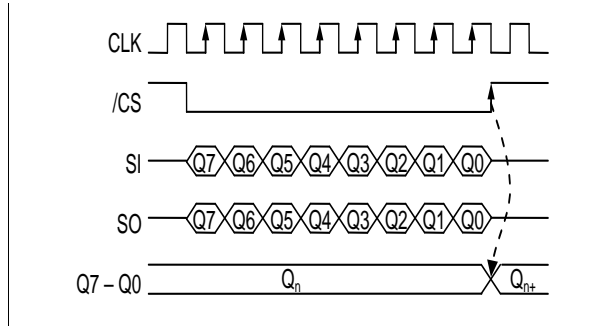
Thermal Performance Specifications

All functions activated (max DC current SPI configuration)

Maximum continuous dissipated power at $T_{case} = +125^{\circ}C$: 1.13 Watts

SPI PROTOCOL (RX & TX)

The digital input should use standard 4-wires synchronous serial peripheral interface (SPI) with data read and write capabilities. The SPI has hardwired Power-On Reset, such that the output bits for Control Bus will be set to default state (low power mode) after turning on 3.3V supply.. Data transmission is enabled by negative edge of CS (Chip Select) and serial data input (SI) are then read at the rising edge of CLK (SPI Clock). The timing diagram in the next picture describes the principle of the SPI timing and handling between shift and storage register.



SPI Settings:

CPOL=1 CPHA=1

Falling edge: Bit is changed.

Rising edge: Bit is sampled.

MSB is transmitted first

SPI Start-up reset (RX & TX)

Upon start-up after VDD positive edge, an internal reset of all registers bits occurs in less than 1ms. Settled to '0'.

SPI TIMING (RX & TX)

Parameter	Symbol	Values			Unit
		Min.	Typ.	Max.	
Serial clock frequency			30	50	MHz
Serial SI and CSX high time		10			ns
Serial SI and CSX low time		10			ns

Digital I/O Levels (RX & TX)

Symbol	Parameter	Min	Typ	Max	Unit
V _{OH}	High Level Output	2.4			V
V _{OL}	Low Level Output			0.4	V
V _{IH}	High Level Input	2.0			V
V _{IL}	Low Level Input			0.8	V
I _{O,Load}	Output Load Current		0.4	1	mA
I _{O,Peak}	Output Peak Current	2			mA
C _{Load}	Capacitive Load			100	pF

Advanced Information

SPI RX MAIN TABLE

Data Bit	Function	Description	
LSB	BR0	VGA Gain	
	BR1		
	BR2		
	BR3	IF Low Pass Filter	IF Low Pass Filter ⁽²⁾
	BR4	Not Used	<u>Must be all set to '0'</u>
	BR5		
	BR6		
	BR7		
	BR8		
	BR9	LO AMPS	LO amplifier enable ⁽⁵⁾
	BR10	IF High Pass Filter	IF High Pass Filter ⁽⁶⁾
	BR11	Not Used	Not Used
	BR12	Prescaler	4 prescaler settings ⁽⁷⁾
	BR13		
	BR14	Pilot Tone	RX channels self test ⁽⁸⁾
	BR15	MUX	4 Analog outputs ⁽⁹⁾
	BR16		
	BR17	DC Power mode	2 loads ⁽¹⁰⁾
	BR18	IF Amp Gain	8 IF gain settings ⁽¹¹⁾
	BR19		
	BR20		
	BR21	1.5MHz mode	2 voltage swing setting ⁽¹²⁾
	BR22	Mixer Gain	2 Mixer gain settings ⁽¹³⁾
MSB	BR23	RX Enable	RX IC Enable ⁽¹⁴⁾

(1)VGA NOMINAL GAIN SETTINGS TABLE

BR2	BR1	BR0	VGA Gain
0	0	0	" +2,6 dB"
0	0	1	" +1,2 dB"
0	1	0	Nominal / "0 dB"
0	1	1	" -1,1 dB"
1	0	0	" -1,9 dB"
1	0	1	" -2,9 dB"
1	1	0	" -3,6 dB"
1	1	1	" -4,3 dB"

(5)LO AMPLIFIER SETTINGS TABLE

BR9	LO amplifier enable
0	OFF
1	ON

Advanced Information

(13) MIXER NOMINAL GAIN SETTINGS TABLE

BR22	Mixer Gain
0	nominal -3dB
1	nominal

(7) PRESCALER MODE SETTINGS TABLE

BR13	BR12	Prescaler mode
0	0	OFF
0	1	Frequency output 1.5MHz
1	0	Frequency output 1.5GHz
1	1	OFF/ Low Pulling

(12) 1.5MHz MODE SETTINGS TABLE

BR21	1.5MHz mode
0	Full output swing 0-Vcc
1	0,1Vpp/50Ω

(10) DC POWER MODE SETTINGS TABLE

BR17	DC power mode
0	Zif ≥ 500Ω / P1G5 -3dB / Reduced DC power
1	Zif ≥ 150Ω / P1G5 nominal

(9) MUX SETTINGS TABLE

BR16	BR15	Mux mode
0	0	ANA=∞ Ω
0	1	ANA=T°C
1	0	ANA=PTX

(14) RX IC ENABLE

BR23	RX Enable
0	RX OFF
1	RX ON

(1) IF GAIN SETTINGS TABLE

BR20	BR19	BR18	IF gain settings
0	0	0	"+4dB"
0	0	1	"+2dB"
0	1	0	Nominal / "0 dB"
0	1	1	"-2dB"
1	0	0	"-4dB"
1	0	1	"-6dB"
1	1	0	"-8dB"
1	1	1	"-10dB"

(2) IF LOW PASS FILTER SETTINGS TABLE

BR3	IF low pass characteristic
0	$F_{cut}=25\text{MHz}$ (nominal)
1	$F_{cut}=60\text{MHz}$

(6) IF HIGH PASS FILTER SETTINGS TABLE

BR10	IF High Pass Filter			
0	Nominal IF High Pass Filter*			
	Capacitor value	Cap=1nF	Cap=10nF	Cap=100nF
	f_{cut}	10kHz	1KHz	100Hz
	Rx GCv @ 100kHz	Nom	Nom	Nom
	Rx GCv @ 10kHz	Nom - 3dB	Nom	Nom
	Rx GCv @ 1kHz	Nom -17dB	Nom - 3dB	Nom
	Rx GCv @ 100Hz	Nom - 20dB	Nom -17 dB	Nom - 3dB
	Rx NFssb @ 100kHz	Nom + 2dB	Nom	Nom
	Rx NFssb @ 10kHz	Nom + 25dB	Nom + 5dB	Nom
	Rx NFssb @ 1kHz	Nom + 62dB	Nom + 28dB	Nom + 20dB
	Rx NFssb @ 100Hz	Nom + 102dB	Nom + 48dB	Nom + 43dB
1	IF low pass through			

The table is valid for gain settings: VGA at max gain and Mixer at nominal gain & any IF gain

*In order to have a pass band characteristic, capacitors must be connected between the pin 2-28 for RX1 and 7-9 for RX2 (see pin-out)

If HPF not used (BR10='1'), pins 2 and 7 can be left open

Advanced Information

SPI TX MAIN TABLE

Data Bit		Function	Description
LSB	BT0	TX3 or TX4 Power	16 MPA power settings ⁽¹⁵⁾
	BT1		
	BT2		
	BT3		
	BT4	TX3 or TX4 Select	TX3 & TX4 ports Selection & power Mute ⁽¹⁸⁾
	BT5		
	BT6	Not used	Not used
	BT7	TX3 or TX4 Enable	TX3 or TX4 IC Enable ⁽¹⁷⁾
	BT8	TX1 or TX2 Power	16 MPA power settings ⁽¹⁵⁾
	BT9		
	BT10		
	BT11		
	BT12	TX1 or TX2 Select	TX1 & TX2 ports Selection & power Mute ⁽¹⁸⁾
	BT13		
	BT14	Core VCO Enable	Core VCO IC DC power control / Enable ⁽¹⁶⁾
MSB	BT15	TX1 or TX2 Enable	TX1 or TX2 IC Enable ⁽¹⁷⁾

(15) TXi PORTS NOMINAL POWER SETTINGS TABLE

BT3	BT2	BT1	BT0	TXi Power stage	TXi Power variation (tbc)
BT11	BT10	BT9	BT8		
0	0	0	0	0	+2.5 dB
0	0	0	1	1	+2.0 dB
0	0	1	0	2	+1.5 dB
0	0	1	1	3	+1.0 dB
0	1	0	0	4	+0.5 dB
0	1	0	1	5	Nominal / 5dBm + 0 dB
0	1	1	0	6	-0.5 dB
0	1	1	1	7	-1.0 dB
1	0	0	0	8	-1.5 dB
1	0	0	1	9	-2.0 dB
1	0	1	0	10	-2.5 dB
1	0	1	1	11	-3.0 dB
1	1	0	0	12	-3.5 dB
1	1	0	1	13	-4.0 dB
1	1	1	0	14	-4.5 dB
1	1	1	1	15	-5.0 dB



(17) TXi IC ENABLE TABLE

BT15	BT7	TXi & TXj IC Status
X	0	(TX3 and TX4) IC OFF*
X	1	(TX3 or TX4) IC ON
0	X	(TX1 and TX2) IC OFF*
1	X	(TX1 or TX2) IC ON

(*) Note: Full IC is DC switched OFF

(18) TXi PORTS SELECTION & POWER MUTE CONTROL TABLE

BT13	BT12	BT5	BT4	TXi port Power Status			
				TX1	TX2	TX3	TX4
0	0	0	0	OFF*	OFF*	OFF*	OFF*
0	1	0	0	ON	OFF*	OFF*	OFF*
1	0	0	0	OFF*	ON	OFF*	OFF*
0	0	1	0	OFF*	OFF*	ON	OFF*
0	0	0	1	OFF*	OFF*	OFF*	ON
<u>VCO low pulling Mute with thermal compensation</u>							
1	1	1	1	OFF*	OFF*	OFF*	OFF*
Possible configurations not considered in those specifications							
0	1	1	0	ON	OFF*	ON	OFF*
0	1	0	1	ON	OFF*	OFF*	ON
1	0	1	0	OFF*	ON	ON	OFF*
1	0	0	1	OFF*	ON	OFF*	ON

(*) Note: Only TXi amplifier DC switched OFF

Recommended SPI nominal settings ⁽¹⁾

- Nominal TX power
- Nominal RF and IF Gain
- IF high pass and low pass filters activated
- Prescalar 1.5MHz
- Low DC power Mode

TX SPI

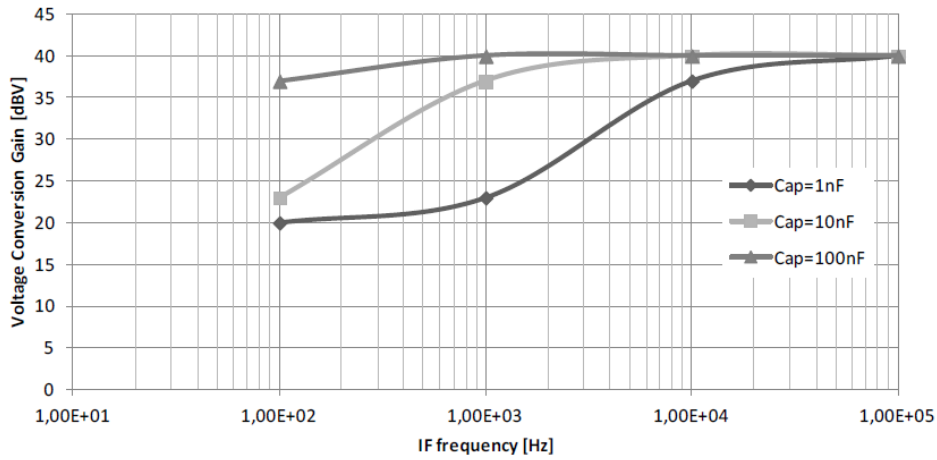
Bit	Function	Bit name	WORD
BT0	TX3 or TX4 Power	1	1
BT1	TX3 or TX4 Power	2	0
BT2	TX3 or TX4 Power	3	1
BT3	TX3 or TX4 Power	4	0
BT4	TX4 select	5	X
BT5	TX3 Select	6	X
BT6	Not used	7	0
BT7	TX3 or TX4 Enable	8	1
BT8	TX1 or TX2 Power	9	1
BT9	TX1 or TX2 Power	10	0
BT10	TX1 or TX2 Power	11	1
BT11	TX1 or TX2 Power	12	0
BT12	TX1 select	13	X
BT13	TX2 Select	14	X
BT14	Core VCO Enable	15	1
BT15	TX1 or TX2 Enable	16	1

RX SPI

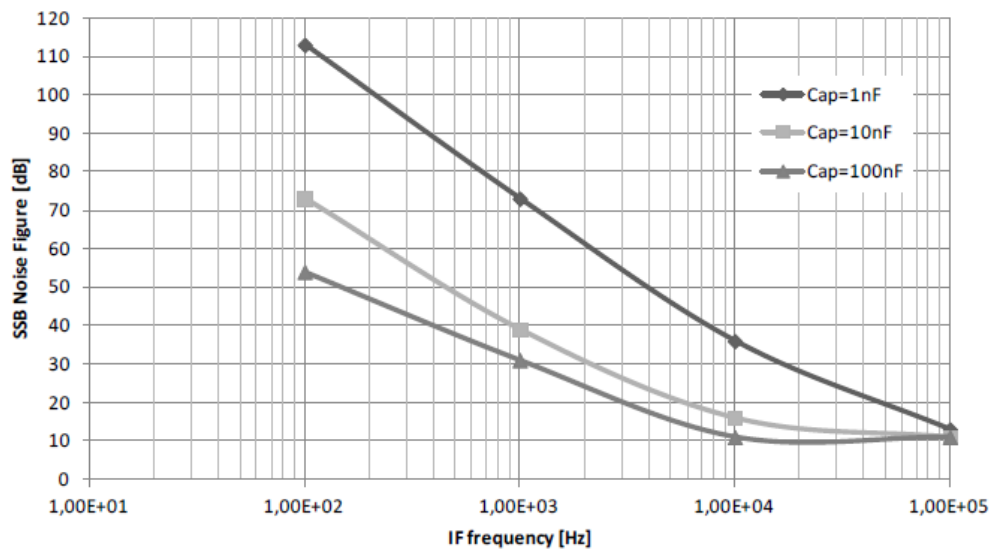
Bit	Function	Bit name	WORD
B0	VGA Gain	G0	0
B1	VGA Gain	G1	1
B2	VGA Gain	G2	0
B3	IF Low Pass Filter	IP	0
B4	Not used	B4	0
B5		B5	0
B6		B6	0
B7		B7	0
B8		B8	0
B9	LO AMPS	LP	1
B10	IF High Pass Filter	F0	0
B11	Not Used	B11	0
B12	Prescaler mode	D0	1
B13	Prescaler mode	D1	0
B14	Pilot Tone	PT	0
B15	MUX	X0	0
B16	MUX	X1	1
B17	DC Power mode	DP	0
B18	IF Amp Gain	I0	0
B19	IF Amp Gain	I1	1
B20	IF Amp Gain	I2	0
B21	1.5MHz mode	D2	0
B22	Mixer Gain	MG	1
B23	IC Enable	EN	1

Measurement on evaluation board

Conversion gain versus IF frequency and HPF cap
(nominal RF & IF gain)

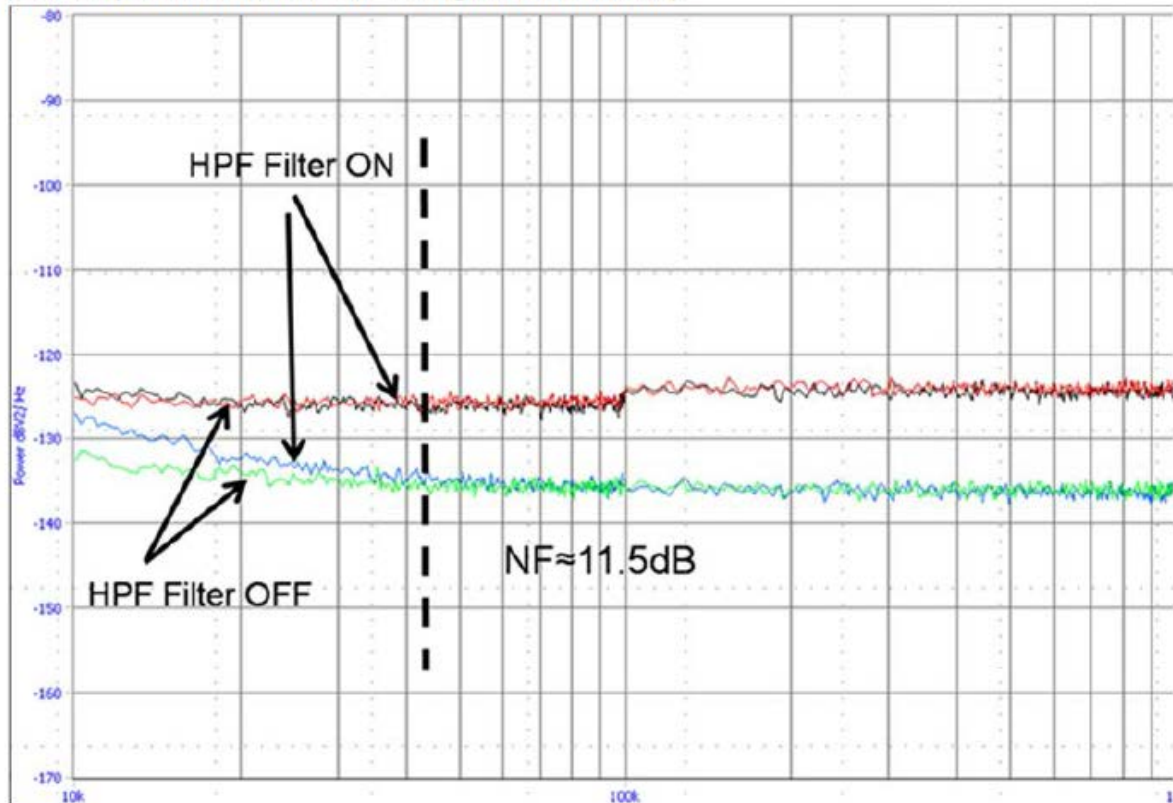


SSB Noise Figure versus frequency and HPF cap

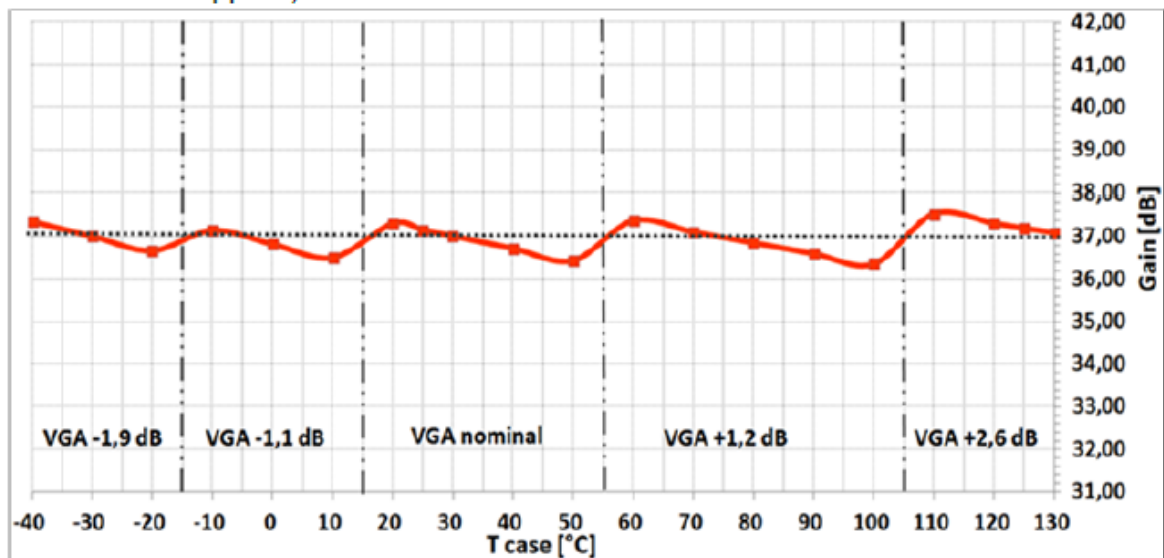


24 GHz 4TX2RX

SSB Noise Figure versus IF frequency
(HPF Cap=10nF / nominal RF & IF gain / HPF on-off)

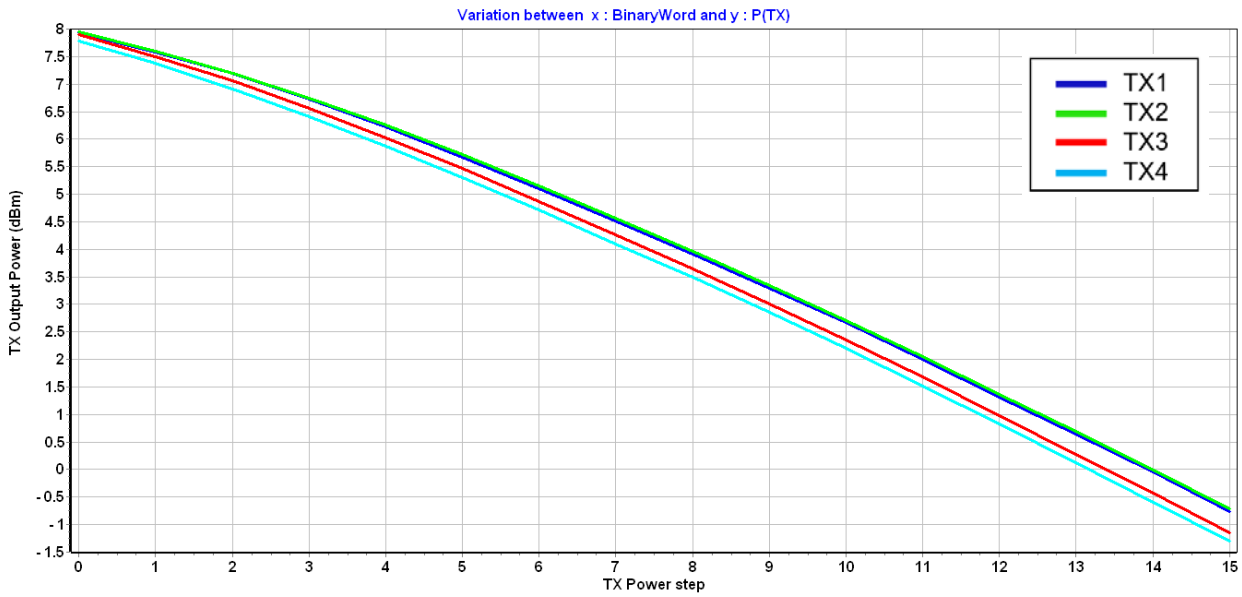


Rx Gain over Tcase using VGA settings
(Nominal 3.3V supplies)

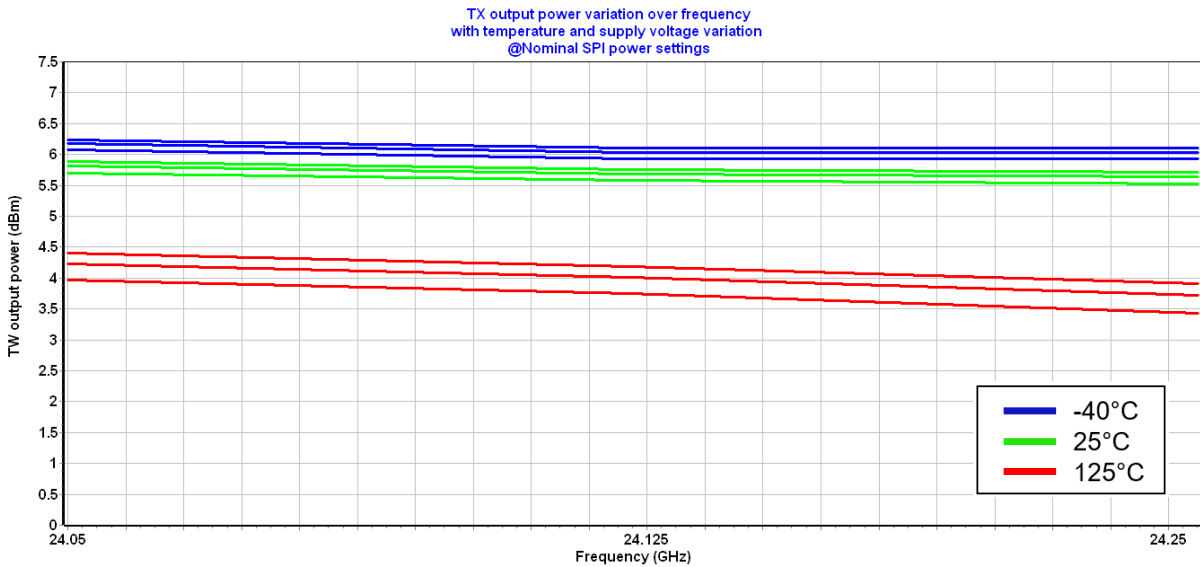


Advanced Information

TXs output power versus power settings
0 = max power, 5 = nominal power, 15 = min power



TX output power over frequency band @nominal power setting
Temperature variation (blue = -40°C, green=25°C, red = 125°C)
Supply voltage variation from 3.2V to 3.4V. (step = 0.1V)

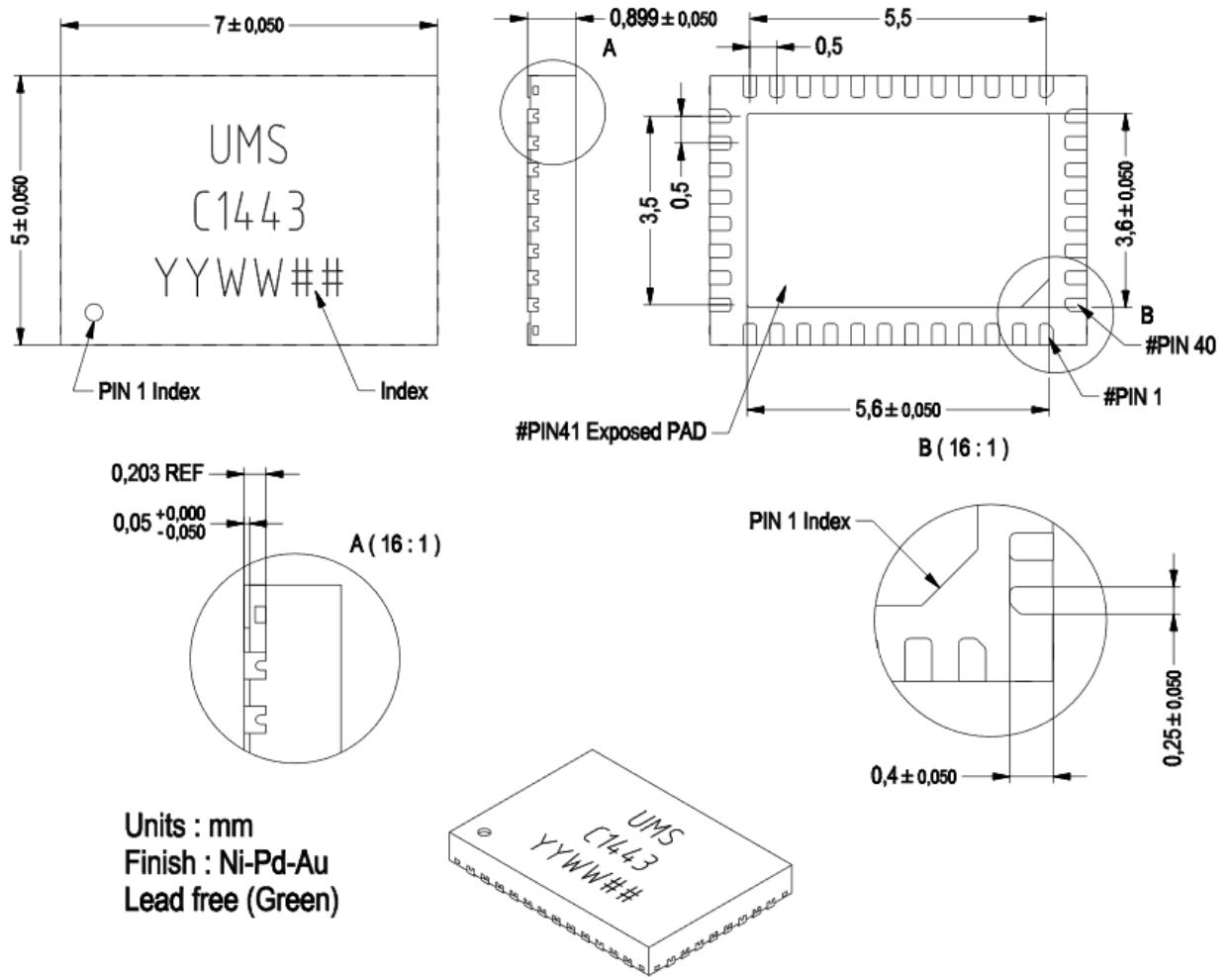


Advanced Information



24 GHz 4TX2RX

Package outline (1)



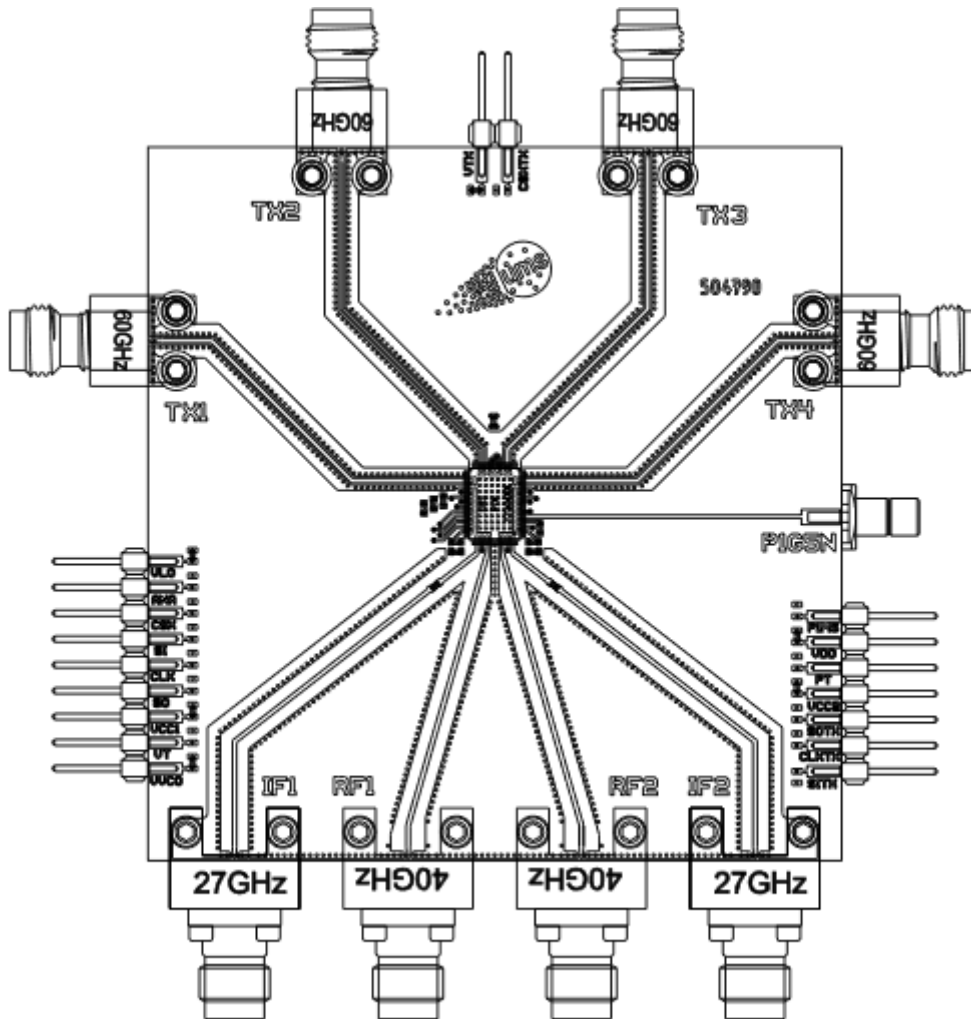
Matte tin, Lead Free (Green)	1- VCC2	15- GND	29- SI
Units : mm	2- PT	16- CSX_Tx	30- CLK
From the standard : JEDEC MO-220 (VGGD)	3- VDD	17- VTX	31- SO
	4- P1G5N	18- GND	32- VCC1
	5- P1M5	19- TX2	33- IF1
	6- Nc	20- GND	34- C1
	7- SO Txc	21- GND	35- RF1
	8- CLK Tx	22- TX1	36- GND
	9- SI Tx	23- GND	37- GND
	10- GND	24- Vvco	38- RF2
	11- TX4	25- Vtune	39- C2
	12- GND	26- VLO	40- IF2
	13- GND	27- ANA	41- GND
	14- TX3	28- CSX	

Advanced Information

(1) The package outline drawing included to this data-sheet is given for indication. Refer to the application note AN0017 (<https://www.ums-rf.com>) for exact package dimensions.

(2) It is strongly recommended to ground all pins marked "Gnd" through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

CHC1443 EVALUATION BOARD



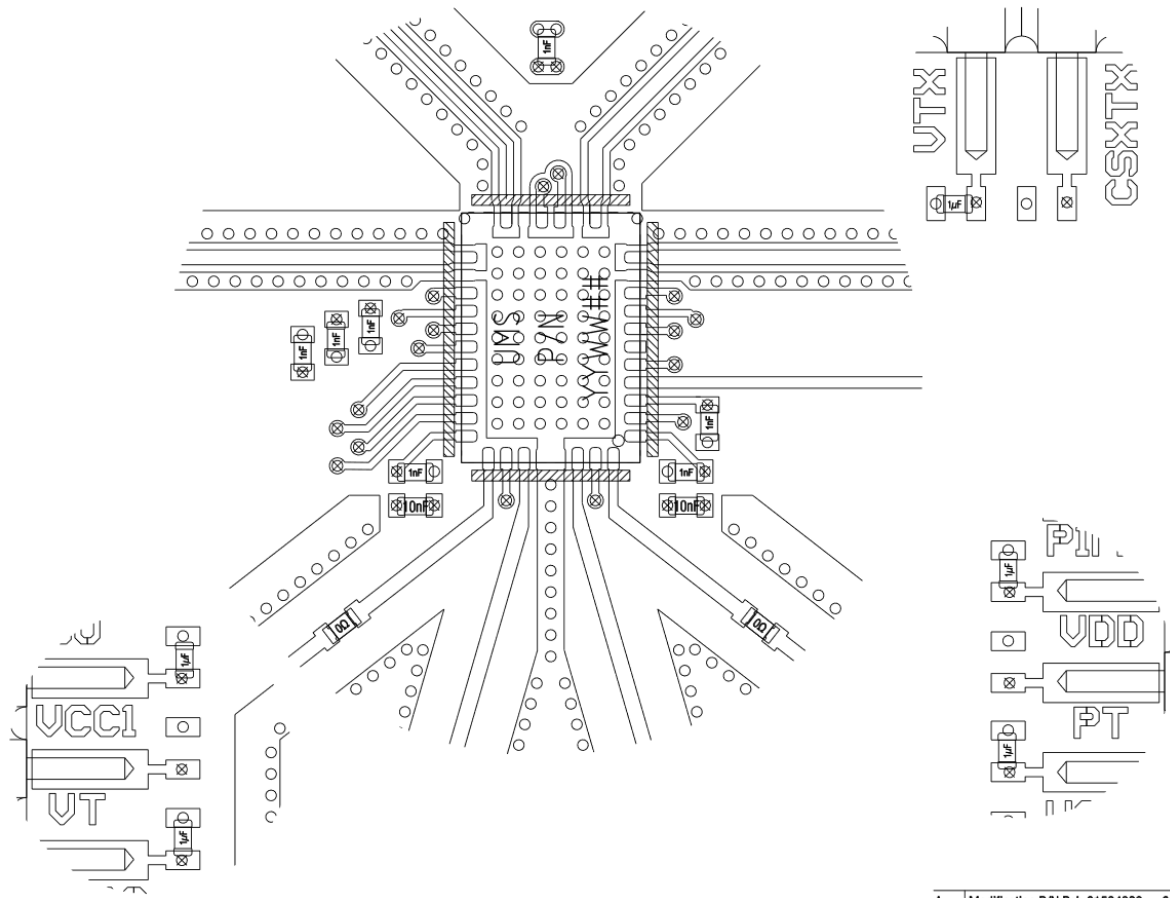
Evaluation board

- Recommended package footprint.
- Based on Ro4003 / 8mils.
- Use micro-strip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 10nF near the packaging and 1µF near the connectors are recommended for all supplies.

Advanced Information

24 GHz 4TX2RX

AI2017
January 2021



A | Modification DAI Deb 61604/20 ~ 616

Advanced Information

Ref. : AI20171025 - 25 Jan 21

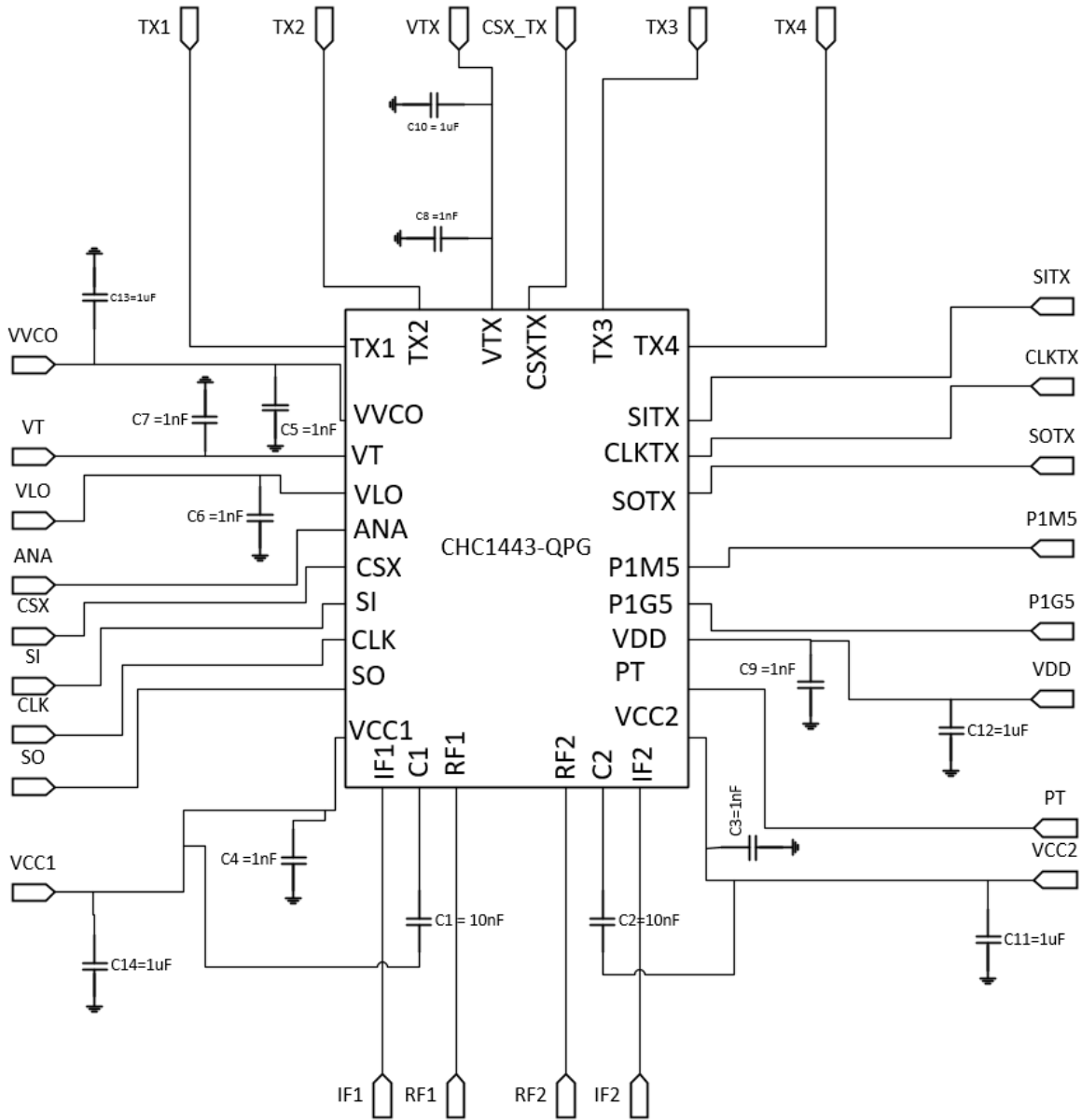
23/24

Subject to change without notice

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Evaluation Board External components



Advanced Information