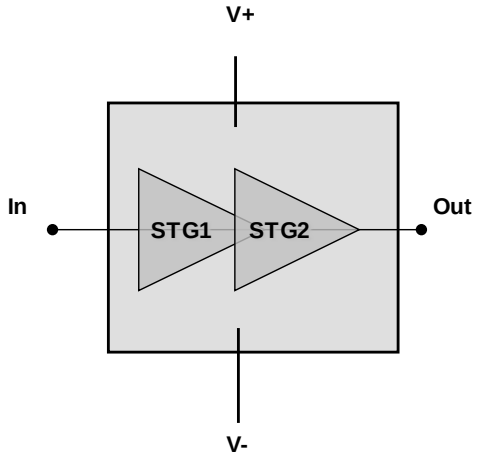
CHA4314-98F

4.7-11.3GHz Medium Power Amplifier

GaAs Monolithic Microwave IC

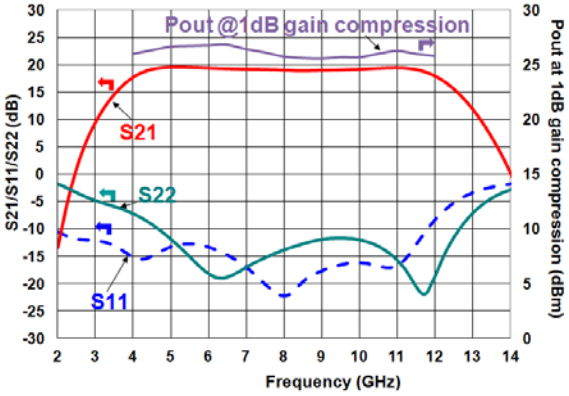
Description

The CHA4314-98F is a two stage monolithic medium power amplifier circuit.
It is designed for a wide range of applications, from military to commercial communication systems.
The circuit is manufactured with a pHEMT process, 0.15µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.
It is available in chip form.



Main Features

- Broadband performances: 4.7-11.3GHz
- Linear Gain: 19dB
- Pout@1dB gain compression: 26dBm
- OIP3: 34dBm
- PAE@1dB gain compression: 31%
- DC bias: Vd=5Volt@Id=180mA
- Chip size 3.45x1.6x0.07mm



Main Electrical Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	4.7		11.3	GHz
Gain	Linear Gain		19		dB
Pout	Output Power @1dB comp.		26		dBm
Pae	PAE @1dB comp.		31		%
OIP3	Third order output intercept point		34		dBm

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Specifications

Tamb.= +25°C, Vd = +5V / IDq = 180mA CW mode

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	4.7		11.3	GHz
Gain	Linear Gain		19		dB
Gain ripple	Peak to peak variation of the linear gain in the frequency range		0.7		dB
Gain_T	Linear gain variation versus temperature at fixed Vg		0.016		dB/°C
RLin	Input Return Loss		12		dB
RLout	Output Return Loss		12		dB
NF	Noise figure		3.5		dB
OIP3	Output third order interception point		34		dBm
P_{-1dB}	Output Power @1dB gain compression		26		dBm
P_{-3dB}	Output Power @3dB gain compression		27		dBm
PAE_{-1dB}	Power added efficiency @1dB gain comp.		31		%
PAE_{-3dB}	Power added efficiency @3dB gain comp.		34		%
Id_{-1dB}	Drain current @1dB gain compression		260		mA
Id_{-3dB}	Drain current @3dB gain compression		300		mA
Vd1,2	Drain supply voltage		5		V
Id	Drain quiescent current		180		mA
Vg	Gate supply voltage		-0.7		V

These values are representative of measurements in test fixture with bonding wires at the RF ports.
Wire bonding at RF accesses: 0.4nH, typically.

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Absolute Maximum Ratings (1)

Tamb.= +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	8V	V
Id	Drain bias current	0.5	A
Vg	Gate bias voltage	-2.5 to+0.4	V
Pin	Input continuous power	+15	dBm
Tj	Maximum Junction temperature (2)	175	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.

(2) See “Device thermal performances” for Thermal Resistance channel to ground paddle

Temperature Range

Ta	Operating temperature range	-40 to +95	°C
Tstg	Storage temperature range	-55 to +150	°C

Typical Bias Conditions

Tamb.= +25°C

Symbol	Pad Nº	Parameter	Values	Unit
VG or VGS	2 or 12	Gate bias voltage tuned to set Idq=180mA	#-0.7	V
VD1 and VD2	8 and 10	Drain bias voltage	5	V

“Power ON” sequence

1. Bias HPA gate voltage at Vg close to Vpinch-off (Typically: Vg ≈ -1.5V)
2. Apply Vds bias voltage (Typically: Vd = +5V)
3. Increase Vgs up to quiescent bias drain current Idq (pulsed applied on the gate)
4. Apply RF signal

“Power OFF” sequence

1. Turn off RF signal
2. Bias HPA gate voltage at Vg close to Vpinch-off (Typically: Vg ≈ -1.5V)
3. Turn Vds bias voltage to 0V
4. Turn Vgs bias voltage to 0V

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Recommended Operating Range [3] [4]

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	6	V
Id	Drain bias current	0.4	A
Vg	Gate bias voltage	-2 to 0	V
Pin	Maximum peak input power	11	dBm
Ta	Operating temperature range	-40 to 95	°C

[3] Electrical performances are defined for specified test conditions

[4] Electrical performances are not guaranteed over all recommended operating conditions

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Device thermal information

The device thermal performances below are based on UMS rules to evaluate the junction temperature.
This same procedure is the basis for junction temperature evaluation of the samples used to derive the Median lifetime and activation energy for the particular technology on which the CHA4314-98F is manufactured (GaAs Power HEMT 0.15µm).
The temperature Tb_{chip} is defined as the chip back side temperature. The thermal resistance (Rth_eq) is given for the full circuit, and assumes CW operation mode is given in the table.

Thermal Resistance(1)	Rth_eq	Tb_{chip} =95°C, Vd=5V, Id_drive=180mA No RF Pdiss=0.9W CW	77	°C/W
Junction Temperature	Tj		164	°C
Median Life	T50		$1.03x10^8$	Hrs

(1) Thermal resistance measured to back of the chip

Thermal Resistance(1)	Rth_eq	Tb_{chip} =95°C, Vd=5V, Id_drive=164mA No RF Pdiss=0.82W CW	77.7	°C/W
Junction Temperature	Tj		159	°C
Median Life	T50		$1.86x10^8$	Hrs

(1) Thermal resistance measured to back of the chip

Thermal Resistance(1)	Rth_eq	Tb_{chip} =95°C, Vd=5V, Id_drive=246mA Pin=9dBm Pout=25.3dBm Pdiss=0.9W CW	78.3	°C/W
Junction Temperature	Tj		165.5	°C
Median Life	T50		$8.98x10^7$	Hrs

(1) Thermal resistance measured to back of the chip

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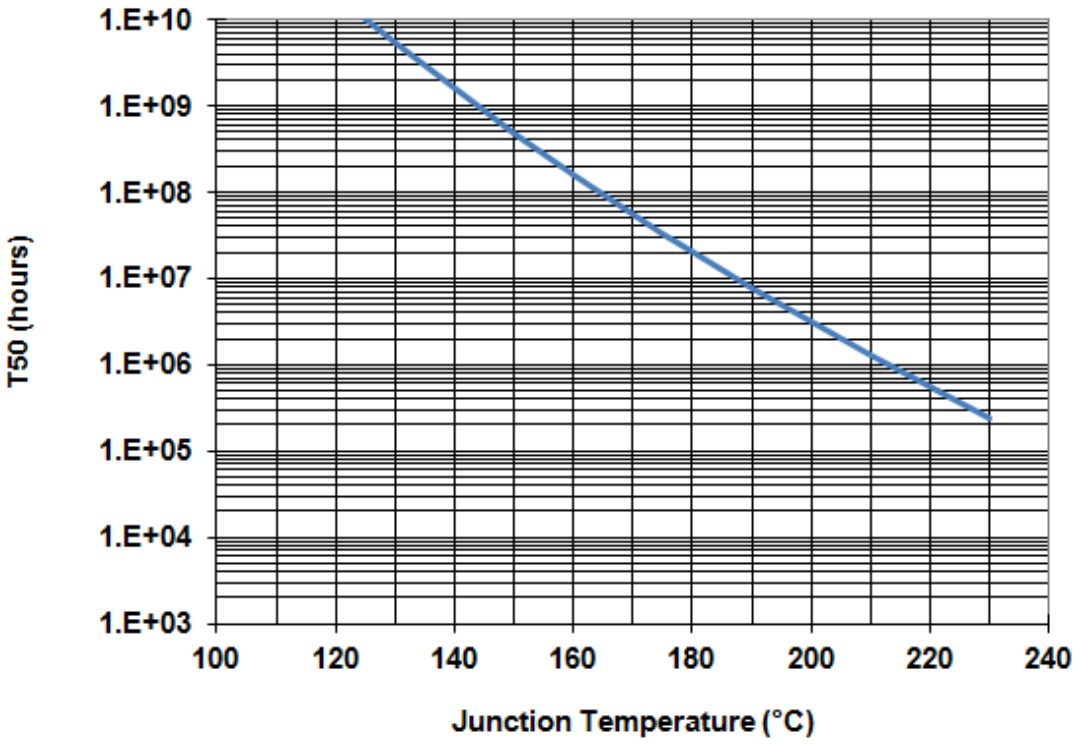

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Typical on-wafer Sij parameters

Tamb.= +25°C, Vd = +5V, Id = 180mA

Freq (GHz)	S11 (dB)	PhS11 (°)	S12 (dB)	PhS12 (°)	S21 (dB)	PhS21 (°)	S22 (dB)	PhS22 (°)
3	-11.6	-154.2	-67.0	-116.7	9.7	130.4	-4.0	-83.9
3.5	-13.3	-163.2	-62.7	-165.2	14.7	75.6	-4.9	-94.1
4	-15.6	-156.2	-58.2	155.3	17.6	22.9	-6.1	-108.8
4.5	-14.4	-144.4	-55.6	115.1	19.0	-25.1	-8.0	-123.2
5	-12.9	-149.9	-54.4	79.8	19.3	-66.7	-10.5	-135.9
5.5	-12.9	-160.7	-53.6	49.6	19.4	-102.5	-13.7	-148.7
6	-14.1	-169.7	-52.9	23.2	19.3	-134.6	-18.2	-163.6
6.5	-16.4	-172.8	-52.4	-0.8	19.2	-164.7	-26.5	166.7
7	-19.2	-160.4	-52.1	-25.5	19.2	166.4	-28.2	42.3
7.5	-19.1	-135.2	-51.6	-47.0	19.1	138.1	-20.0	10.4
8	-16.3	-123.7	-50.9	-68.8	18.9	110.3	-16.0	-4.5
8.5	-14.2	-131.0	-50.7	-94.6	18.8	84.1	-13.8	-15.7
9	-14.4	-142.7	-50.6	-115.8	18.8	57.1	-12.2	-25.5
9.5	-16.4	-151.5	-50.3	-137.0	18.9	28.9	-11.1	-35.2
10	-22.1	-147.9	-49.9	-160.1	18.9	-0.5	-10.4	-44.8
10.5	-22.2	-54.6	-49.6	175.6	18.9	-32.6	-10.0	-55.4
11	-12.6	-47.9	-49.3	148.0	18.6	-67.4	-10.1	-68.0
11.5	-7.5	-62.4	-49.6	116.8	17.9	-104.6	-11.2	-85.4
12	-4.6	-79.5	-50.7	83.5	16.6	-144.6	-15.1	-114.5
12.5	-2.9	-100.7	-52.8	50.5	14.5	171.9	-21.1	124.3
13	-2.0	-109.9	-56.0	19.4	11.0	127.2	-9.2	49.2
14	-1.2	-132.2	-64.6	-31.5	-1.7	50.7	-2.0	-12.3
15	-1.0	-149.2	-73.6	-86.8	-21.4	63.3	-0.7	-46.9
16	-0.8	-164.7	-68.8	-147.7	-20.0	93.3	-0.5	-68.1
17	-0.8	-179.9	-64.9	146.9	-24.7	71.5	-0.5	-83.9
18	-0.9	163.8	-65.0	99.4	-36.3	103.9	-0.5	-97.2
19	-1.2	144.8	-65.0	82.9	-27.2	156.4	-0.6	-108.7
20	-1.8	120.7	-64.9	73.5	-22.0	134.1	-0.7	-120.3
21	-3.0	88.4	-62.7	50.1	-19.4	103.2	-0.9	-131.7
22	-4.1	51.3	-65.0	13.4	-18.0	71.3	-1.1	-144.0
23	-4.2	0.2	-67.6	-1.0	-17.1	36.0	-1.4	-159.9
24	-3.4	-44.9	-71.0	-16.4	-17.2	2.5	-2.1	-177.1
25	-2.5	-78.0	-70.2	4.9	-17.8	-32.7	-2.8	162.8
26	-2.2	-101.6	-69.0	-47.6	-18.7	-66.5	-4.4	125.6
27	-1.8	-119.0	-65.9	-112.2	-20.1	-106.0	-6.1	65.1
28	-1.5	-132.2	-67.7	165.9	-22.7	-143.9	-5.0	-1.2
29	-1.3	-144.0	-67.6	141.1	-26.1	-175.3	-3.1	-46.0
30	-1.2	-153.9	-64.7	119.5	-29.7	162.4	-1.9	-74.0
31	-1.2	-162.8	-69.0	125.1	-33.5	149.0	-1.3	-93.8
32	-1.2	-169.7	-53.9	108.0	-34.3	129.5	-0.9	-108.7
34	-1.1	175.4	-58.4	11.1	-40.5	90.5	-0.8	-134.2

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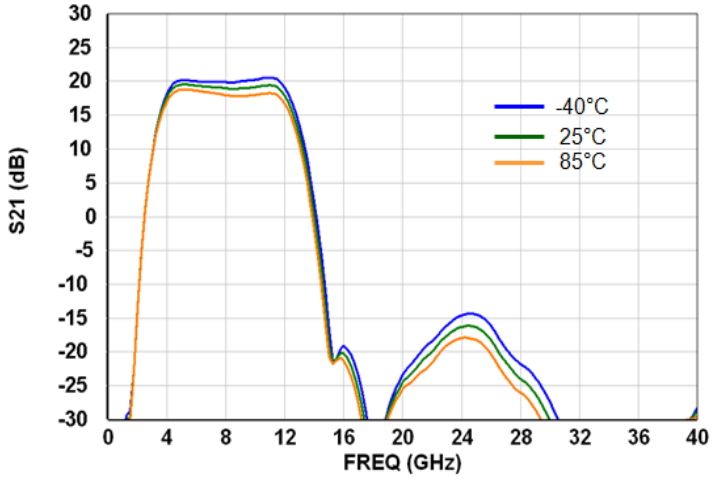
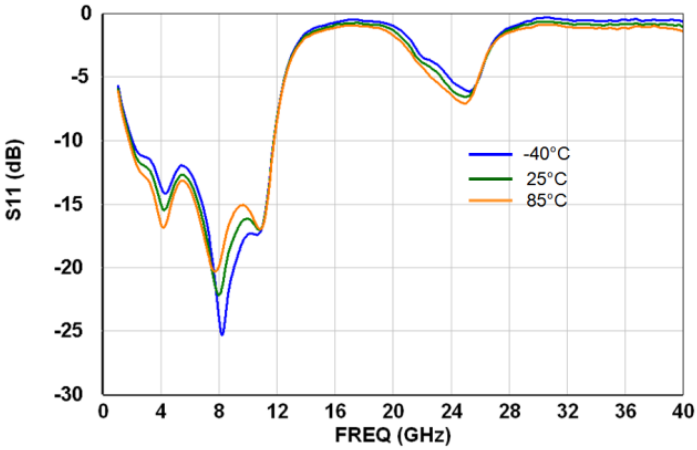
Typical Test Fixture Measurements

Vd = +5V, Vg fixed to set Idq = 180mA @ Tbackside = 25°C

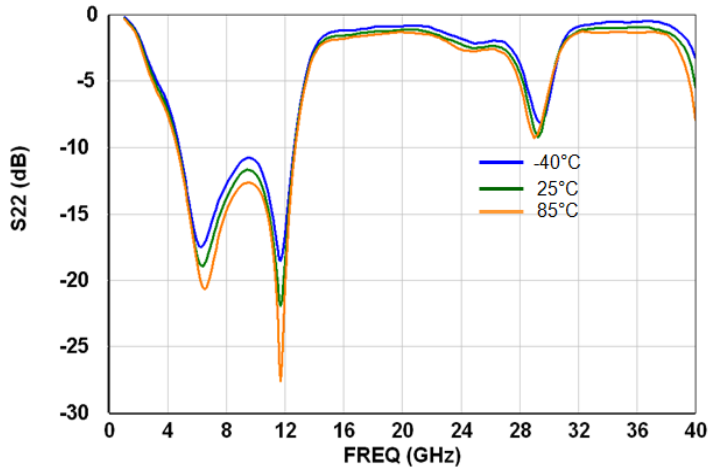
Wide frequency range Linear Gain



Wide frequency range Input Return Losses



Wide frequency range Output Return Losses



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Typical Test Fixture Measurements

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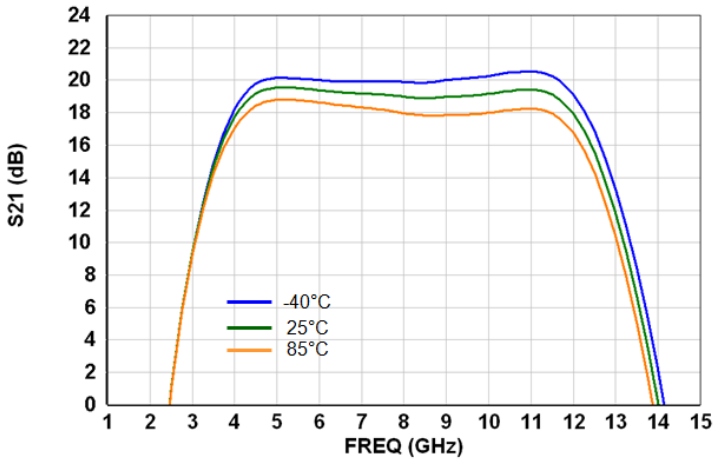
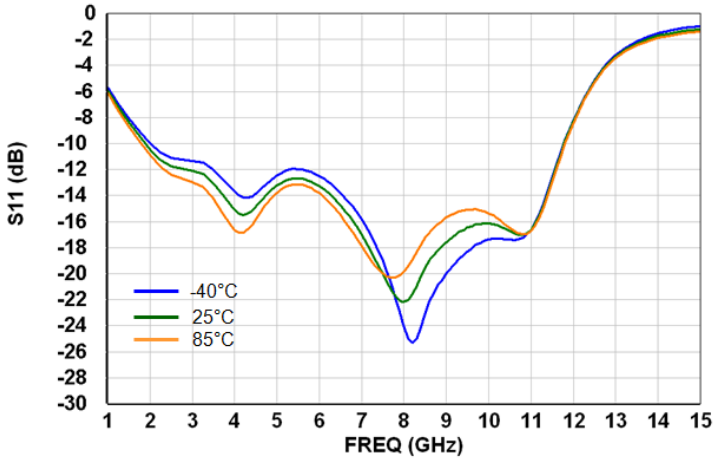
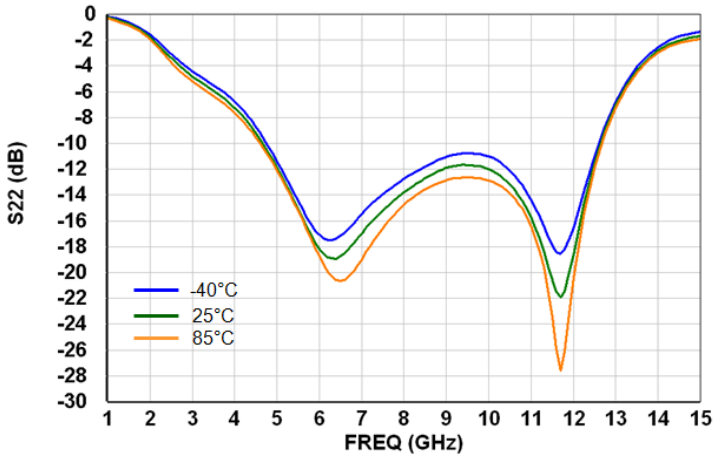
Linear Gain



Input Return Losses



Output Return Losses



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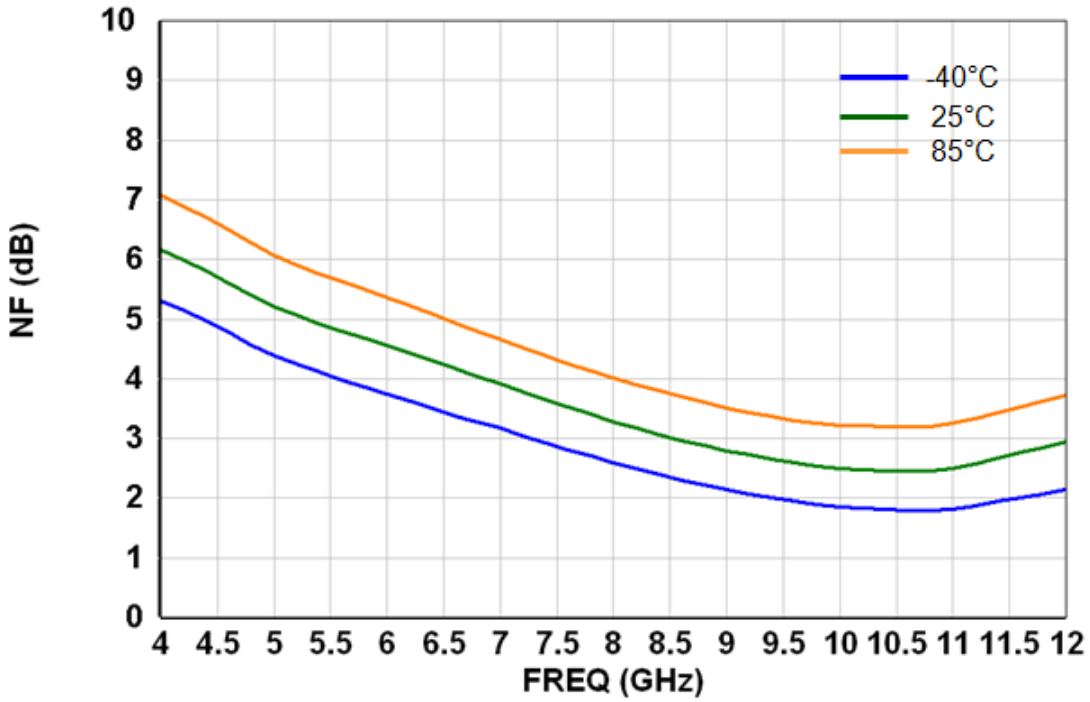
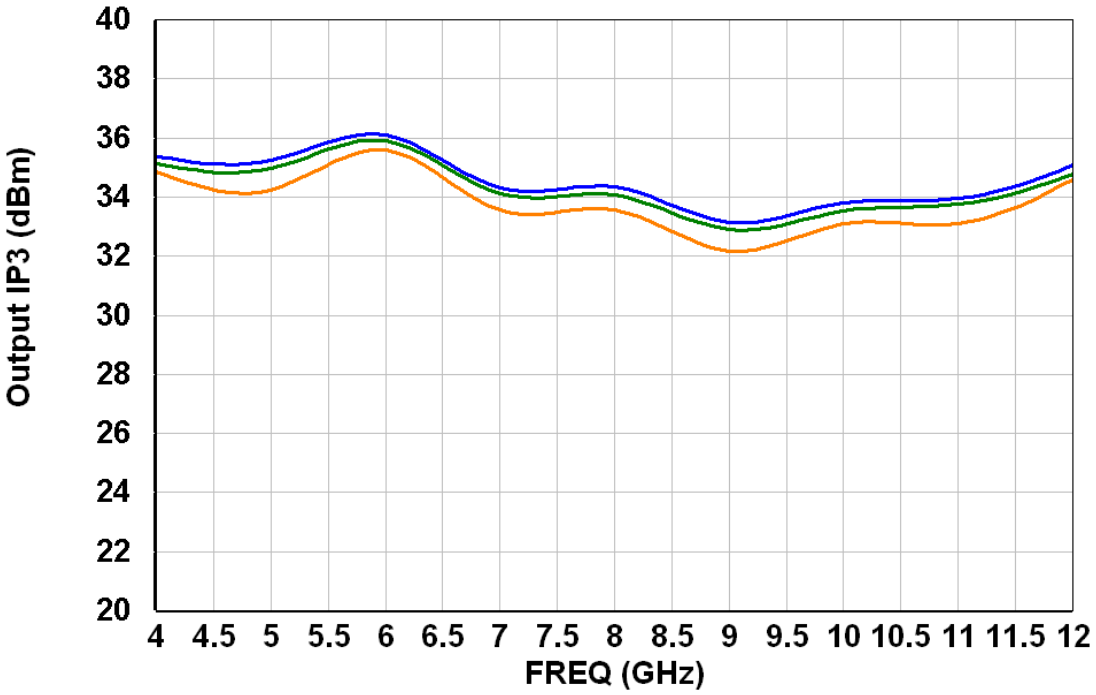
Typical Test Fixture Measurements

Vd = +5V, Vg fixed to set Idq = 180mA @ Tbackside = 25°C

NF



Output IP3



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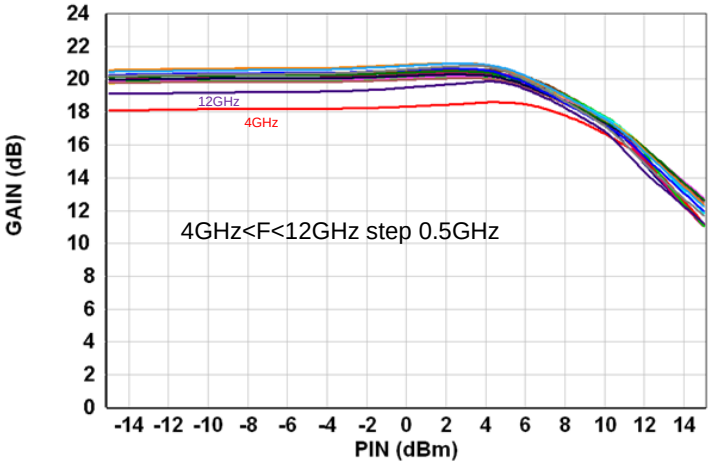
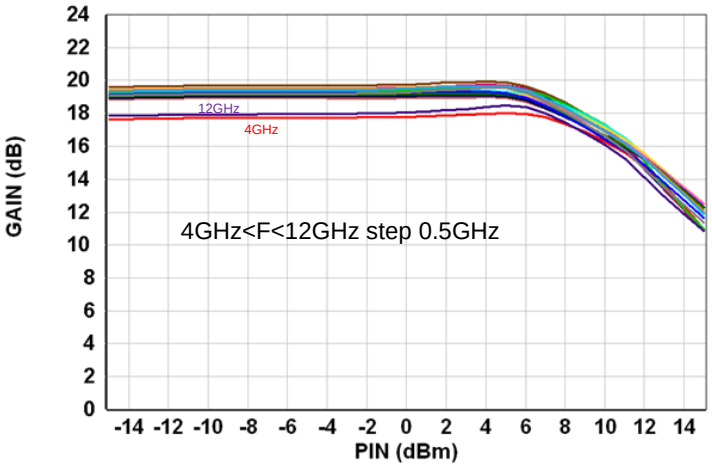
Typical Test Fixture Measurements

Vd = +5V, Vg fixed to set Idq = 180mA @ Tbackside = 25°C

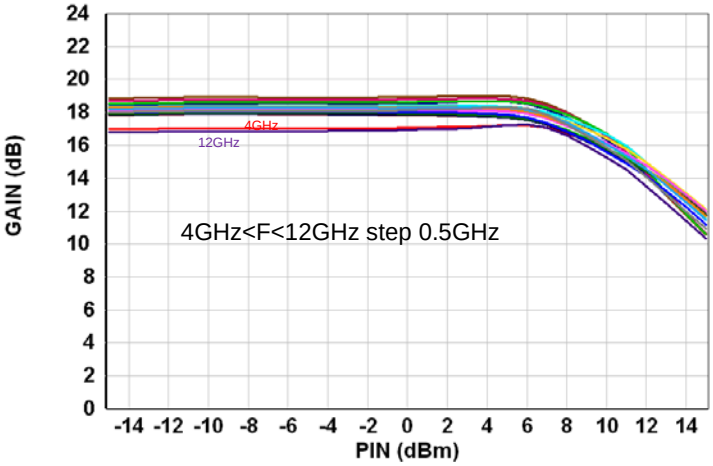
Gain versus Pin at Tbackside = -40°C



Gain versus Pin at Tbackside = 25°C



Gain versus Pin at Tbackside = 85°C



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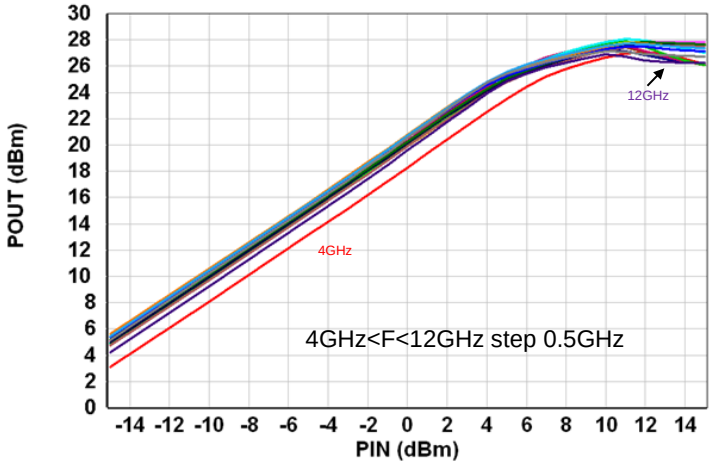
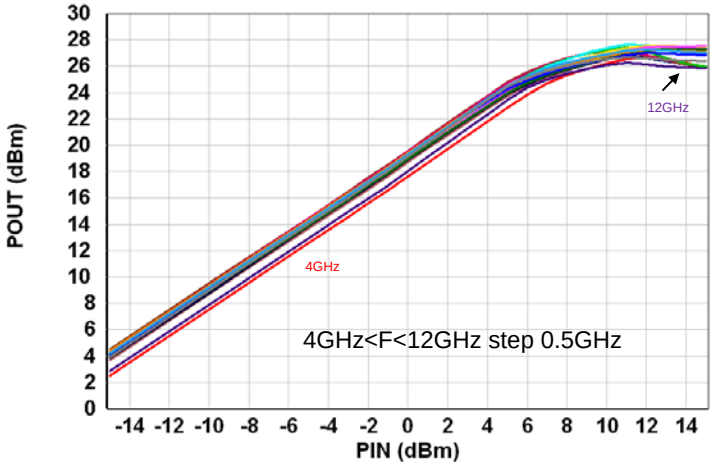
Typical Test Fixture Measurements

Vd = +5V, Vg fixed to set Idq = 180mA @ Tbackside = 25°C

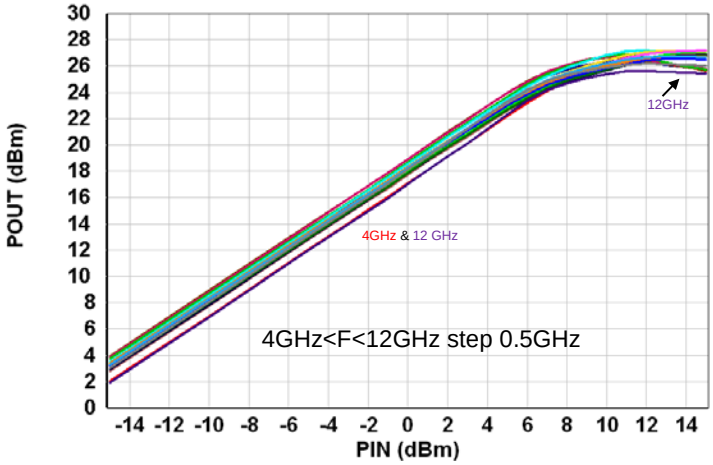
Pout versus Pin at Tbackside = -40°C



Pout versus Pin at Tbackside = 25°C



Pout versus Pin at Tbackside = 85°C



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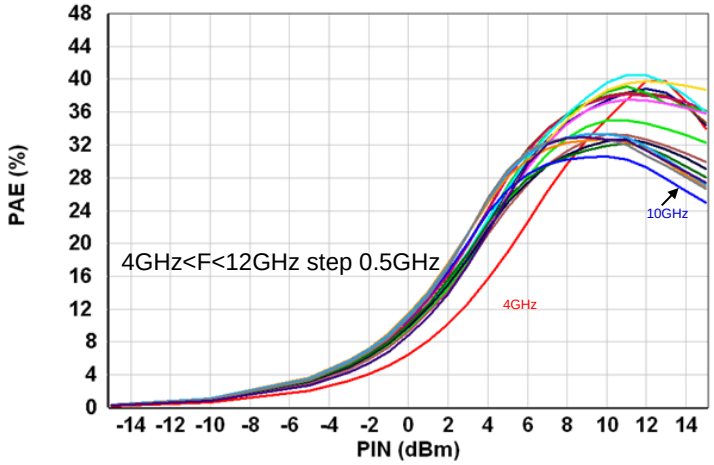
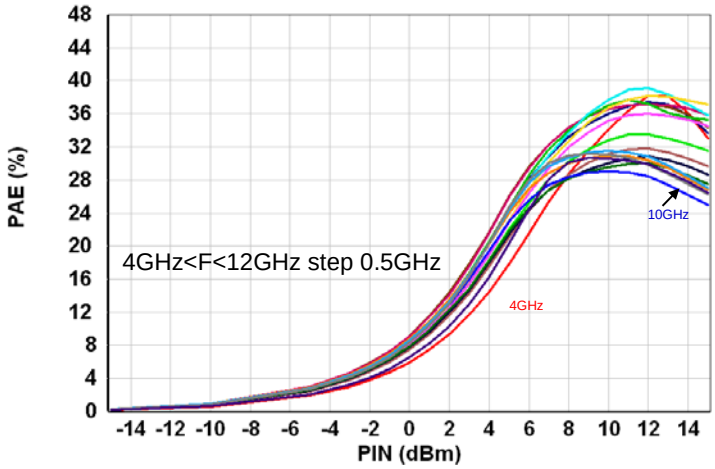
Typical Test Fixture Measurements

Vd = +5V, Vg fixed to set Idq = 180mA @ Tbackside = 25°C

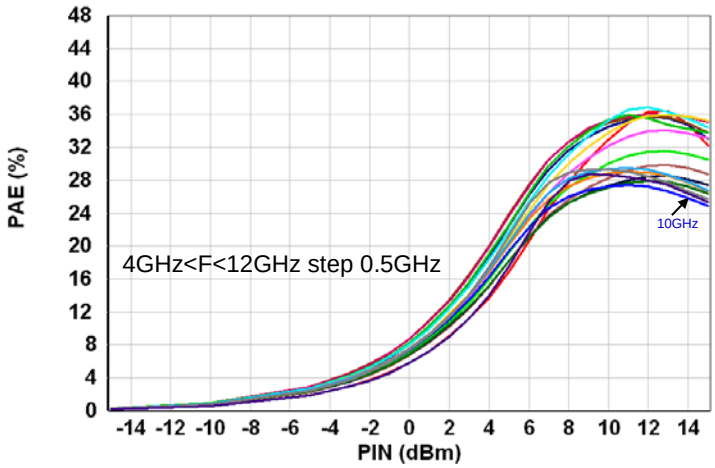
PAE versus Pin at Tbackside = -40°C



PAE versus Pin at Tbackside = 25°C



PAE versus Pin at Tbackside = 85°C



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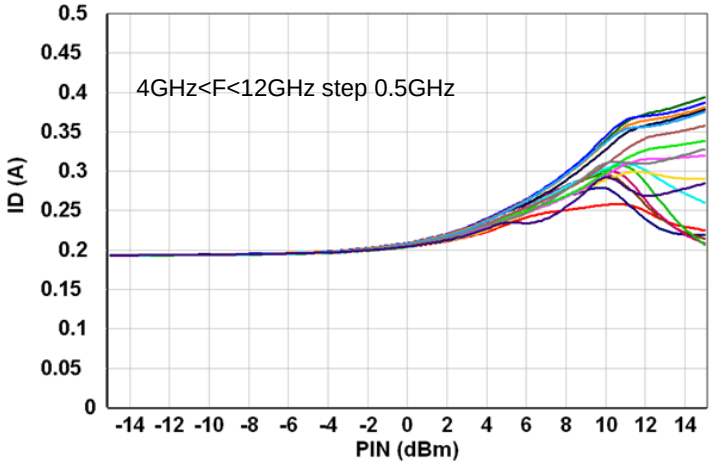
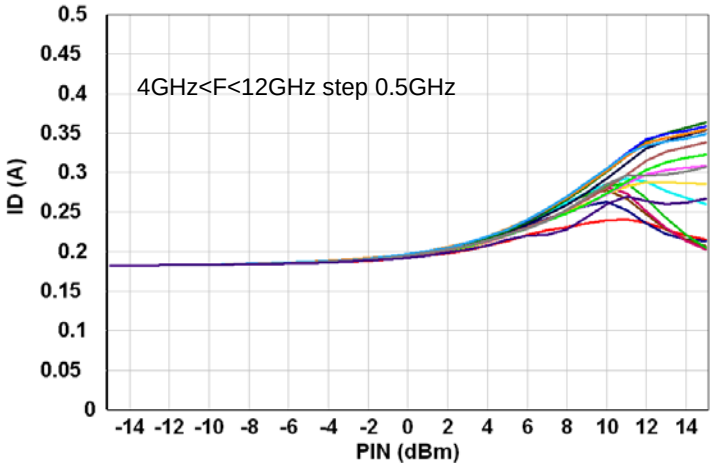
Typical Test Fixture Measurements

Vd = +5V, Vg fixed to set Idq = 180mA @ Tbackside = 25°C

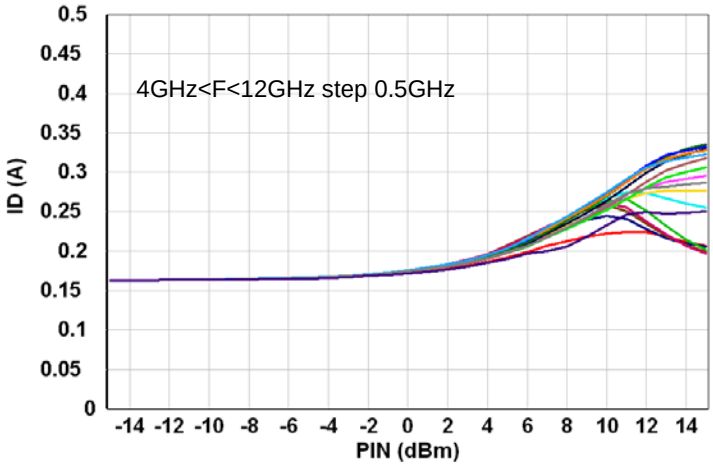
ID versus Pin at Tbackside = -40°C



ID versus Pin at Tbackside = 25°C



ID versus Pin at Tbackside = 85°C



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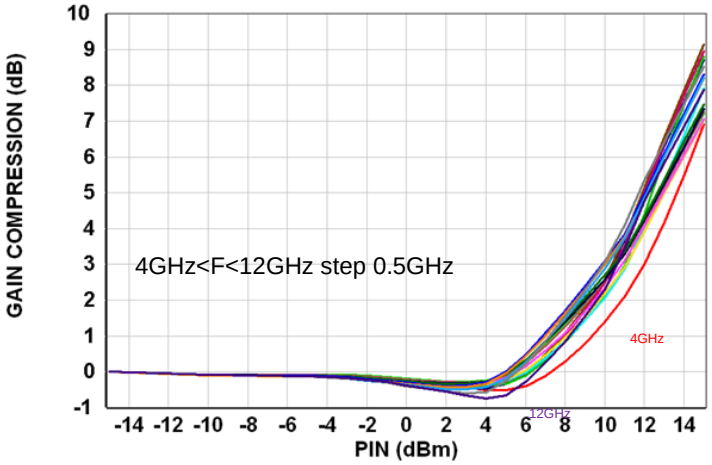
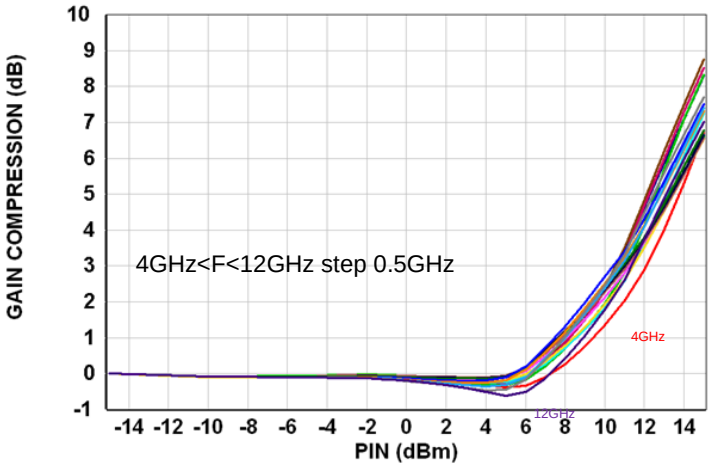
Typical Test Fixture Measurements

Vd = +5V, Vg fixed to set Idq = 180mA @ Tbackside=25°C

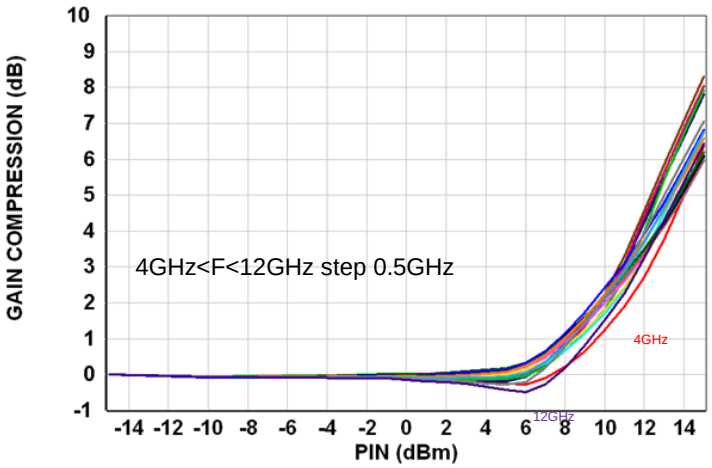
Gain compression versus Pin at Tbackside = -40°C



Gain compression versus Pin at Tbackside = 25°C



Gain compression versus Pin at Tbackside = 85°C



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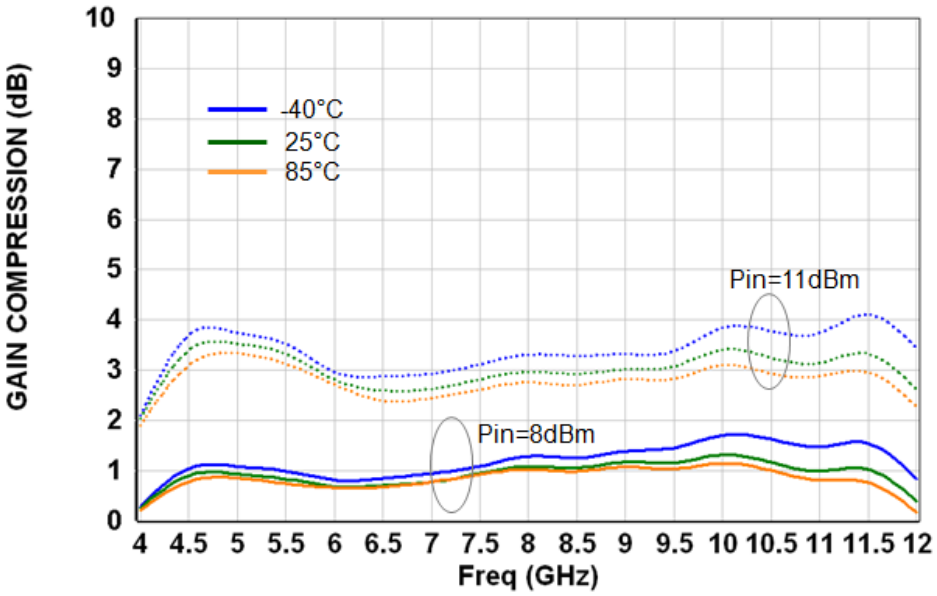
Typical Test Fixture Measurements

Vd = +5V, Vg fixed to set Idq = 180mA @ Tbackside = 25°C

Gain compression versus Frequency at Pin = 8dBm and 11dBm



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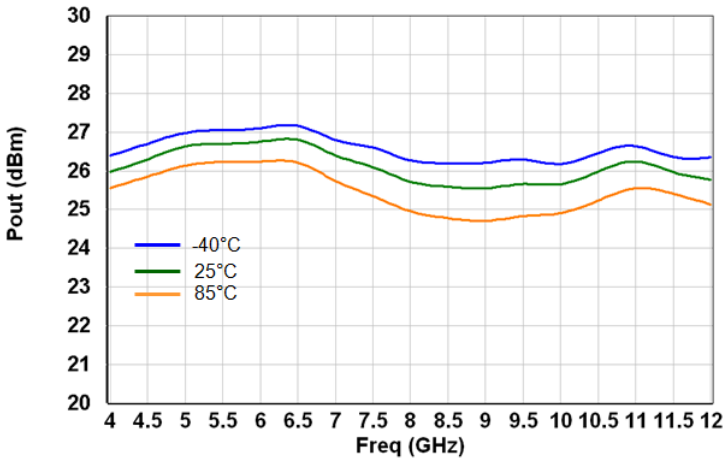
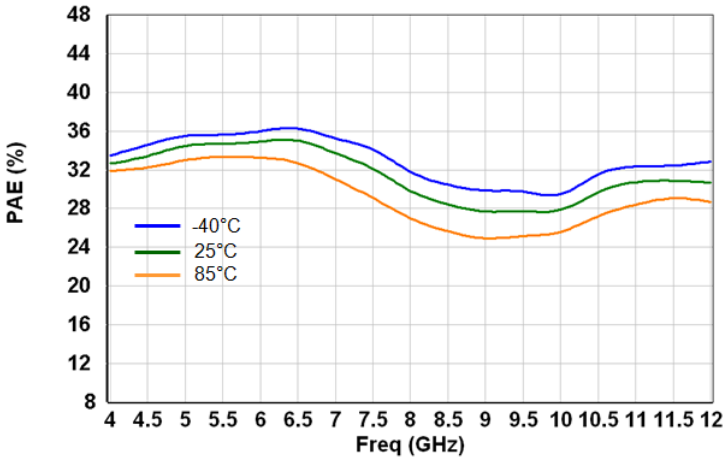
Typical Test Fixture Measurements

Vd = +5V, Vg fixed to set Idq = 180mA @ Tbackside = 25°C

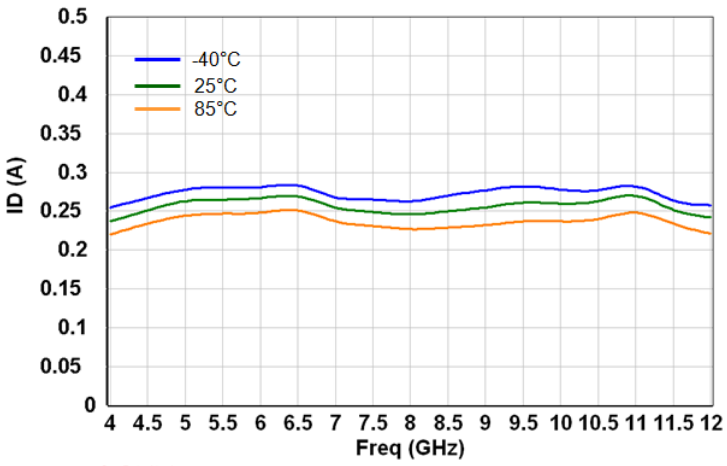
Output power at 1dB gain compression



PAE at 1dB gain compression



ID at 1dB gain compression



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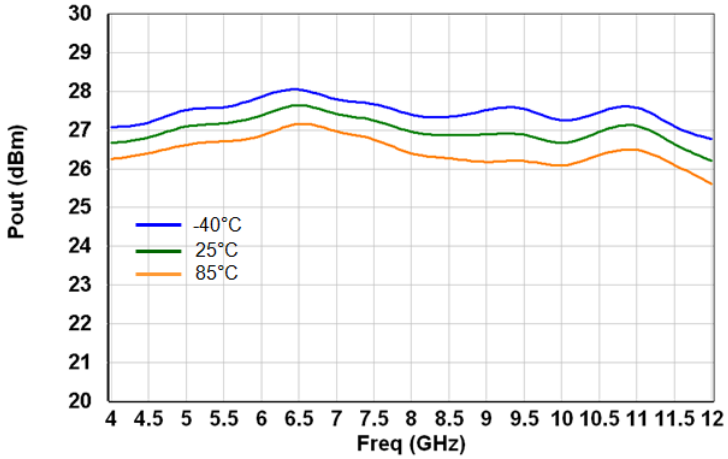
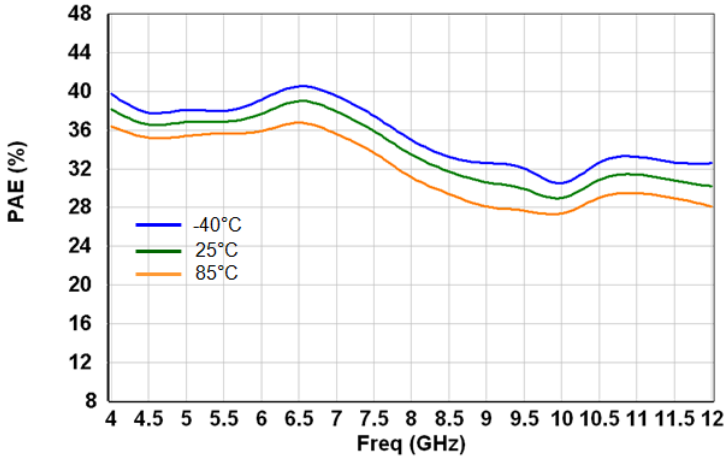
Typical Test Fixture Measurements

Vd = +5V, Vg fixed to set Idq = 180mA @ Tbackside = 25°C

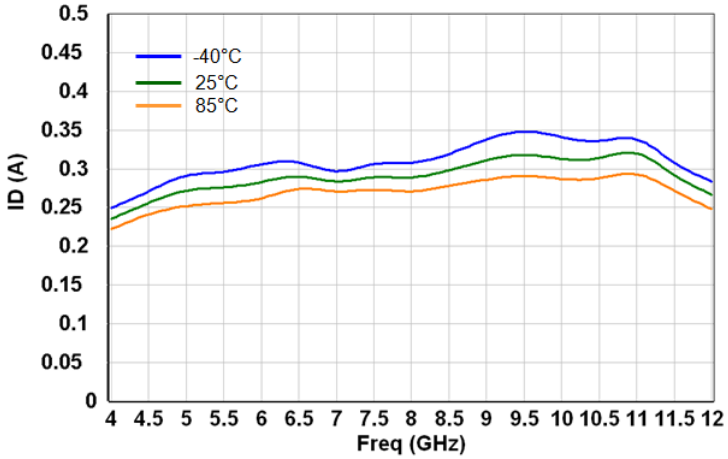
Output power at 3dB gain compression



PAE at 3dB gain compression



ID at 3dB gain compression



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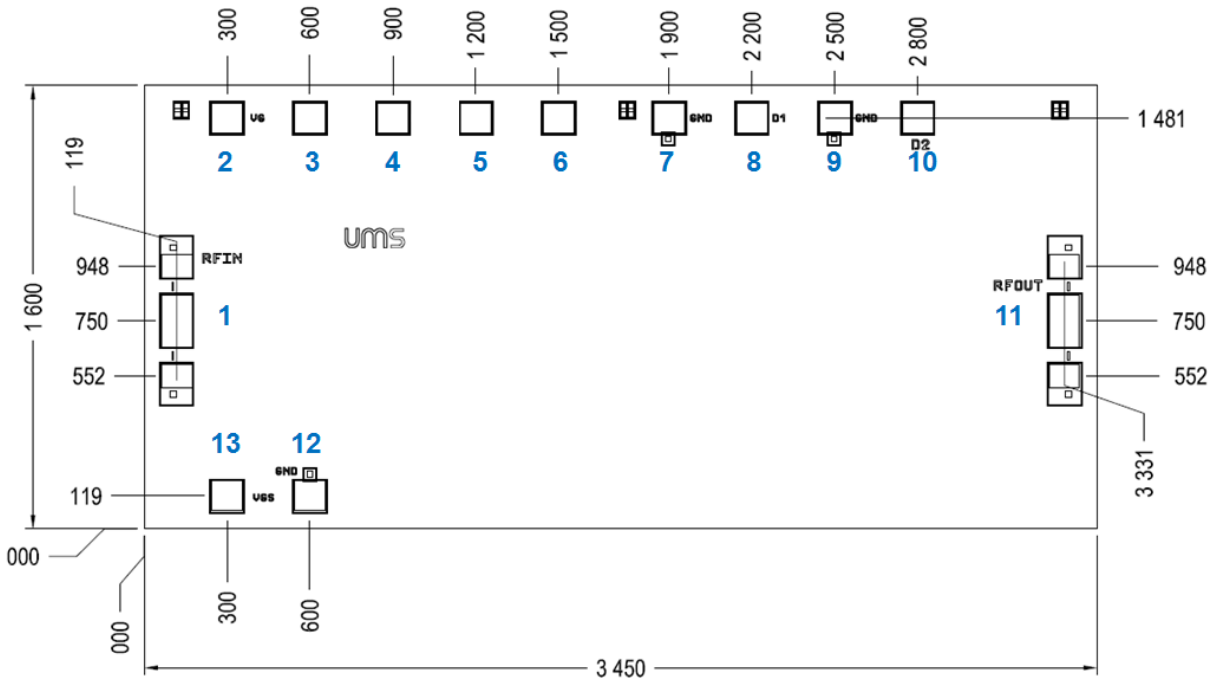
Mechanical data



Chip size = 3450x1600 ±35µm
Chip thickness = 70µm ±7µm
RF pads (1, 11) = 108 x 186µm²
DC pads (2, 3, 4, 5, 6, 7, 8, 9,10, 12, 13) = 110 x 108µm²

PAD Number	Name	Description
1	RFIN	Input RF port
2	VG	Negative supply voltage (gate of stages 1 and 2)
3,4,5,6	Not used	Not connected
7,9,12	GND	Ground (NC)
8	D1	Positive supply voltage (drain of stage 1)
10	D2	Positive supply voltage (drain of stage 2)
11	RFOUT	Output RF port
13	VGs	Negative supply voltage (gate of stages 1 and 2)

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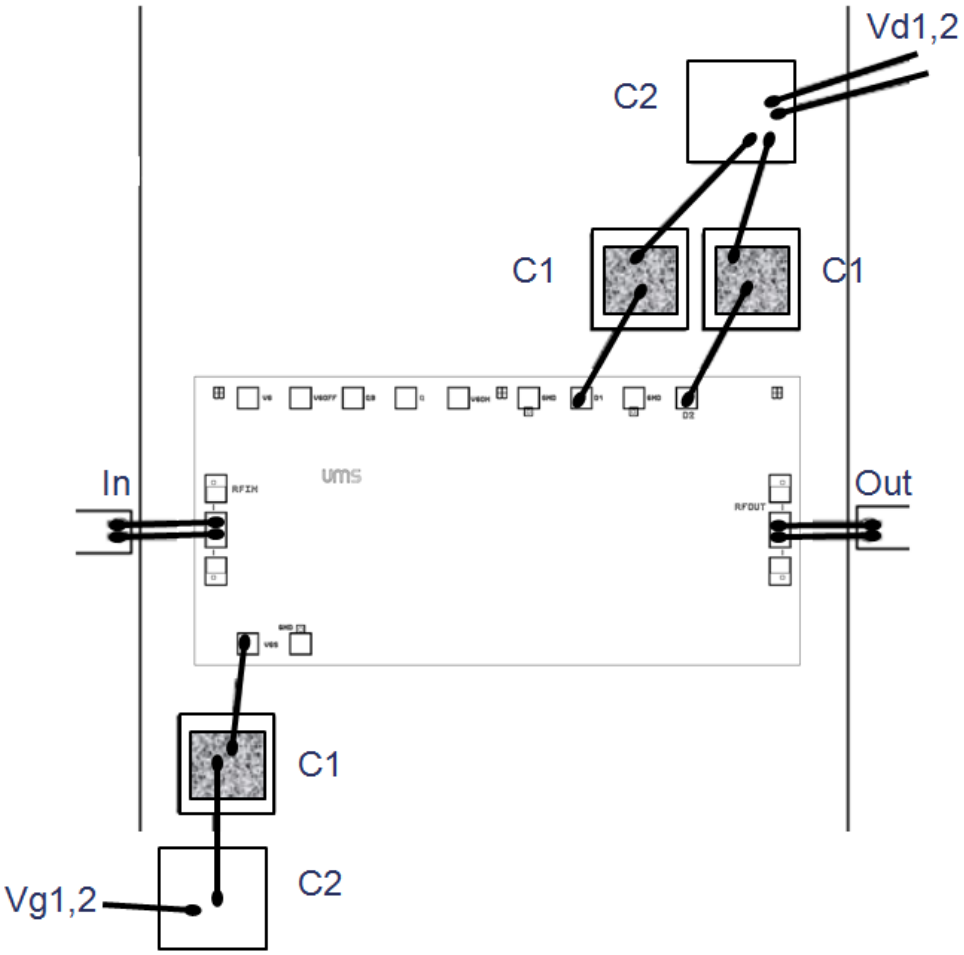
Recommended assembly plan



25µm wedge bonding is preferred

Note: Supply feed should be bypassed. 25µm diameter gold wire is to be preferred.

Bill of Materials

Label	Value	Description
C1	RF	Capa 120pF ±10% 50V
C2	RF	Capa 470pF ±5% 50V

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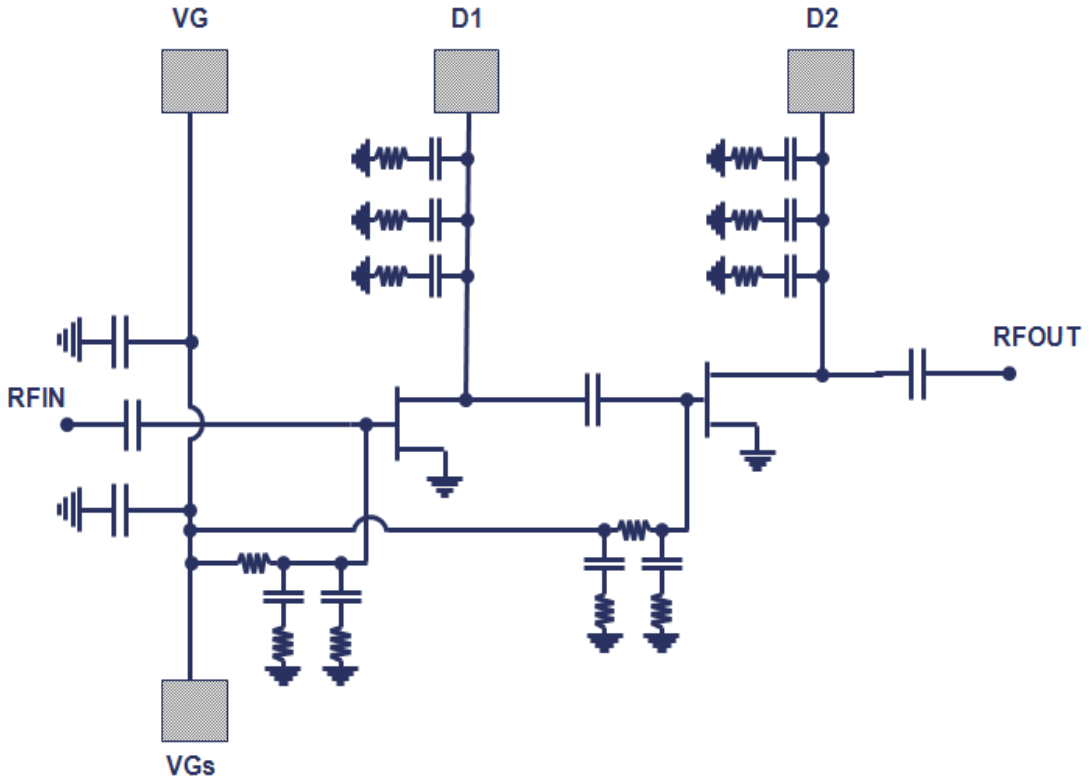
Recommended circuit bonding table

Label	Type	Decoupling	Comment
RFIN	RF	Not required	Inductance (Lbonding) = 0.4nH 2 gold wires with diameter of 25 µm (600µm)
RFOUT	RF	Not required	Inductance (Lbonding) = 0.4nH 2 gold wires with diameter of 25 µm (600µm)
Vd1,2 (D1 & D2)	DC	120pF, 470pF	Inductance ≤ 1nH (mainly for first decoupling level) ⇒1.2mm length wires with a diameter of 25 µm
Vg1,2 (VG & VGs)	DC	120pF, 470pF	Inductance ≤ 1nH (mainly for first decoupling level) ⇒1.2mm length wires with a diameter of 25 µm

- The overall biasing network proposed is compliant with CW mode. For a DC pulse applied on the gate or drain; it can be integrated differently depending on module technology and on modulation characteristics (gate or drain pulse, pulse length and Duty Cycle). However, the first decoupling level should always be kept, the second one should be adapted to modulator characteristics. A third one could be added and should be kept and optimized on the non-modulated ports.

DC Schematic



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Recommended ESD management

Refer to the application note AN0020 available at https://www.ums-rf.com for ESD sensitivity and handling recommendations for the UMS products.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at https://www.ums-rf.com.

Ordering Information

Chip form:	CHA4314-98F/00

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