

27.5-43.5GHz Low Noise Amplifier

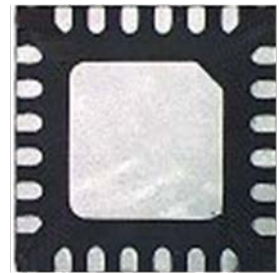
GaAs Monolithic Microwave IC in SMD leadless package

Description

The CHA2595-QDG is a wide band monolithic Low Noise Amplifier with State of the art wide band, low noise, adjustable gain performance.

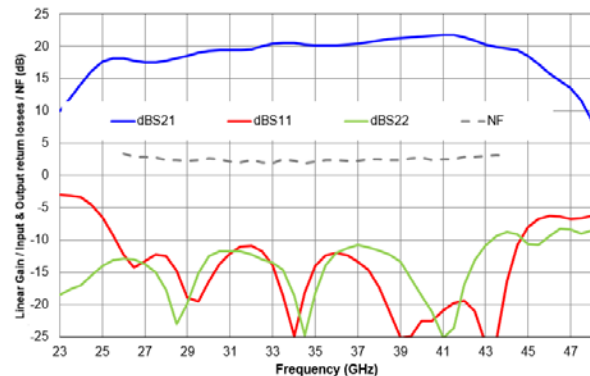
It is designed for a wide range of applications, from military to commercial communication and test instrumentation systems.

It is manufactured with a successfully space evaluated pHEMT process, 100nm gate length, via holes through the substrate, air bridges and electron beam gate lithography. It is supplied in RoHS compliant low cost SMD package.



Main Features

- Broadband performances: 27.5-43.5GHz
- Typical Linear Gain: 19.5dB
- Typical Noise Figure: 2.3dB
- P_{1dB}: 11dBm
- P_{sat}: 12dBm
- OIP3: >20dBm
- DC bias: V_d=3.3V@I_d=61mA,
- 24L QFN 4x4
- MSL1



Main Electrical Characteristics

T_{amb}. = +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	27.5		43.5	GHz
Gain	Linear Gain	18	19.5		dB
NF	Noise Figure		2.3	3.1	dB
P _{1dB}	Output Power @1dB gain comp.	8	11	13.5	dBm

Electrical Characteristics

Tamb.= +25°C, Vd (D) = 3.3V, Vg (G1=G2=G3) set in order to get Idq = 61mA (≈0V)

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	27.5		43.5	GHz
Gain	Linear Gain				dB
	27.5GHz		17.0		
	29GHz		19.0		
	32GHz		20.0		
	38GHz		21.0		
	42GHz		21.5		
NF	Noise Figure				dB
	27.5GHz		2.5		
	29GHz		2.3		
	32GHz		2.2		
	38GHz		2.8		
	43.5GHz		3.1		
IRL	Input return loss		10		dB
ORL	Output return loss		10		dB
P _{1dB}	Output power at 1dB gain comp				dBm
	27.5GHz		8.0		
	29-32GHz		>9.5		
	33-38GHz		>11		
	39-43GHz		>12		
P _{sat}	Output power at 3dB gain comp				dBm
	27.5GHz		9.0		
	29-32GHz		>10.5		
	33-38GHz		>11.5		
	39-43GHz		>13.5		
OIP3	Output 3 rd order intercept point		20		dBm
Vd	Drain bias voltage	3.0	3.3	3.5	V
Id	Drain bias current		61		mA

These values are representative of on-board measurements as defined on the drawing in paragraph "Evaluation mother board".

Absolute Maximum Ratings ⁽¹⁾T_{amb.} = +25°C

Symbol	Parameter	Values	Unit
V _d	Drain bias voltage	4.0	V
V _g	Gate bias voltage	-1.5 to +0.4	V
P _{in}	RF input power	0	dBm
T _j	Maximum Junction temperature ⁽²⁾	175	°C

⁽¹⁾ Operation of this device above any one of these parameters may cause permanent damage.

⁽²⁾ Thermal Resistance channel to ground paddle (see "Device thermal performances" in the following)

Recommended Operating Range ^{3, 4}

Symbol	Parameter	Values	Unit
V _d	Drain bias voltage	3.0 to 3.6	V
I _{dq}	Drain bias current	60 to 90	mA
V _g	Gate bias voltage	-0.5 to 0.2	V
P _{in}	Input power range	-2	dBm

⁽³⁾ Electrical performances are defined for specified test conditions

⁽⁴⁾ Electrical performances are not guaranteed over all recommended operating conditions

Temperature Range

Ta	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +150	°C

Typical Bias Conditions

Tamb.= +25°C

Symbol	Pad N°	Parameter	Values	Unit
D	15	DC Drain voltage all stages	3.3	V
G* ⁽¹⁾	14	DC Gate voltage all stages	≈0	V

⁽¹⁾ Can be adjusted to set Id = 61mA.

“Power ON” sequence

1. Ground the device
2. Bias circuit gate voltage at Vg low enough (Typically Vg ≈ -1V)
3. Apply Vds bias Voltage (Typically Vd to 3.3V)
4. Increase slowly Vgs up to quiescent bias drain current Idq
5. Apply RF signal

“Power OFF” sequence

1. Turn RF power supply off
2. Bias circuit gate voltage at Vg low enough (Typically Vg ≈ -1V)
3. Turn Vds Bias voltage to 0V
4. Set Vg to -1V in order to get Idq = 0mA
5. Set Vg to 0V

Device thermal performances

All the figures given in this section are obtained assuming that the QFN device is only cooled down by conduction through the package thermal pad (to be adapted to the assembly / package) (no convection mode considered).

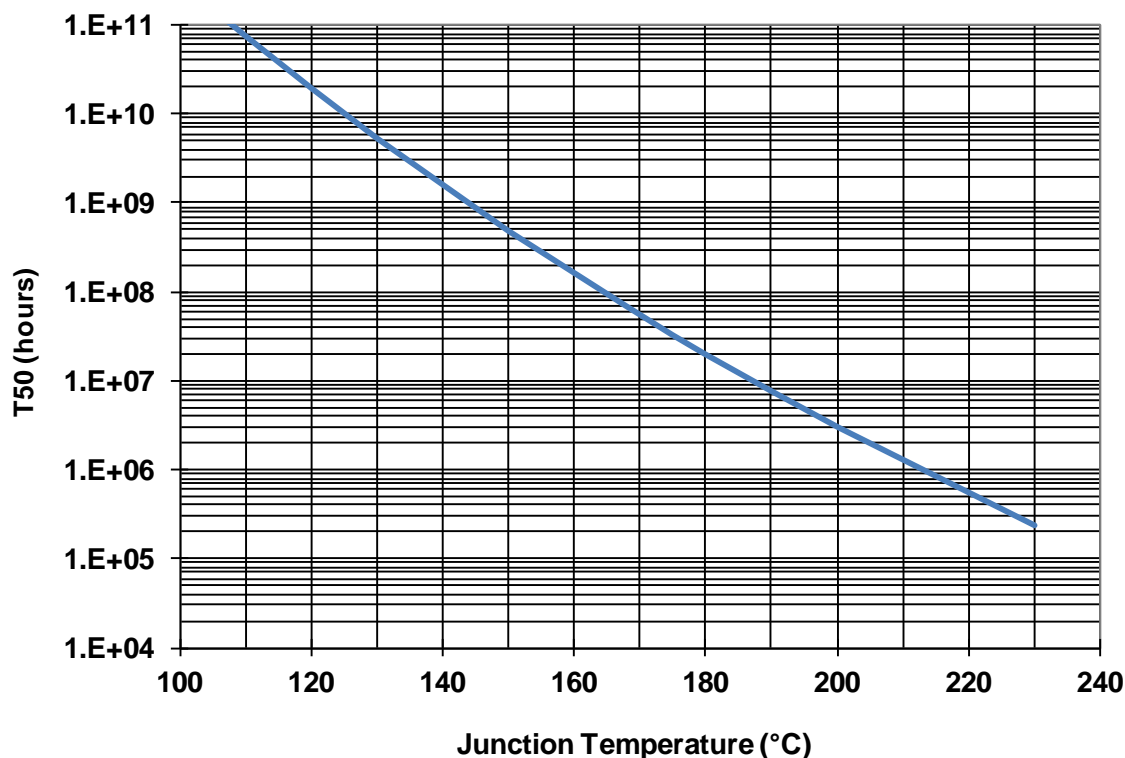
The temperature is monitored at the package back-side interface (T_{case}).

The system maximum temperature must be adjusted in order to guarantee that $T_{junction}$ remains below the maximum value specified in the Absolute Maximum Ratings table.

So, the system PCB must be designed to comply with this requirement.

Parameter	Biasing conditions	Tjunction (°C)	R _{TH} (°C/W)	T50 (hours)
R _{TH} ⁽¹⁾ Thermal Resistance (Junction to Case)	Vd = 3.3V Id = 61mA P _{diss} = 0.2W	103	79	3.6e ¹¹

(1) Assuming 85°C T_{case}



Typical Package Sij parameters

Tamb.= +25°C, Vd = +3.3V, Id =61mA

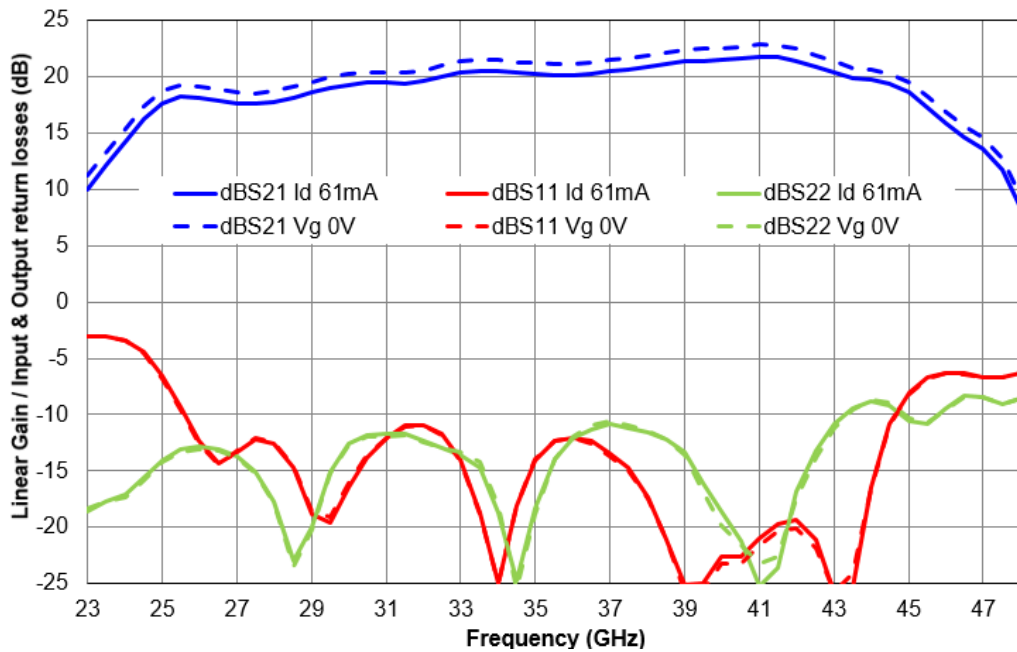
Freq (GHz)	S11 (dB)	PhS11 (°)	S12 (dB)	PhS12 (°)	S21 (dB)	PhS21 (°)	S22 (dB)	PhS22 (°)
4	-2.27	85.13	-58.7	32.4	-46.45	137.99	-3.22	109.69
6	-9.94	77.56	-62.78	-13.07	-37.5	-24.43	-2.31	82.3
8	-6.35	81.82	-61.72	-47.09	-31.19	-100.63	-3.01	51.7
10	-4.37	55.5	-58.63	-24.75	-23.18	-167.83	-3.75	24.81
12	-3.02	23.25	-62.98	-118.76	-18.06	117	-4.25	-3.32
13	-2.52	5.11	-63.76	-70.18	-16.7	82.19	-4.43	-19.41
14	-2.12	-13.72	-54.64	-130.36	-15.83	52.07	-4.56	-37.21
15	-1.82	-33.7	-54.61	143.79	-14.96	29.08	-4.87	-56.02
16	-1.59	-53.79	-56.77	123.86	-13.39	7.81	-5.3	-75.19
17	-1.38	-73.82	-54.79	83.06	-11.32	-12.85	-5.78	-94.81
18	-1.23	-94.56	-53.38	61.48	-8.86	-33.55	-6.29	-113.04
19	-1.17	-115.05	-52.41	15.02	-5.96	-55.12	-6.98	-130.58
20	-1.07	-135.09	-56.79	-16.38	-2.47	-78.96	-8.02	-148.61
21	-1.04	-157.48	-57.88	42.64	1.27	-106.92	-9.18	-164.98
22	-1.03	178.29	-54.36	2.63	5.25	-138.12	-10.82	-178.78
23	-1.3	149.13	-54.65	23.06	9.54	-173.39	-13.01	173.17
24	-2.06	107.64	-53.9	65.6	14.27	142.86	-14.62	-178.53
25	-6.7	34.23	-42.93	67.93	18.12	81.66	-12.17	-174.15
26	-12.82	-117.35	-39.12	16.98	18.17	18.44	-10.58	169.81
27	-9.45	166.48	-39.14	-15.55	16.97	-25.89	-9.93	154.76
28	-9.1	130.94	-38.73	-39.16	16.85	-60.87	-9.63	134.88
29	-10.73	109.09	-39.93	-41.5	17.83	-95.7	-10.65	118.89
30	-12.47	109.05	-37.89	-61.97	19.36	-136.23	-12.51	101.16
31	-9.93	120.08	-37.38	-107.98	20.28	176.6	-14.01	115.24
32	-9.16	95.72	-37.64	-126.03	19.7	131.51	-11	105.81
33	-9.03	71.02	-45.13	-169.26	19.33	96.79	-12.67	89.47
34	-9.83	56.68	-47.9	-168.91	19.98	58.49	-11.66	84.59
35	-10.77	43.87	-58.39	-90.28	20.57	16.56	-11.06	74.31
36	-12.34	46.21	-47.08	-101.18	20.35	-26.46	-11.81	58.95
37	-12.63	52.43	-46.4	-121.62	20.49	-63.66	-11.74	64.31
38	-12.24	47.86	-50.12	-131.24	20.89	-84.3	-10.78	57.35
39	-11.48	27.65	-52.35	-141.48	21.02	-150.25	-14.48	58.28
40	-16.91	21.06	-46.45	-82.25	21.06	165.29	-11.24	68.21
41	-17.04	62.35	-45.15	-70.44	21.21	118.91	-8.49	62.16
42	-13.73	73.06	-38.42	-101.53	20.7	69.13	-7.5	50.79
43	-13.93	72.29	-37.59	-136.18	20.47	21.26	-7.38	26.07
44	-9.65	93.75	-38.98	-159.09	20.14	-39.07	-10.59	15.3
45	-5.75	73.79	-39.47	-148.24	17.64	-100.79	-11.56	45.25

Typical Board Measurements

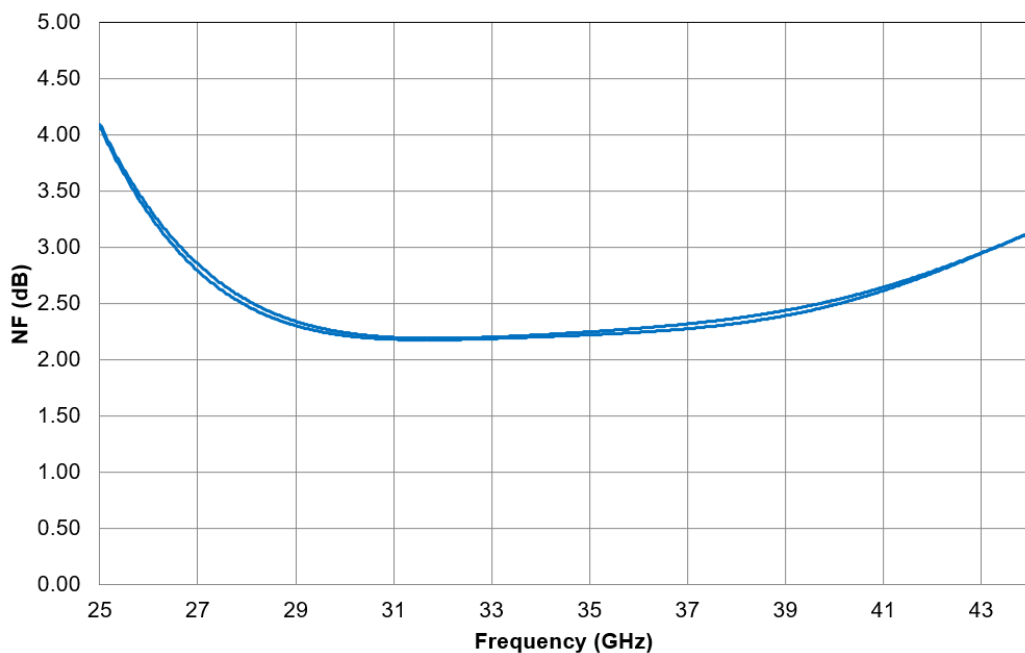
Tamb.= +25°C, Vd = 3.3V

Losses due to board are de-embedded. Measurements are given in the QFN's access plan

Linear Gain and Return Losses versus Frequency
Vd = 3.3V, Vg = 0V and set in order to get Idq = 61mA



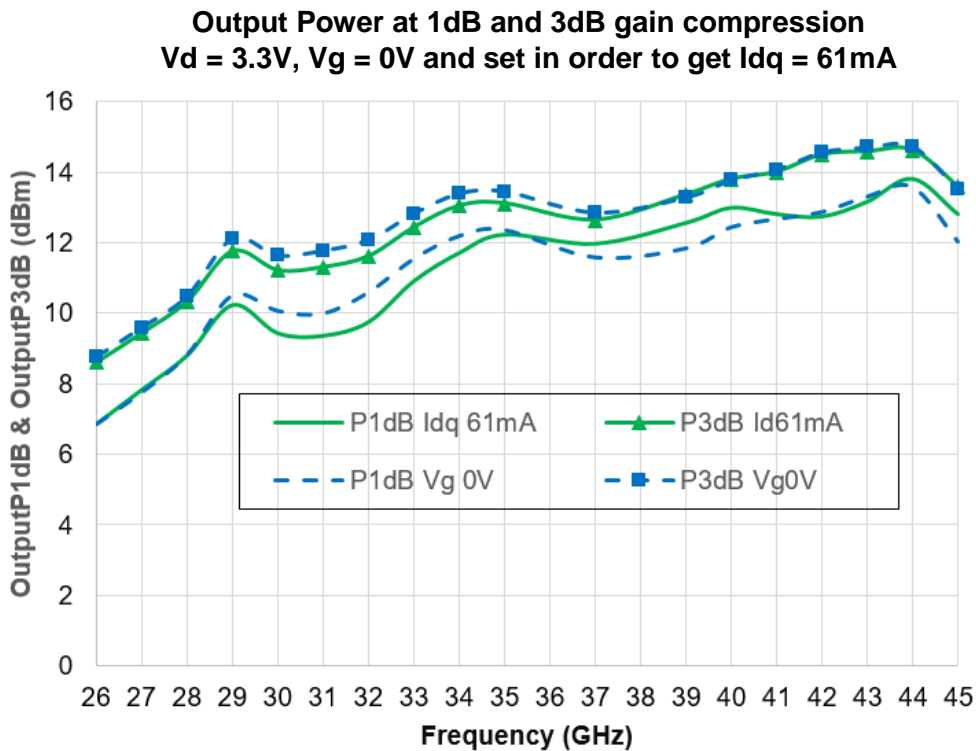
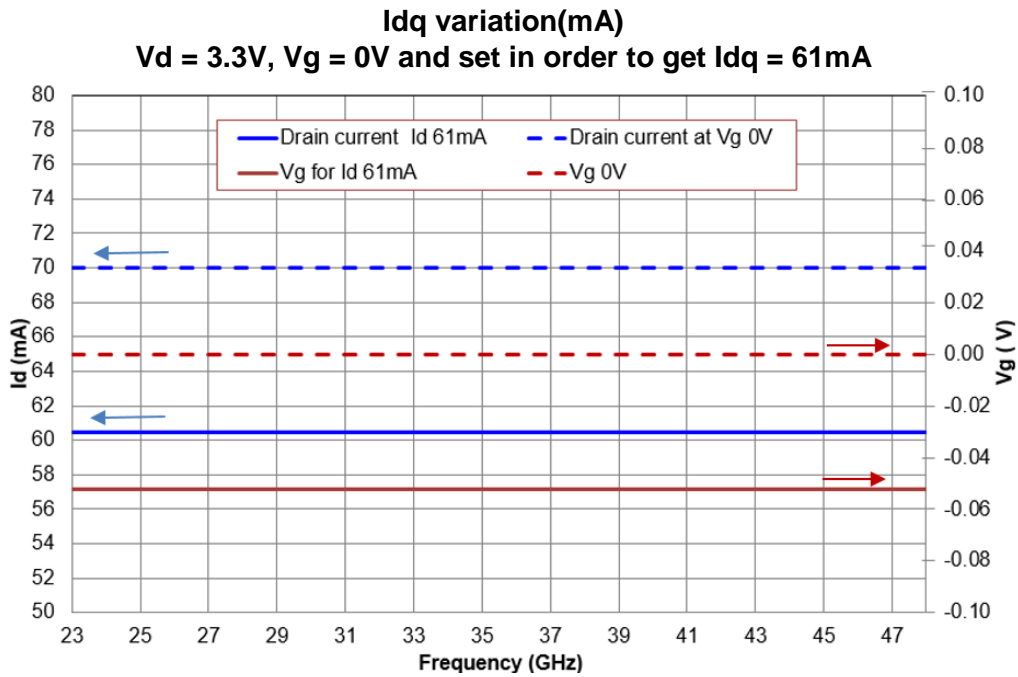
Noise Figure versus frequency
Vd = 3.3V, Vg = 0V and set in order to get Idq = 61mA



Typical Board Measurements

Tamb. = +25°C, Vd = 3.3V, Vg = 0V and Vg set in order to obtain Idq = 61mA

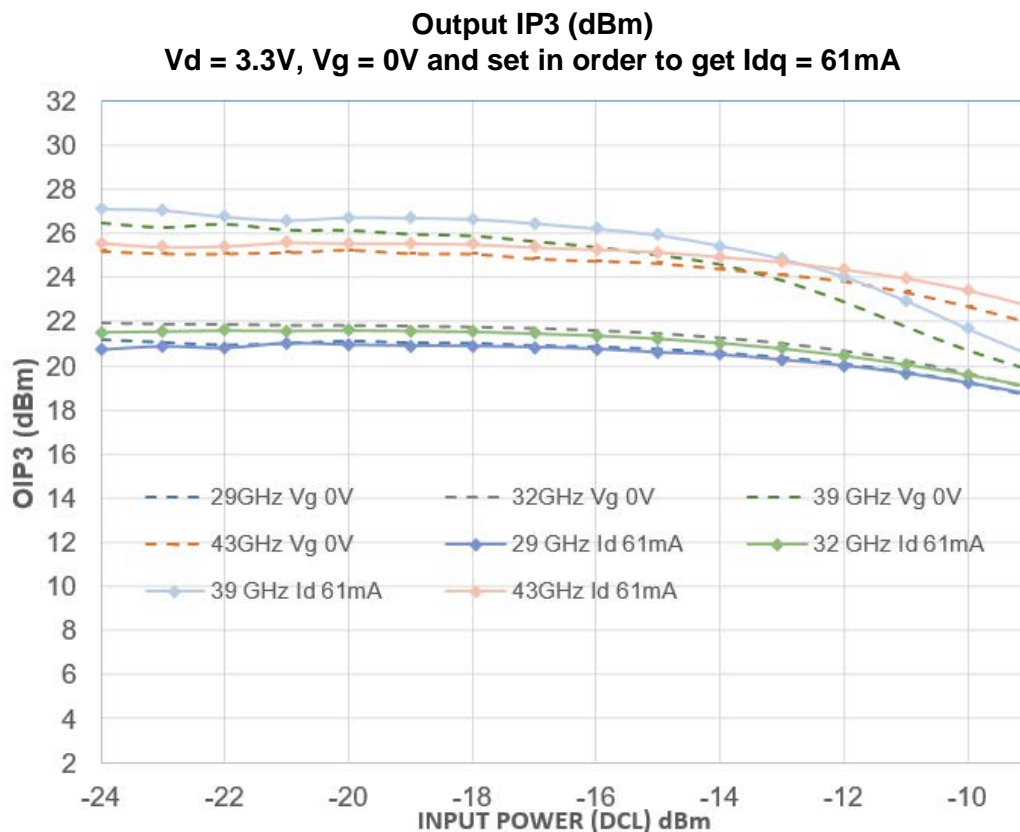
Losses due to board are de-embedded. Measurements are given in the QFN's access plan



Typical Board Measurements

Tamb.= +25°C, Vd = 3.3V, Vg = 0V and Vg set in order to obtain Idq = 61mA

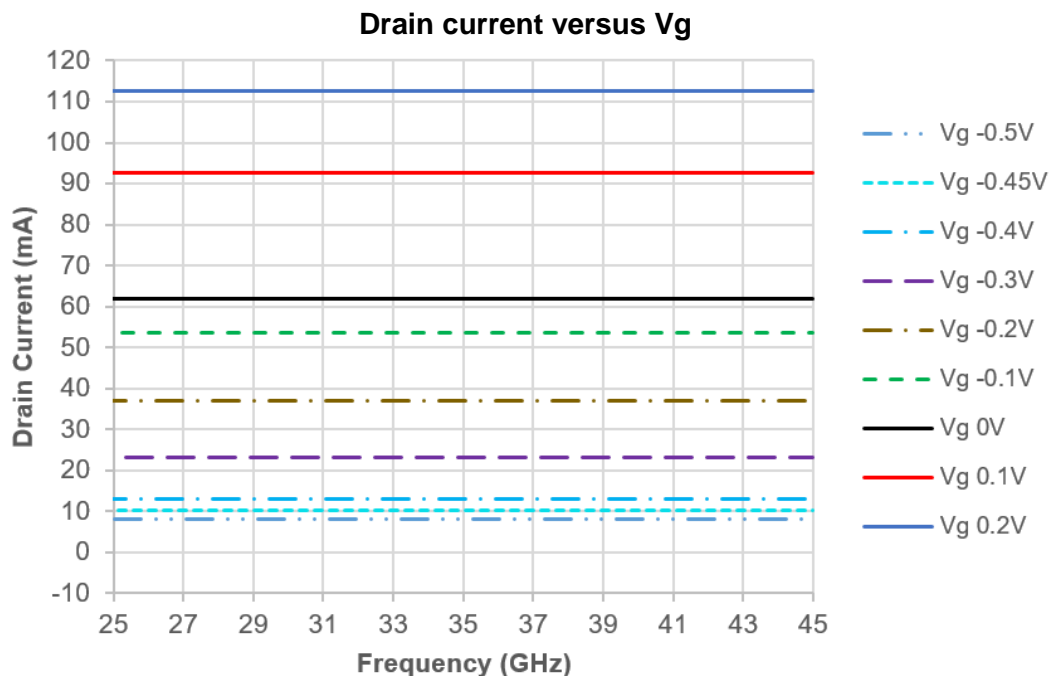
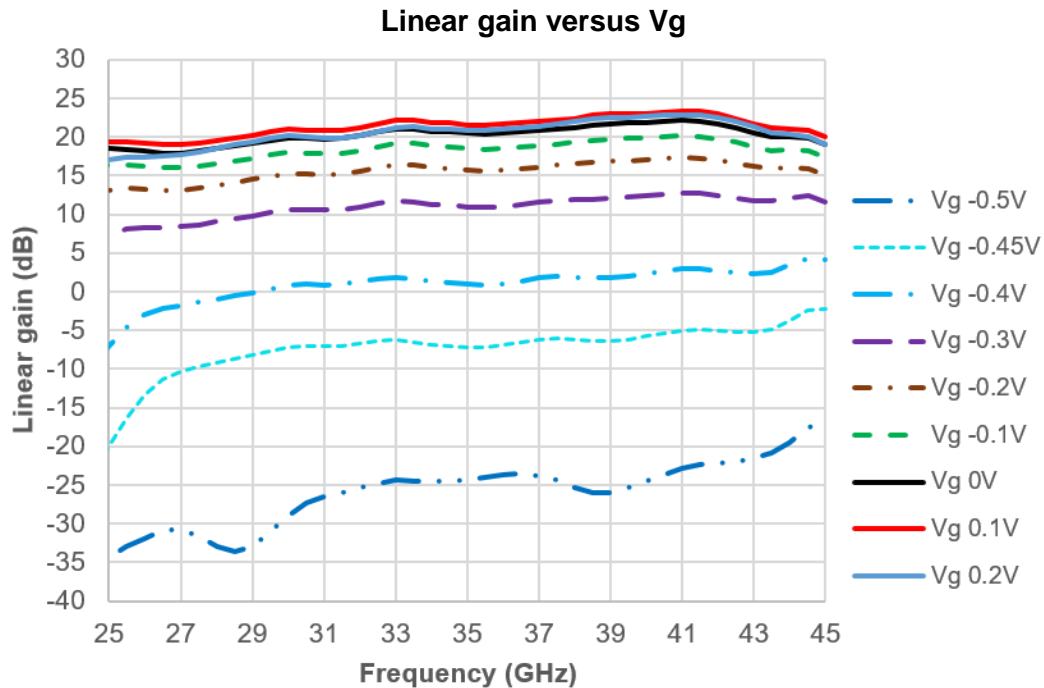
Losses due to board are de-embedded. Measurements are given in the QFN's access plan



Typical Board Measurements

Tamb.= +25°C ,Vd = 3.3V

Losses due to board are de-embedded. Measurements are given in the QFN's access plan

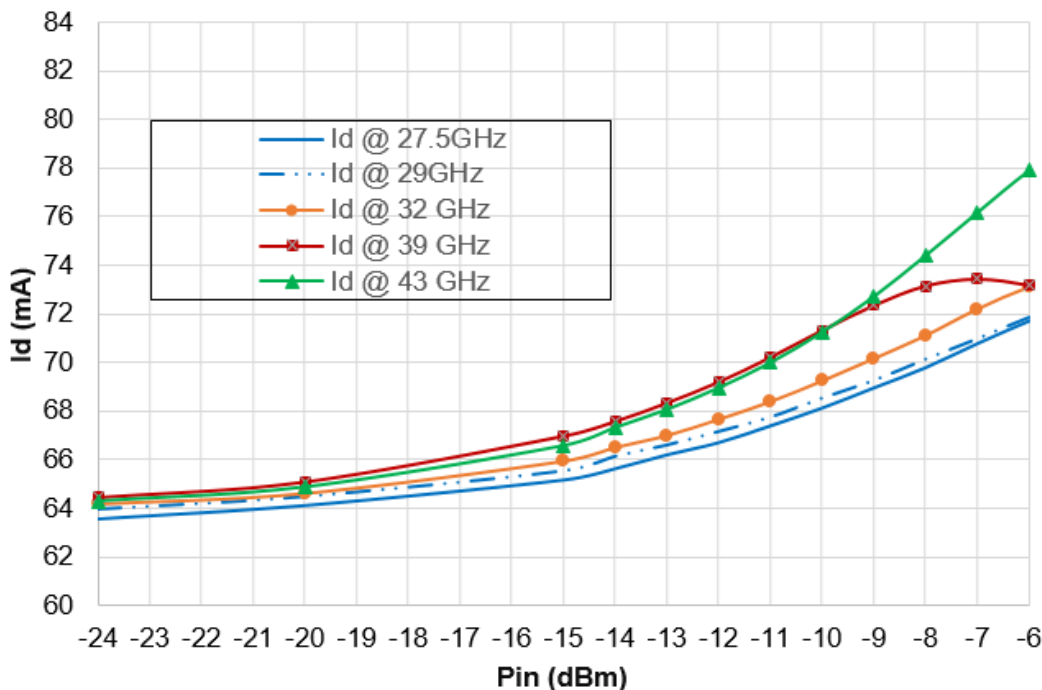


Typical Board Measurements

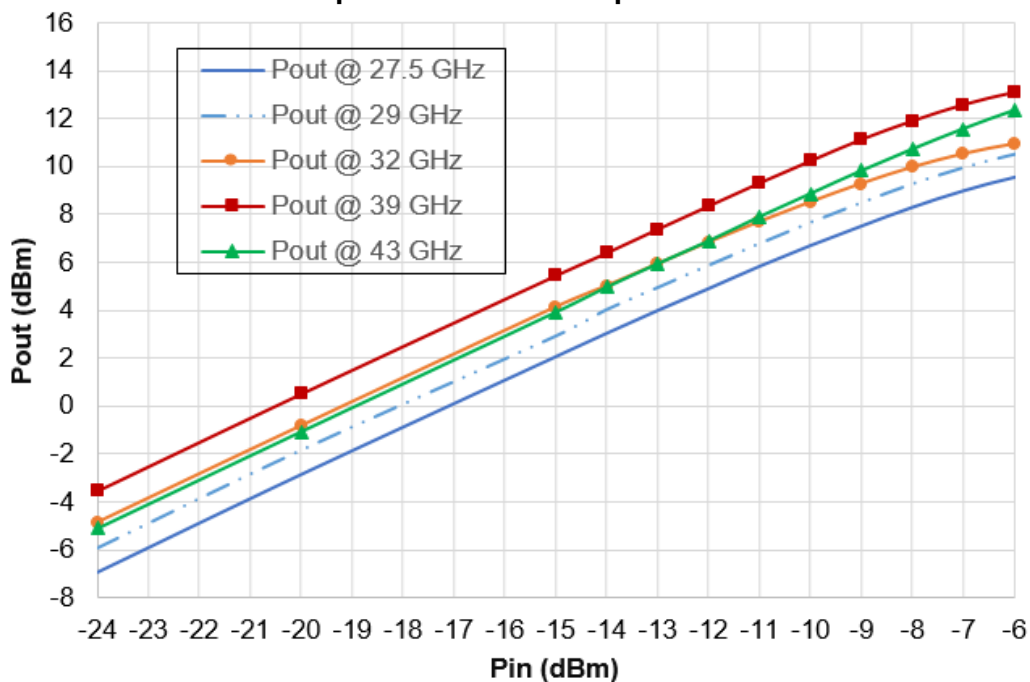
Tamb.= +25°C, Vd = 3.3V, Id = 61mA

Losses due to board are de-embedded. Measurements are given in the QFN's access plan

Drain current (Id) versus Input Power



Output Power versus Input Power

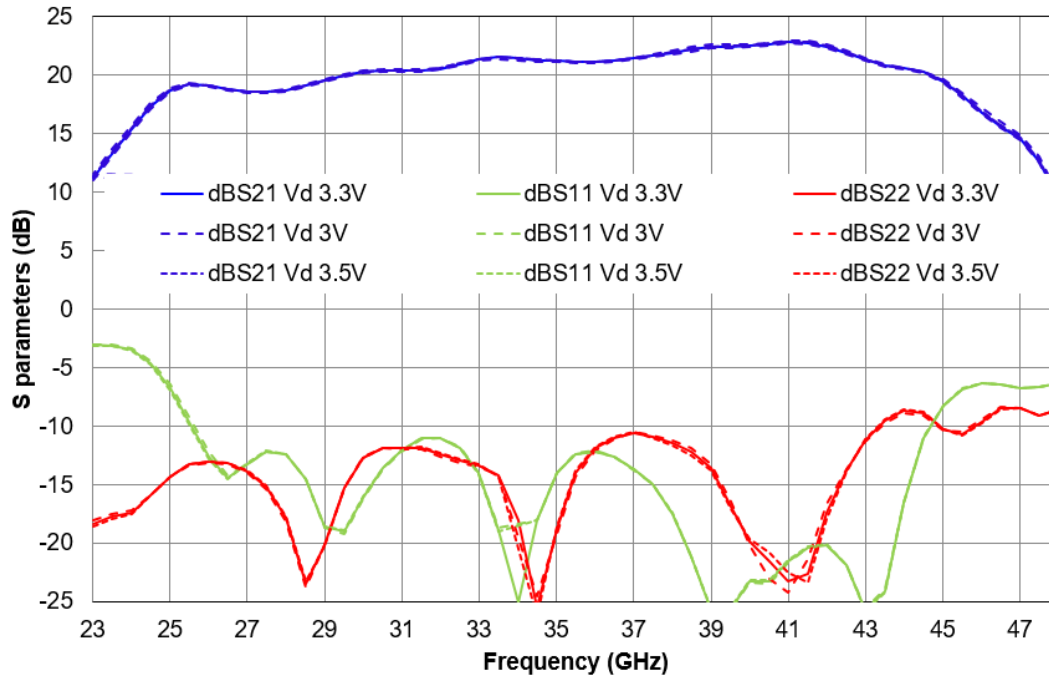


Typical Board Measurements

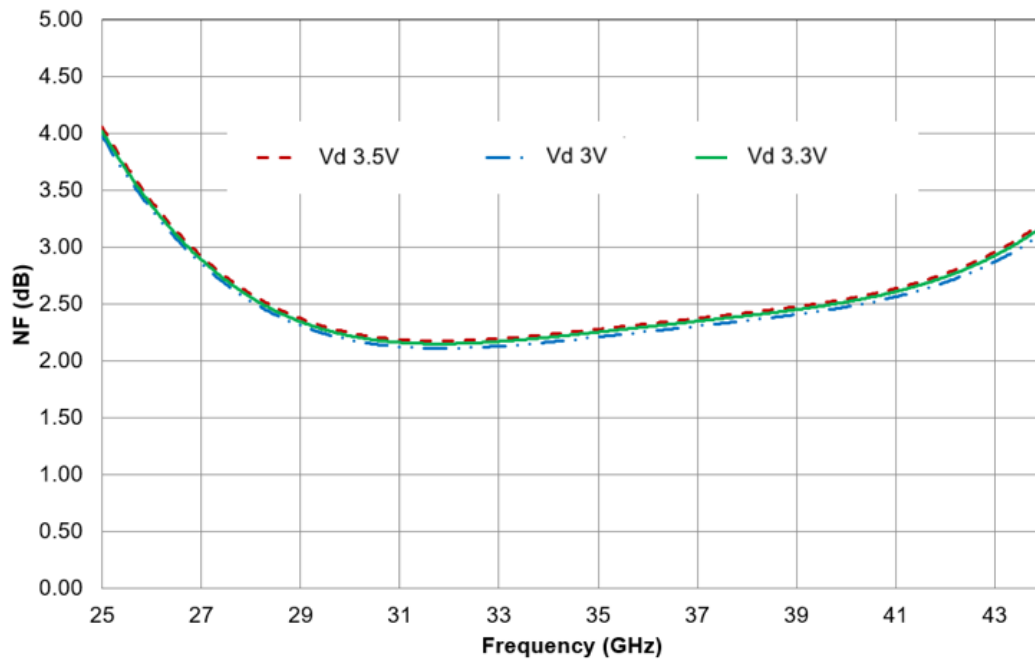
Tamb.= +25°C , Vg = 0V

Losses due to board are de-embedded. Measurements are given in the QFN's access plan

Linear Gain and Return Losses versus drain voltage variation



**Noise figure versus drain voltage variation
(3.0V, 3.3V, 3.5V)**

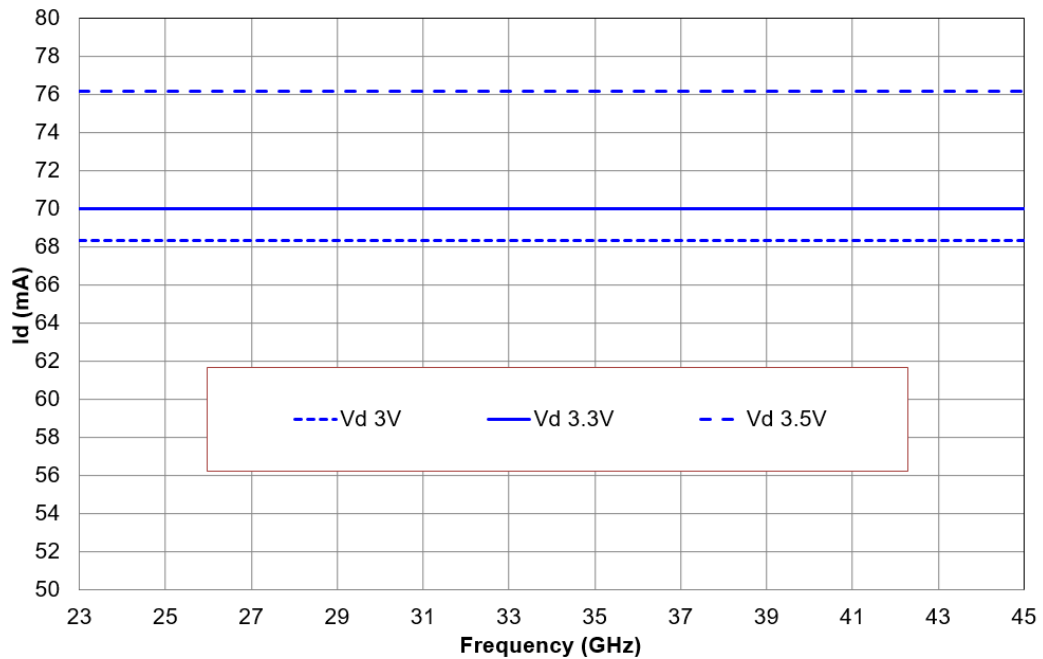


Typical Board Measurements

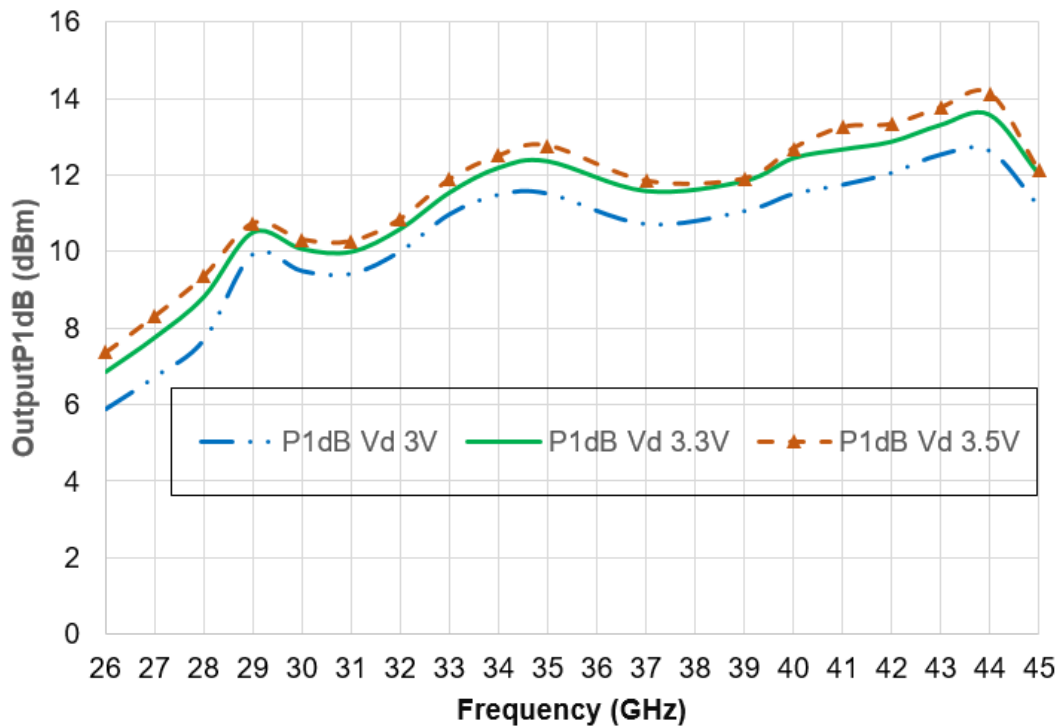
Tamb.= +25°C , Vg = 0V

Losses due to board are de-embedded. Measurements are given in the QFN's access plan

Idq variation versus drain voltage variation



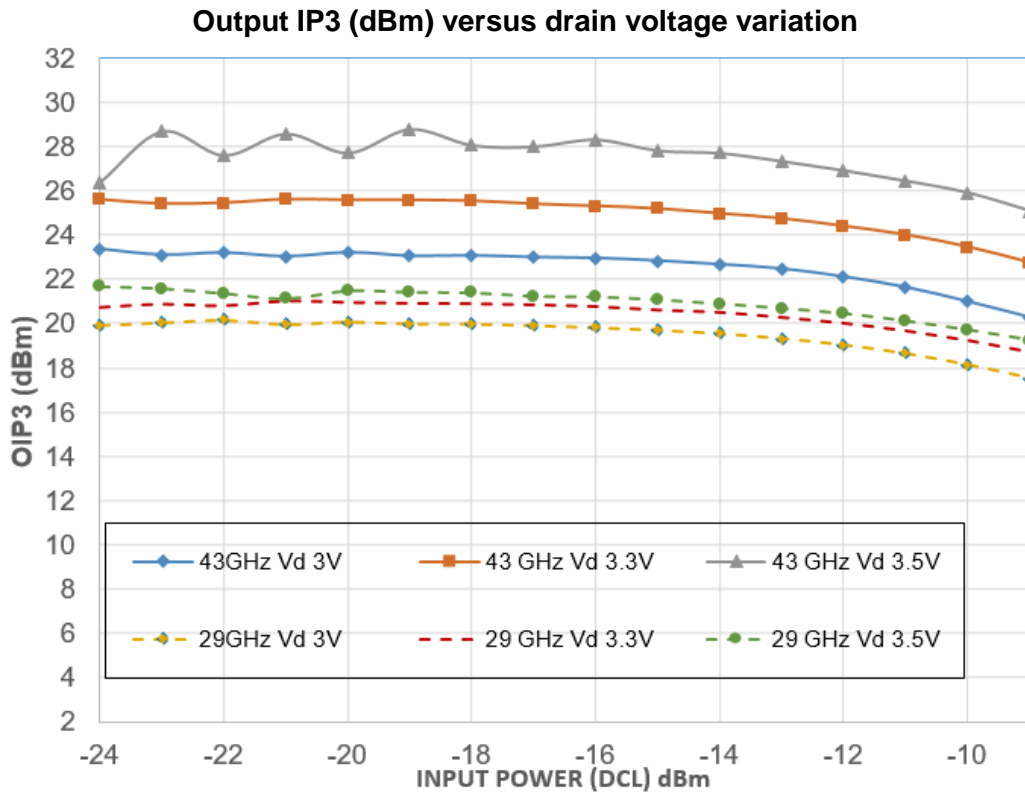
Output Power at 1dB gain compression versus drain voltage variation



Typical Board Measurements

Tamb.= +25°C , Vg = 0V

Losses due to board are de-embedded. Measurements are given in the QFN's access plan

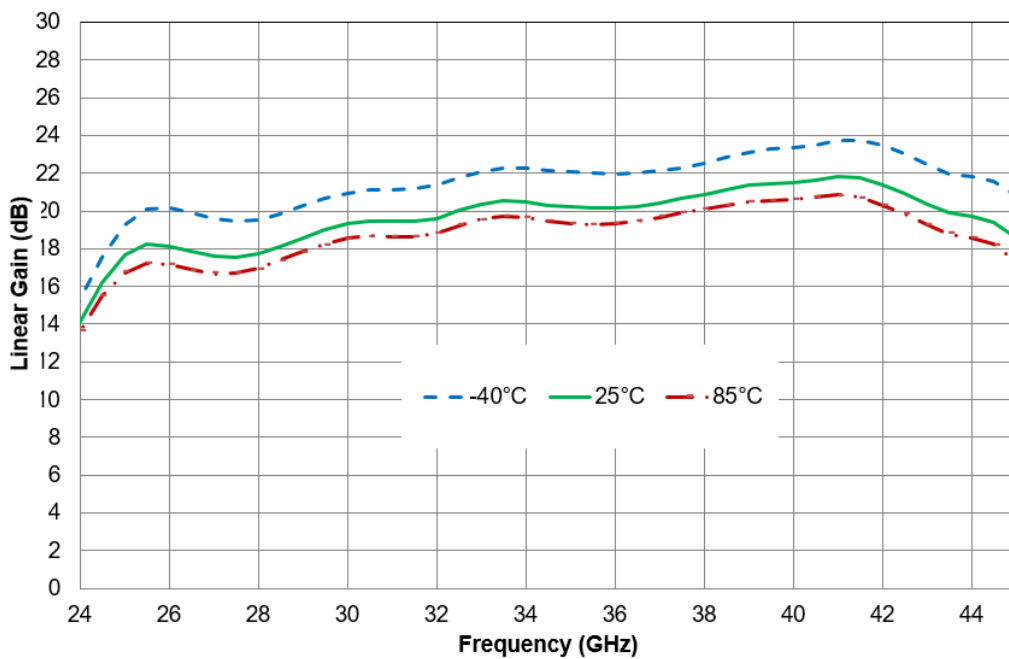


Typical Board Measurements

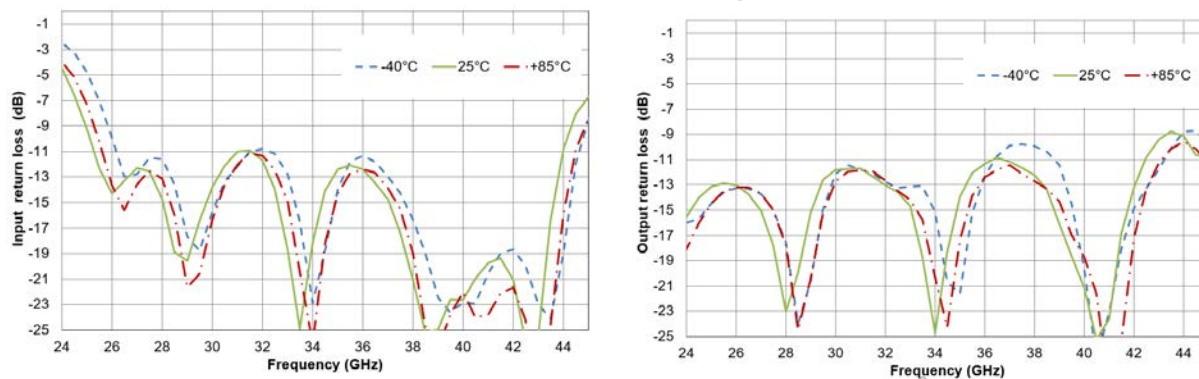
Measurement in temperature, $V_d = 3.3V$, $V_g = 0V$

Losses due to board are de-embedded. Measurements are given in the QFN's access plan

Linear Gain versus temperature



Return Losses versus temperature

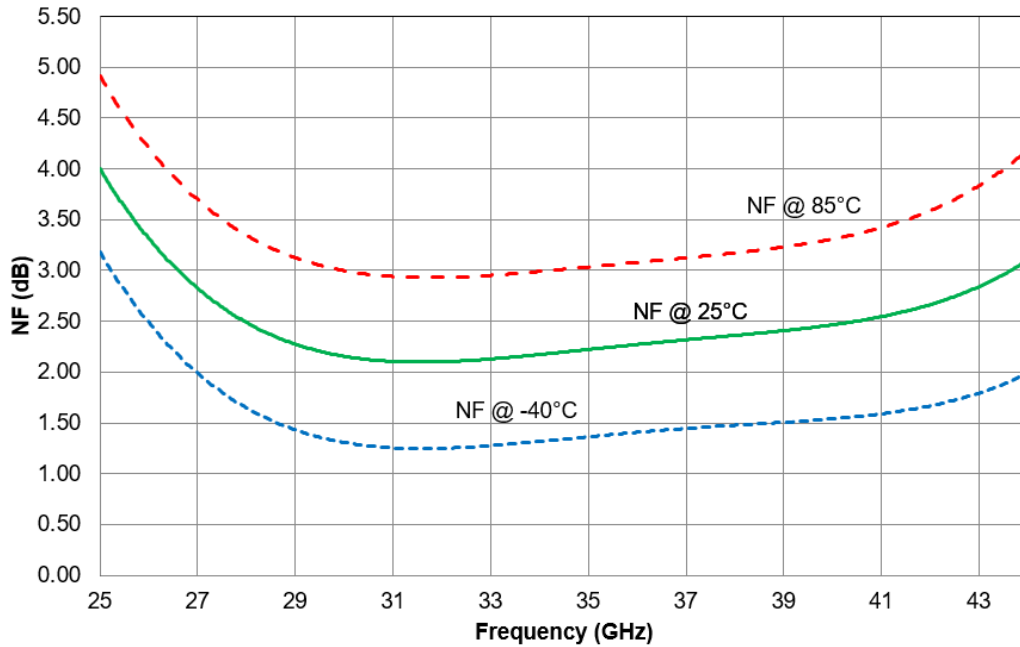


Typical Board Measurements

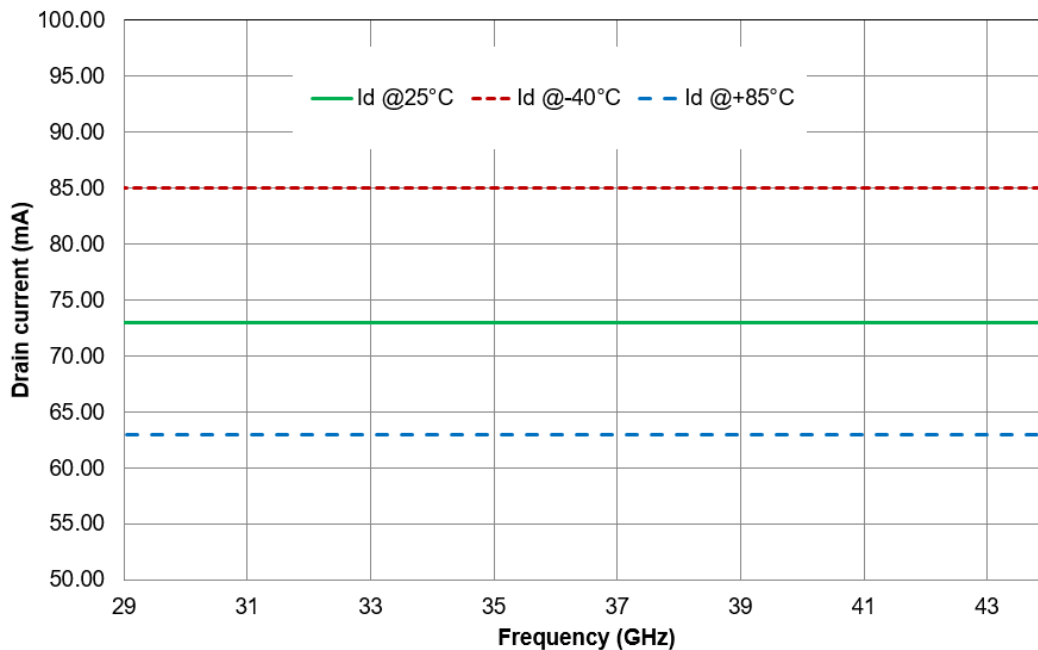
Measurement in temperature, $V_d = 3.3V$, $V_g = 0V$

Losses due to board are de-embedded. Measurements are given in the QFN's access plan

Noise figure versus temperature



Drain current versus temperature $V_g = 0V$

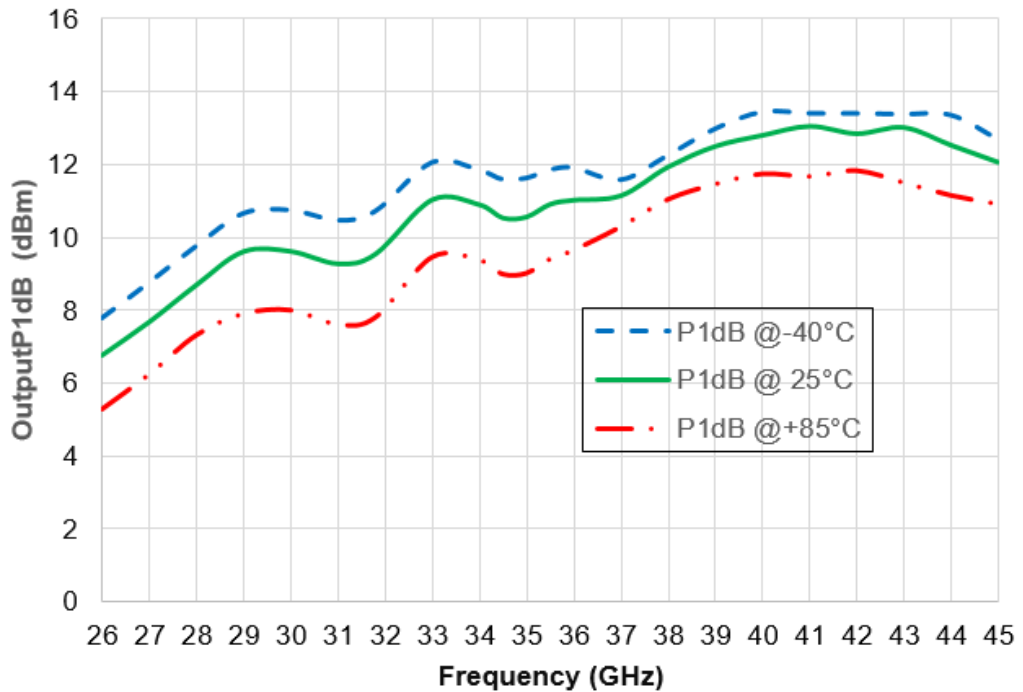


Typical Board Measurements

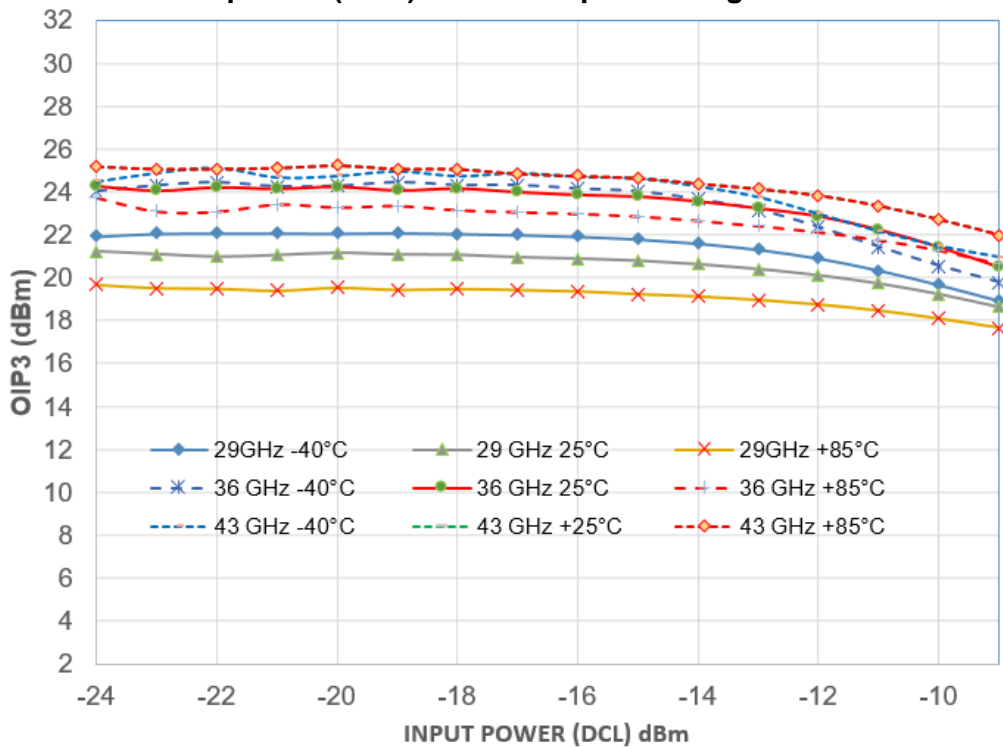
Measurement in temperature, Vd = 3.3V, Vg = 0V

Losses due to board are de-embedded. Measurements are given in the QFN's access plan

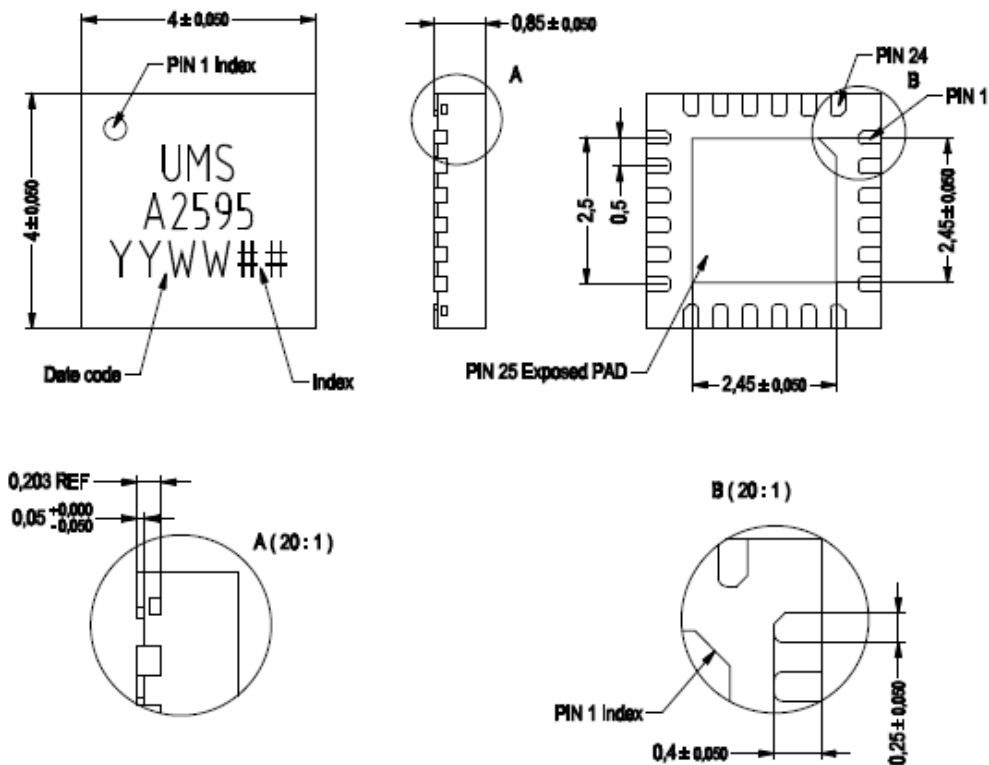
Output Power at 1dB gain compression versus temperature



Output IP3 (dBm) versus temperature Vg = 0V



Package outline ⁽¹⁾



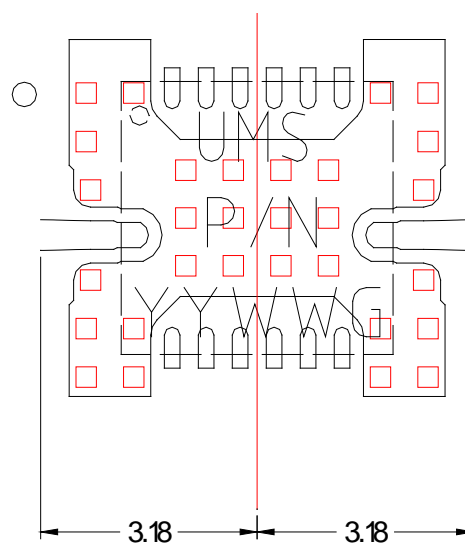
Matte tin, Lead Free	(Green)	1- Nc	9- G2	17- Gnd ⁽²⁾
Units :	mm	2- Gnd ⁽²⁾	10- G3	18- Nc
From the standard :	JEDEC MO-220 (VGGD)	3- Gnd ⁽²⁾	11- Gnd ⁽²⁾	19- Nc
		4- RF in	12- Nc	20- Gnd ⁽²⁾
	25 GND	5- Gnd ⁽²⁾	13- Gnd ⁽²⁾	21- D
		6- Gnd ⁽²⁾	14- Gnd ⁽²⁾	22- Nc
		7- Nc	15- RF out	23- Nc
		8- G1	16- Gnd ⁽²⁾	24- Nc

⁽¹⁾ The package outline drawing included to this data-sheet is given for indication. Refer to the application note AN0017 (<https://www.ums-rf.com>) for exact package dimensions.

⁽²⁾ It is strongly recommended to ground all pins marked “Gnd” through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

Definition of the Sij reference planes

The reference planes used for Sij measurements given above are symmetrical from the symmetrical axis of the package (see drawing beside). The input and output reference planes are located at 3.18mm offset (input wise and output wise respectively) from this axis. Then, the given Sij parameters incorporate the land pattern of the evaluation motherboard recommended in paragraph "Evaluation motherboard".



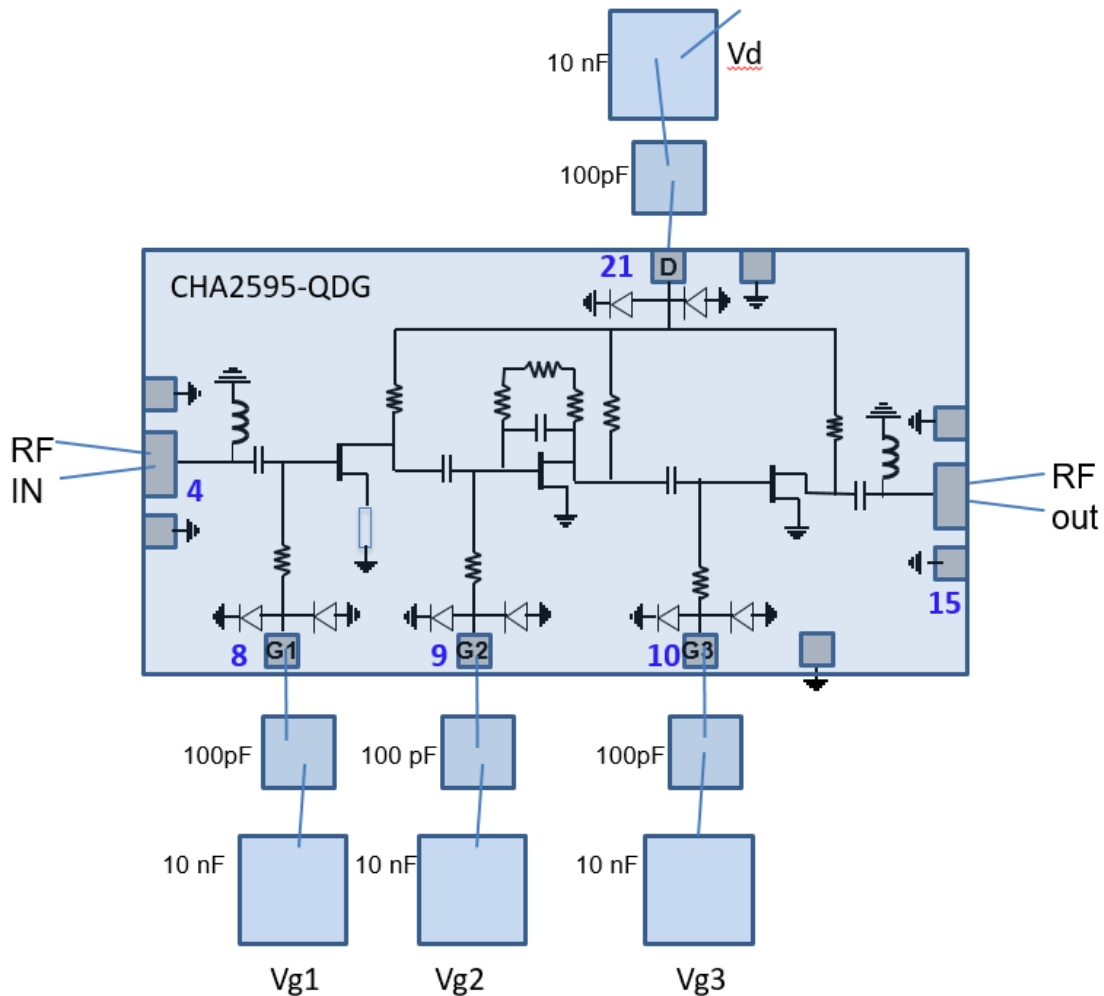
ESD sensitivity

Standard	Value
JS-001-2017	HBM Class 1B (500V passed)
JESD22 A115	MM Class A (50V passed)
JESD22-C101	CDM Class IV (2kV passed)

Package Information

Parameter	Value
Package body material	RoHS-compliant
	Low stress Injection Molded Plastic
Lead finish	100% matte tin (Sn)
MSL Rating	MSL1

Application Circuit:



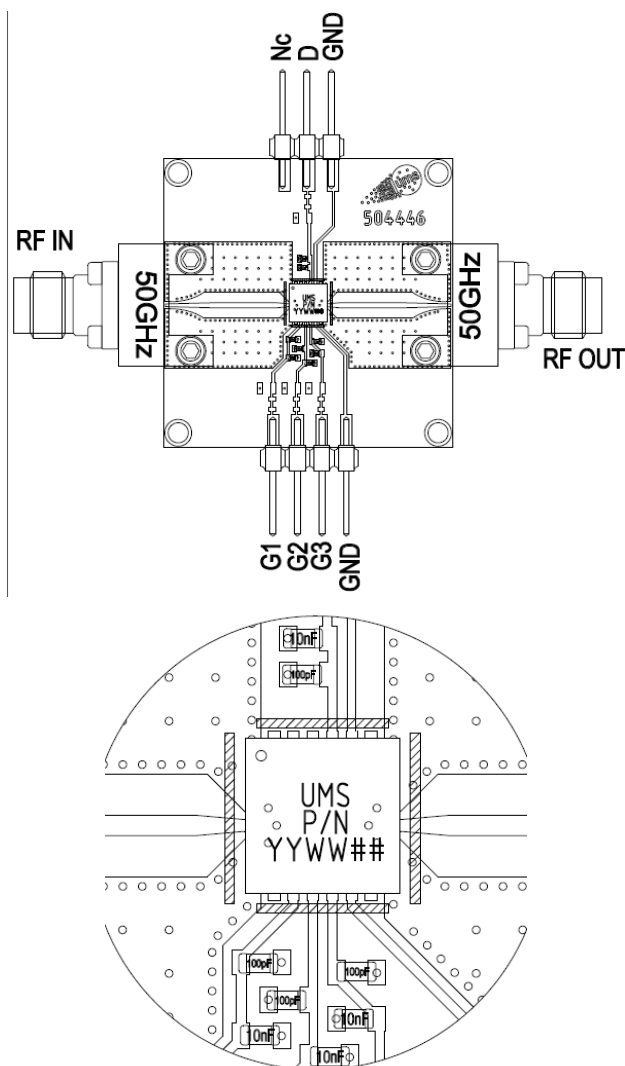
Depending on the board, additional capacitors such as 1 μ F may be added on each biasing access if necessary, for better low frequency decoupling.

Pin Description:

Pin	Symbol	Description
2,3,5,6,11,13,14,16,17,20,25 (exposed PAD)	GND	Must be grounded properly, internal connections to ground are made
1,7,12,18,19,22,23,24	NC	No internal connections
4	RF IN	RF input
15	RF OUT	RF output
8,9,10	VG1, VG2, VG3	Gate voltage, bias network required
19	RF OUT	RF output
21	Vd	Drain voltage, bias network required

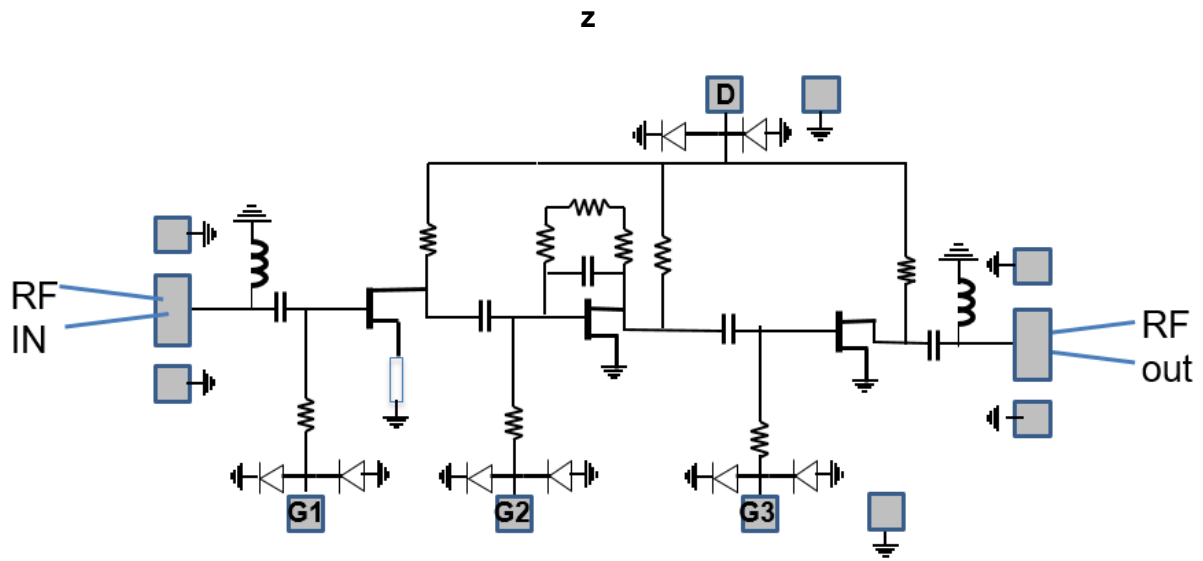
Evaluation mother board

- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a micro-strip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 10nF \pm 10% are recommended for all DC accesses.
- See application note AN0017 for details.



Note: All board measurements are performed using shielded cables, even for DC bias, to ensure safe operation.

DC Schematic & biasing



CHA2595-QDG

Notes

Due to ESD protection circuits on RF input and output, an external capacitance might be requested to isolate the product from external voltage that could be present on the RF accesses.

ESD protections are also implemented on gate and control accesses.

The DC connections do not include any decoupling capacitor in package, therefore it is mandatory to provide a good external DC decoupling (10nF) on the PC board, as close as possible to the package.

Recommended package footprint

Refer to the application note AN0017 available at <https://www.ums-rf.com> for package footprint recommendations.

SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACH N°1907/2006. More environmental data are available in the application note AN0019 also available at <https://www.ums-rf.com>.

Recommended ESD management

Refer to the application note AN0020 available at <https://www.ums-rf.com> for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

QFN 4x4 package:

CHA2595-QDG/XY

Stick: XY = 20

Tape & reel: XY = 21

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